PSEC6: an 8-Channel 40 GSa/s Waveform Sampling ASIC in TSMC 65nm with 10.24 GHz PLL

Ahan Datta[a,*], Andrew Arzac[a], Davide Braga[b], Gordon Chen[a], Troy England[b], Farah Fahim[b], Henry J. Frisch[a], Nathan Gehl[a], Mary Heintz[a], Sumin Kim[a], Ava Lalich[a], Jinseo Park[d], Nathaniel J. Pastika[b], Hector D. Rico-Aniles[c], Paul M. Rubinov[b], Xiaoran Wang[b], Y.M. Richmond Yeung[a]

[a] *Enrico Fermi Institute, the University of Chicago, 933 East 56th Street, 60637, Chicago, IL, USA*
[b] *Fermi National Accelerator Laboratory, 60510, Batavia, IL, USA*
[c] *North Central College, 30 N. Brainard Street, 60540, Naperville, IL, USA*
[d] *Stanford University, 450 Jane Stanford Way, 94305, Stanford, CA, USA*

Abstract

Picosecond level timing resolution is a prerequisite capability for improved coincidence matching, time-of-flight measurements, and secondary vertex reconstruction. Here, we present the specification, design, and simulation results for a new Application Specific Integrated Circuit (ASIC), called PSEC6, in the TSMC 65nm process. It features 8 channels, a maximum sampling rate of 40 GSa/s, a buffer length of 204.8 nanoseconds, and a 10.24 GHz Phase Locked Loop (PLL), which is the first of its kind in the 65nm CMOS process. The event readout rate is 32 kHz, with the digitization done by an off-chip Analog-to-Digital Converter (ADC).

Simulations predict a 4.0 GHz analog input bandwidth and 20 mW per channel during sampling; the 10.24 GHz PLL has a predicted jitter of 550 fs RMS at 15.7 mW. The paper describes the sampling architecture, chip signal paths, PLL design, and presents simulation results.

Keywords: Waveform-Sampling, ASIC, 4 GHz Bandwidth, 65nm CMOS, Switched Capacitor Array

1. Introduction

Single picosecond timing resolution is key to implementing high accuracy time-of-flight measurements and secondary/tertiary vertex reconstruction at colliders. One possible application would be the digitization of signals from a Large-Area-Picosecond-Photodetector (LAPPD), for example [1]. For these applications, the readout electronics must be multi-hit capable, have a long buffer, a high sampling rate, a high analog bandwidth, and a low power consumption [2]. These criteria define the specifications of PSEC6, as given in Table 1.

PSEC6 is an extension of the PSEC5 ASIC which was taped out in August 2024 [3]. For PSEC6, we have added a 10.24 GHz PLL to reduce timing drift across sampling runs. We additionally re-designed the clock divider chain and digital blocks to eliminate failure modes that appeared during the testing of PSEC5.

PSEC6 is expected to achieve single picosecond timing resolution with a 40 GSa/s sampling rate and a 4 GHz analog bandwidth. Simulations predict average power consumption of each of the eight channels to be 20 mW and of the PLL to be 15.7 mW.

PSEC6 relies on an external ADC to convert the sampled capacitor voltages to digital data. This reduces chip complexity, power cost, and die size while allowing for flexibility in the choice of ADC. Using a 40 MHz ADC, we estimate a dead time per event of 32 μs.

The block diagram of the chip is given in Figure 1. Each detector input is buffered through to the sampling switches. The sampling switches are triggered by the sampling clock at 10 GHz, driven from the PLL. The sampled voltages are read out using a further pair of source followers to external ADCs. The various settings on the chip are controlled by the digital block [4].

Process	65nm TSMC
Signal to Noise	1000
Sampling Rate	**40GSa/s (5GSa/s)**
Fast Buffer Length	4×1.6 ns
Slow Buffer Length	204.8ns
Analog Bandwidth	4.9 GHz
Power Consumption (Sampling)	20 mW (per channel)
Channels/Chip	8
Area	2.7 mm^2
Readout Rate	32 kHz

Table 1: Specifications for PSEC6 ASIC

*Corresponding author
Email address: ahand@uchicago.edu (Ahan Datta)

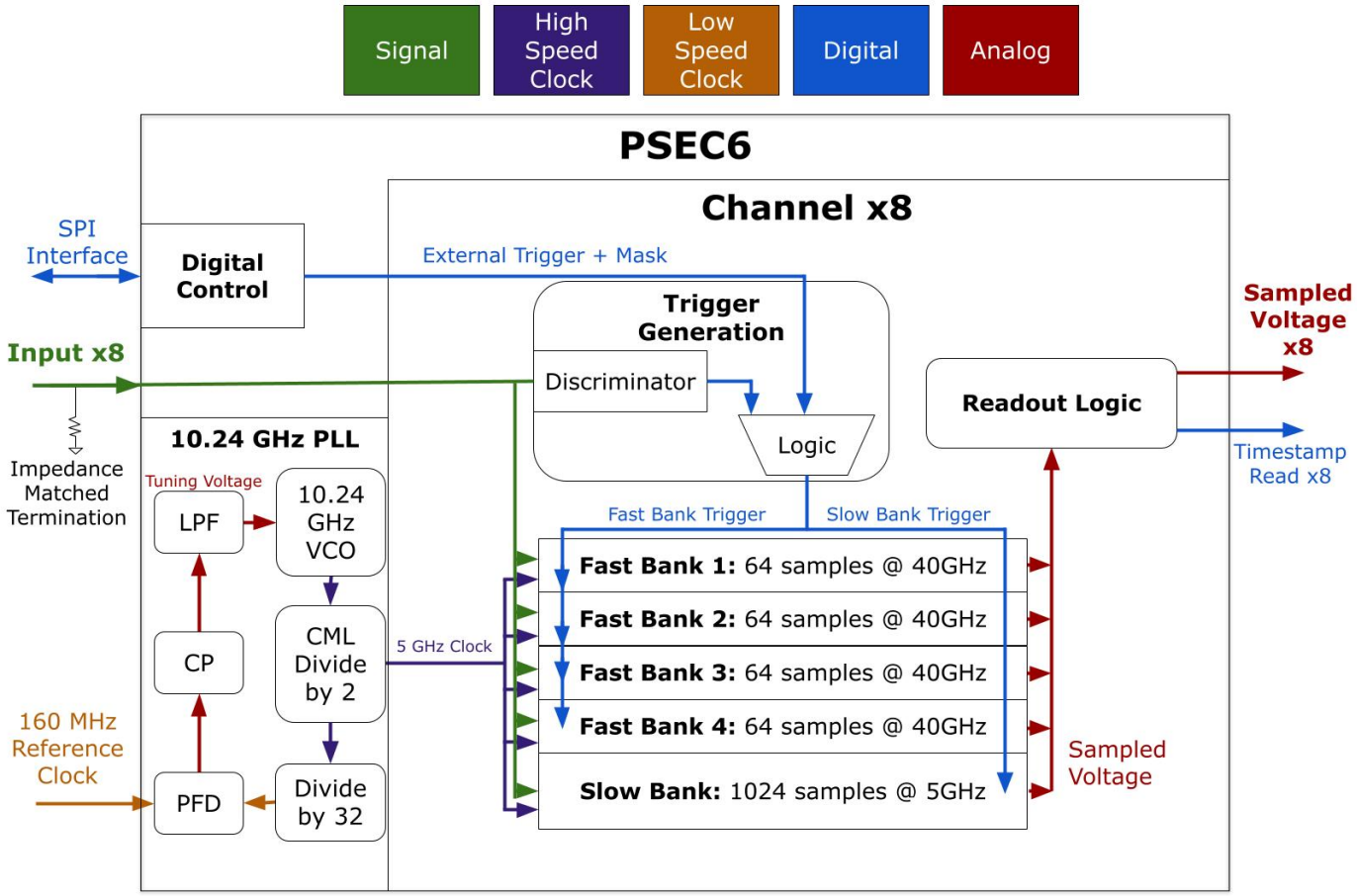

Figure 1: **Block diagram for PSEC6**: The layout and different sampling frequencies of the fast and slow buffer switched capacitor array (SCA) architectures are shown. The fast banks are triggered by the per-channel trigger generation logic. The sampling clock is generated by the 10.24 GHz PLL. The analog readout is controlled by the digital readout logic and fed into external ADCs for digitization. The initialisms in the PLL are defined in Section 4.

2. Switched Capacitor Array

Switched Capacitor Arrays (SCA) are sequentially-triggered capacitor-based sample-and-hold circuits which sample the voltage input at a frequency determined by the input clock frequency. Given that each sample captures a certain time segment and that the number of sampling capacitors per channel is fixed due to size considerations, there is an inverse relationship between sampling rate and buffer length.

2.1. Fast and Slow Bank Architecture

To achieve both a high sampling rate and a long sampling window, we employ two different types of SCAs: fast banks and slow banks. In each channel, there are four fast banks and one slow bank. The slow bank samples at 5 GSa/s over a buffer length of 204.8 nanoseconds. The four independent fast banks sample at 40 GSa/s with a shorter buffer length of 1.6 nanoseconds each. The fast banks are triggered by a discriminator whose parameters are controlled by the user [3].

To achieve a 40 GSa/s sampling rate from a 10 GHz clock, the fast buffers employ a four-phase interleaved sampling scheme. The sampling clock incurs four 90° phase offsets within each fast buffer. Thus, the fast buffer can sample at 40 GSa/s while being driven by a single 10 GHz clock. The 10 GHz clock is divided once to provide the 5 GHz sampling clock for the slow buffer.

The user has the choice to either run the fast buffers sequentially or to allow each fast buffer to run independently. In the former case, there is a 6.4 nanosecond sampling window for a single event. In the latter case, the chip is multi-hit capable for up to four distinct events, with a sampling window of 1.6 nanoseconds per event. PSEC6 can also be configured to sample two distinct events with a sampling window 3.2 nanoseconds per event.

The slow buffer fulfills two purposes. For one, it samples the baseline of the detector, allowing for baseline calibration and noise characterization. Additionally, it serves as a long time series in which to temporally locate the events captured in the fast bank. This is especially important for applications that rely on time differences, such as time-of-flight.

2.2. Switch Design

The choice of sampling switch is important for three characteristics: analog bandwidth, physical gate length, and transition

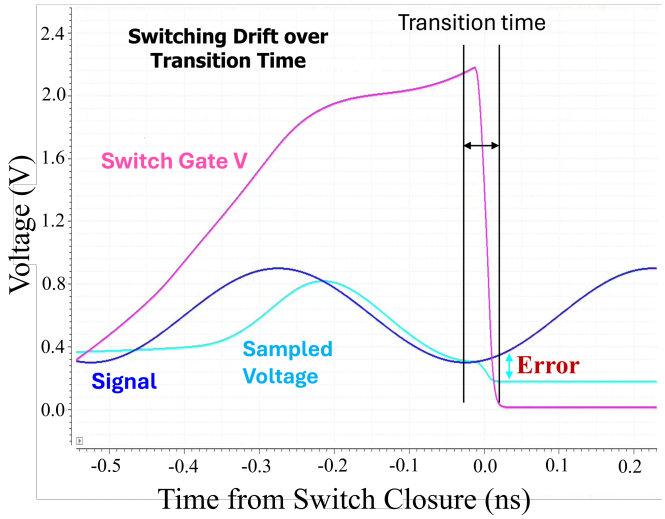

Figure 2: **Simulation of the Switching Drift**: A SPICE Simulation of the switching drift induced by a finite gate voltage (light pink) transition time on the order of 0.1 nanoseconds. The sampled voltage (light blue) drifts away from the true signal (dark blue) during the transition window, which adds a systematic error into the sample. The gate voltage is a 2.5V peak-to-peak digital signal driven by a dual-edge-triggered flip-flop (see Section 2.3). The delay and non-linearity between the signal and sampled voltage prior to the gate voltage transition is due to the non-idealities of the input buffer and parasitic elements along the signal path.

time. High analog bandwidth is important to resolve the rising edge and separation between pulses with short rise times. Physical gate length is a tradeoff between larger process variation at shorter lengths and larger area requirements at longer lengths. A low transition time is important to reduce charge leakage after sampling, which induces irreducible systematic error (see Figure 2).

As a compromise between these three characteristics, we chose to use an I/O voltage (2.5 V) NMOS transistor with 280 nanometer gate length. The I/O voltage NMOS switch has a 6 GHz bandwidth and a hold time exceeding 20 μs at the cost of a longer gate length. Our clock voltage, however, is 1.2 V, meaning that we need a 1.2 V to 2.5 V voltage level shifter. The schematic used is in Figure 3.

2.3. Clock Distribution

A key input to the SCA is the sampling clock which triggers the sequential sample-and-hold circuits. We need the sampling clock to be low jitter with a near 50% duty cycle. Furthermore, the fast banks must see a sampling clock frequency of 10 GHz. Unfortunately, parasitic elements of the clock distribution network make the distribution of a 10 GHz clock across the chip technically difficult and power intensive. Thus, we opt to distribute a 5 GHz clock across the chip instead of the 10 GHz clock.

The clock distribution is handled by the buffer chain shown in Figure 4. A 5.12 GHz clock is generated by the PLL and distributed outward in two directions through a chain of large buffers: one branch to channels one through four, and one to

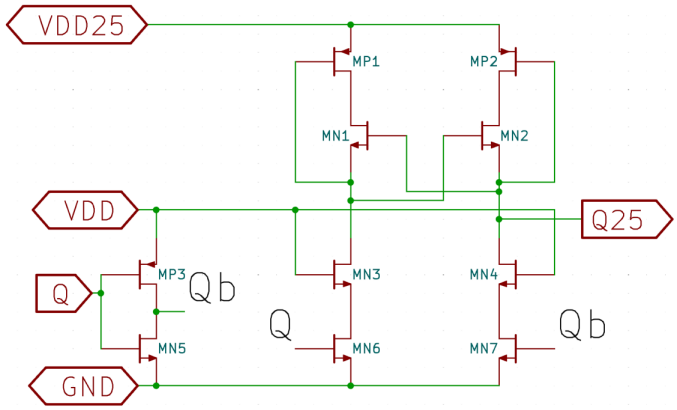

Figure 3: **Shifting the Gate Voltage**: Schematic of voltage level shifter required to convert the 1.2V CMOS sampling clock to the 2.5V gate voltage required for the NMOS I/O voltage sampling switch.

channels five through eight. Along each branch, one large buffer stage is placed between consecutive channels to maintain signal integrity. The clock inputs of channels two through seven are driven by a middle-size buffer, while channels one and eight use a small buffer. This difference in input-buffer sizing reflects the differing loads on the large buffers: the large buffers feeding channels two through seven drive both a channel input buffer and the next large buffer in the chain, whereas the large buffers at the two ends (channels one and eight) drive only a single channel input buffer.

At each channel, 5 GHz distributed clock is converted to the 10 GHz sampling clock using an existing design of a Dual-Edge-Triggered Flip Flop (DET FF), as shown in Figure 5 [5]. The typical problems of dual-edge triggering, high power consumption and instability, are avoided by careful simulation of the duty cycle and jitter tolerances across the process variations likely to be seen by the chip.

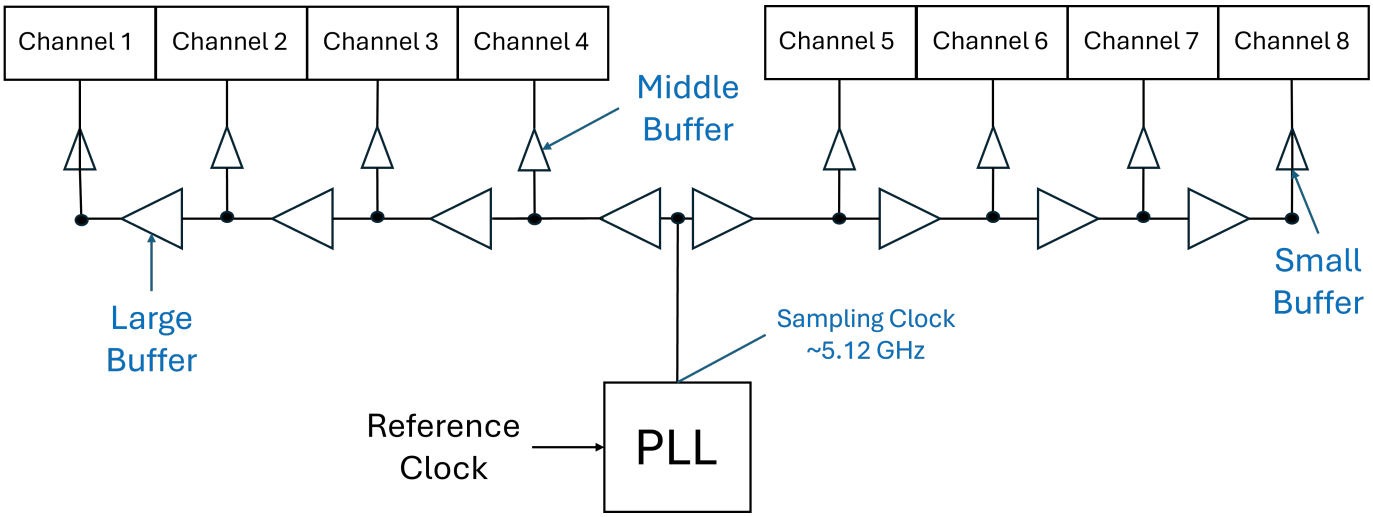

Figure 4: **Clock Distribution Buffer Chain**: Block diagram description of the clock distribution buffer chain. Each buffer is a chain of four inverters. The transistor widths of the buffers are in a ratio of 4:2:1.

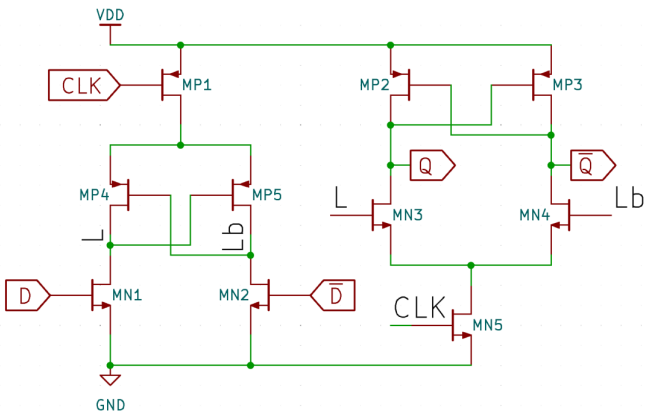

Figure 5: **Doubling the Clock Frequency**: Schematic of the dual-edge-triggered flip-flop (DET FF) used to reduce the distributed clock frequency to 5 GHz while maintaining the sampling frequency of 40 GSa/s.

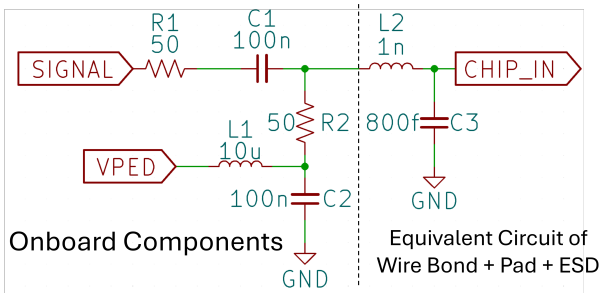

Figure 6: **Chip Entry Path**: Schematic of expected on-board components and parasitic components, arising from the ESD protection and pad devices on the chip, used for SPICE verification of the bandwidth. The pedestal voltage, V_{ped}, is expected to be supplied externally to bias the detector signal into the optimal range for the input buffer and discriminator.

3. Signal Paths

The critical signal paths for the chip are the input path and the analog readout path. The input path is defined to be the path between the package pin input for the detector voltage and the sampling switch. The readout path is defined to be the path from the sampling capacitor to the package pin output of the sampled voltage. See the green and red paths respectively in Figure 1 for reference.

3.1. Input Signal Path

The input path is characterized by the components shown in Figure 6. The onboard components will be on the PCB (Printed Circuit Board) which carries the chip, provides the biases, and AC-couples the detector output to the chip. The components shown on the right are parasitics due to the wirebond, input pad, and ESD protection devices. A SPICE simulation of the schematic returned an analog bandwidth of 4.0 GHz.

To reduce the loading on the detector output, we employ a source follower as shown in Figure 7. The simulated analog bandwidth of the source follower was found to be 4.9 GHz. Thus, the effective analog bandwidth of the input signal path is 4.0 GHz.

3.2. Readout

The readout of the chip is controlled by a 40 MHz readout clock. At each rising edge of the readout clock, the voltage from the next sampling capacitor in each channel is sent to the corresponding readout pin of the chip. To reduce the charge leakage from the small sampling capacitors (35 fF), the output is buffered through two source followers, similar to the schematic in Figure 7, directly to the pad. The output to the pad is analog and is digitized by an external ADC located on the PCB.

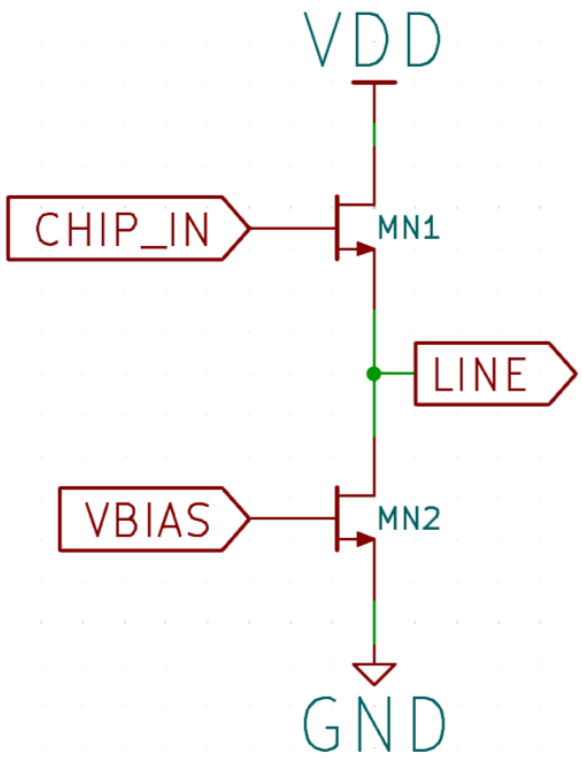

Figure 7: **Input Buffer for the Signal**: Schematic of the input source follower for the detector signal. The bottom NMOS acts as a current source, using a global voltage bias, and the top NMOS takes the signal input. The bandwidth of this source follower was simulated to be 4.9 GHz.

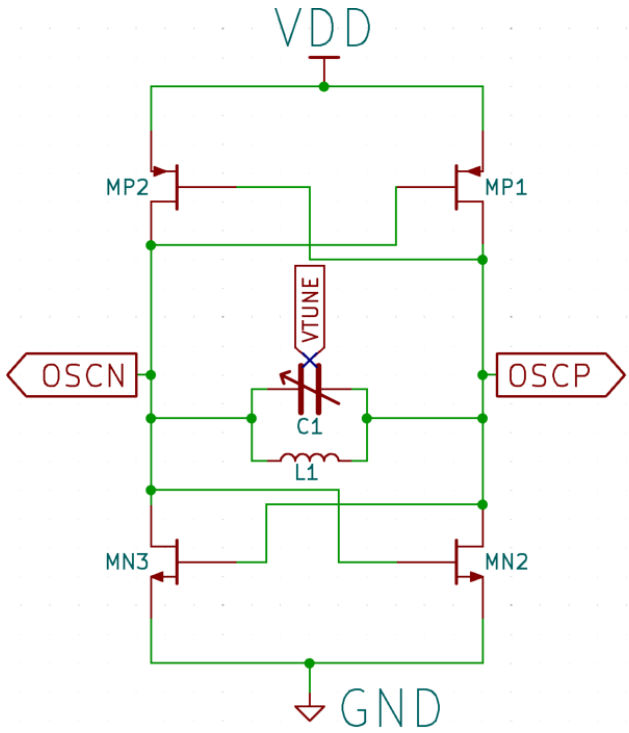

Figure 8: **Voltage Controlled *LC*-Oscillator**: Schematic of the LC-oscillator based Voltage Controlled Oscillator (VCO) used for the PLL. The capacitor and inductor values are tuned to have a central frequency value of 10.24 GHz. The capacitance value is voltage-controlled using both an analog varactor and a digital switched capacitor bank.

4. Phase Locked Loop

A Phase Locked Loop (PLL) is a feedback loop in phase space to lock the phase of an oscillator to that of an external reference [6, 7]. Figure 1 shows a block diagram of the PLL.

The PLL architecture is as follows. The 10.24 GHz output of the oscillator is first divided down by 64, creating a 160 MHz PLL clock. The PLL clock is compared against a 160 MHz reference clock, supplied by a crystal oscillator, to find the phase error by the Phase Frequency Detector. This phase error is then converted to a correcting voltage using a Charge Pump and Loop Filter, closing the loop [8].

4.1. Voltage Controlled Oscillator

The Voltage Controlled Oscillator (VCO) for this PLL, shown in Figure 8, is a 10.24 GHz center frequency *LC*-VCO. The VCO has a digital binary switched capacitor bank to adjust the frequency range. The VCO also has an analog control voltage, V_{tune}, with a gain parameter $K_{\text{VCO}} \approx 220$ MHz/V, and has a maximum tuning range of 9.75 GHz to 11.04 GHz. The PLL is implemented using the analog feedback, V_{tune}.

4.2. Divider Chain

The divider chain converts the 10.24 GHz output of the VCO into the 5.12 GHz sampling clock and the 160 MHz PLL clock, as shown in Figure 9. The first level of divider is implemented in Current-Mode Logic (CML), which uses more power and can operate at higher frequencies. The output of the first level divider is used for the 5.12 GHz sampling clock. The CML stage designs were derived from References [9, 10]. The second level of dividers is built in True-Single-Phase-Clock logic (TSPC logic), striking a balance between power consumption and operating frequency [11]. The third and final level of divider is constructed using a single flip-flop divider to lower the power consumption. The output of the third level dividers is used for the 160 MHz PLL clock.

4.3. Phase Frequency Detector

The Phase Frequency Detector (PFD) used in this PLL is shown in Figure 10. Lower reset times improve the stability and locking time of the PLL by decreasing the total feedback path delay of the PLL [12, 13]. Thus, we use a `NOR` gate in the reset path to minimize the reset time of the PFD. This has the added benefit of symmetrically loading the two D-flip-flops used in the PFD, which reduces the magnitude of reference spurs caused by PLL asymmetry.

4.4. Charge Pump

The Charge Pump (CP) design used in the PLL is given in Figure 11. This charge pump is a current-steering design using NMOS steering transistors for symmetry. The current sink bias is controllable by the user to determine the right balance of

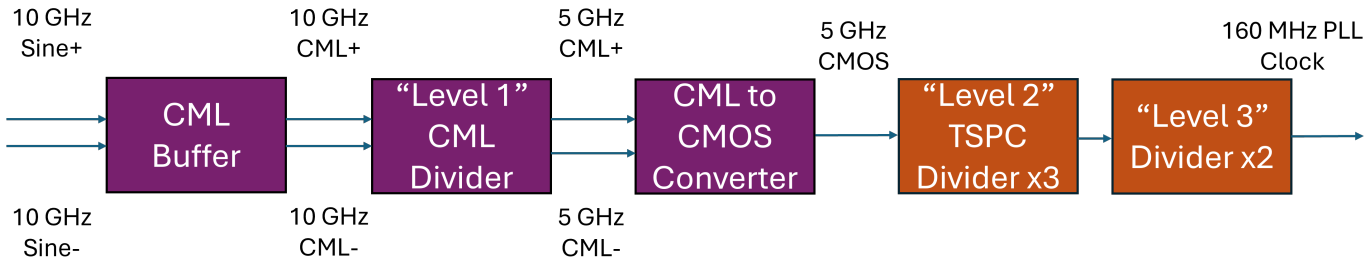

Figure 9: **PLL Clock Divider Chain**: Block diagram description of the divider chain used for the PLL feedback, sampling clock, and output clock paths. The first stage, shown in purple, uses Current-Mode Logic (CML), trading high power consumption for 10.24 GHz division. The later stages, which operate at lower frequencies, are shown in orange. The second level dividers use True Single Phase Clock (TSPC) logic, balancing power consumption and speed. The third level dividers are standard single flip-flop dividers for minimal power consumption.

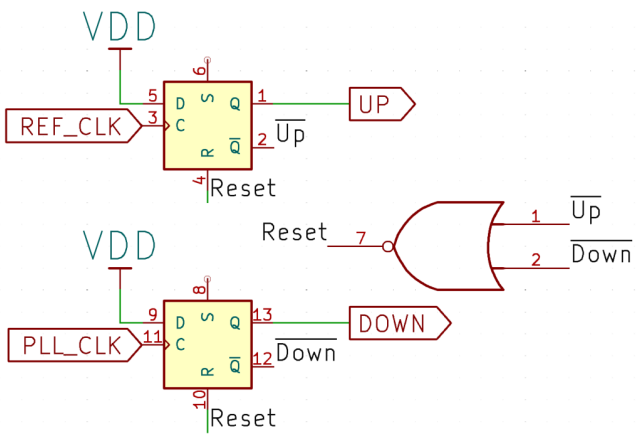

Figure 10: **Phase Frequency Detector**: Schematic of the two-flip-flop Phase Frequency Detector (PFD) used in the PLL. The feedback path is designed around a NOR gate to minimize the reset path time, which improves the stability and performance of the PLL.

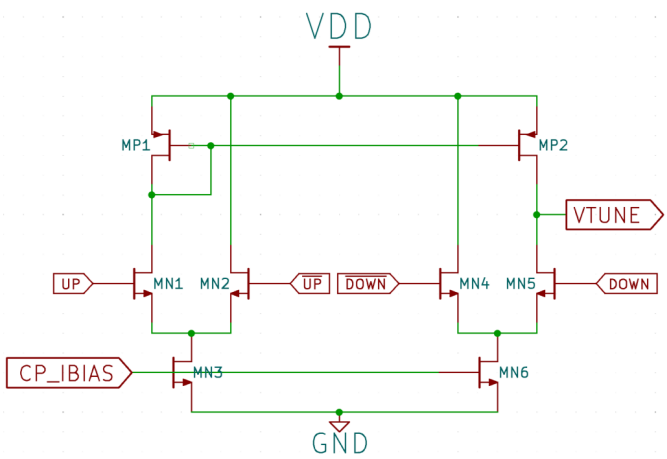

Figure 11: **Charge Pump**: Schematic of the symmetric Charge Pump (CP) used in the PLL. The use of primarily NMOS transistors for both the up and down path reduces the asymmetry in the feedback paths, as it avoids the inherent characteristic difference between PMOS and NMOS transistors. The current mirror required for the up path induces a minor asymmetry in the design, hurting performance.

phase margin, power consumption, and settling time. The current mirror in the up path introduces some unavoidable asymmetry. This CP was modeled from an existing design [14].

4.5. Loop Filter

The Loop Filter (LPF) used in this PLL is shown in Figure 12. The LPF smooths the output of the charge pump and determines the phase margin and poles of the PLL. The LPF component sizing controls the phase margin, which is critical to the PLL stability. Process variation can shift the value of R by up to 20%. Thus, we implemented a tunable resistor between 750 Ω and 1.6 kΩ to ensure that the PLL is always stable.

4.6. PLL Simulation Results

The results of simulating the PLL in the typical process corner are shown in Figure 13. The convergence voltage, V_0, being near mid-rail implies that the PLL frequency and VCO center frequency match. The convergence timescale, ω_0, is on the order of microseconds, which meets the desired specifications. The detailed PLL specifications across corners are given in Table 2.

Figure of Merit	**Value**
Frequency	10.24 GHz
Average Total Power	P_{typ} = 15.7 mW P_{max} = 76.6 mW
RMS Jitter	J_{typ} = 550 fs J_{max} = 814 fs
Duty Cycle of Sampling Clock	46.3 – 54.8%
Charge Pump Current	I_{cp} = 200 μA
Characteristic Damping Time Scale	$\tau = 1 - 2\ \mu s$
Phase Margin	50.13°

Table 2: PSEC6 10.24 GHz PLL simulation parameters and predicted values.

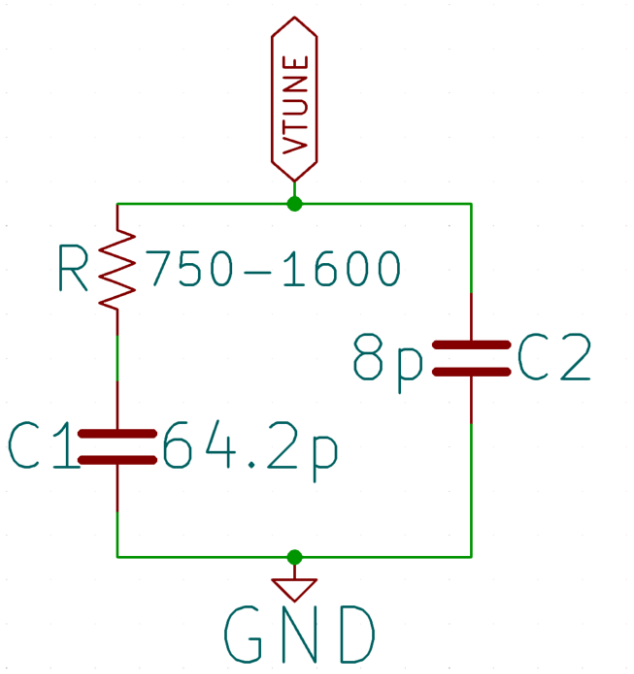

Figure 12: **Loop Filter**: Schematic of the Loop Filter (LPF) used in the PLL. The exact capacitor and resistor values, shown in units of Farads and Ohms respectively, were determined to reduce the loop jitter while maintaining an adequate phase margin. C_2 is kept an order of magnitude smaller than C_1 such that we are able to approximate the PLL as type-II with a simpler pole structure. The resistor is variable using a switched resistor array controlled digitally.

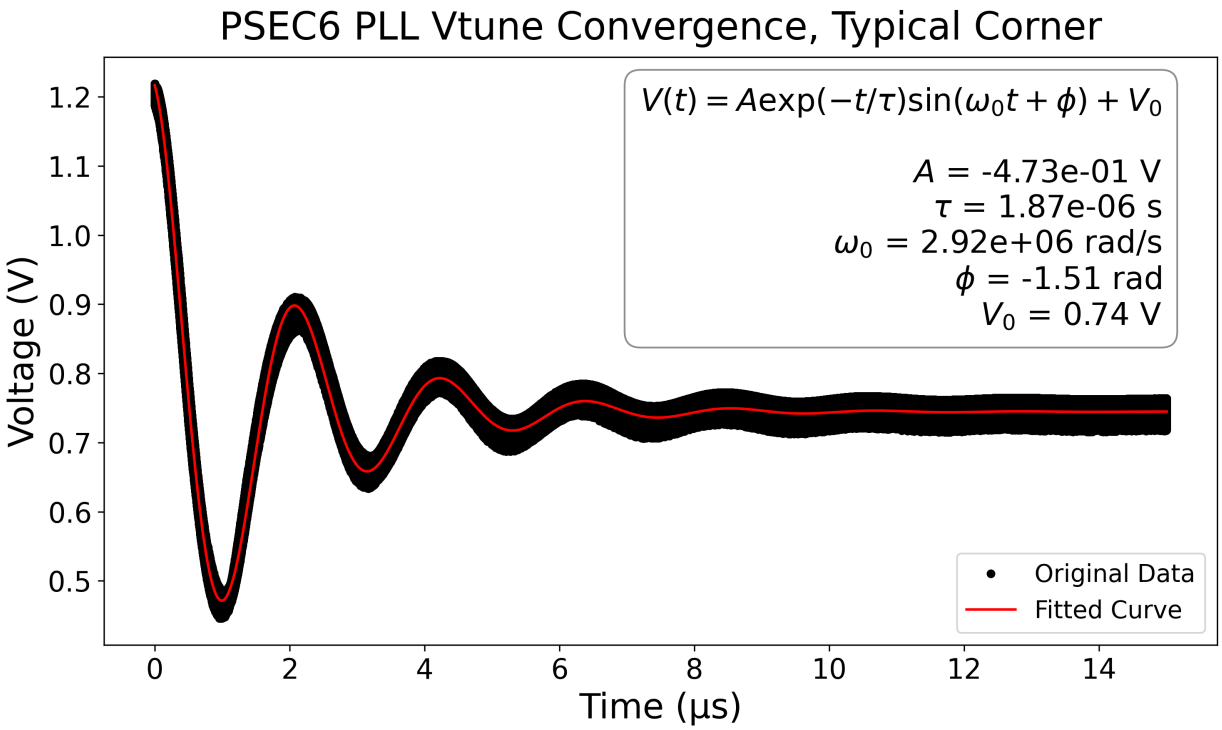

Figure 13: **PLL V_{tune} Convergence**: Plot showing the convergence of V_{tune}, the tuning voltage of the VCO, in time as a function of the PLL. This simulation is done in the typical corner. Using an exponentially decaying sinusoidal fit, we extract a settling voltage, V_0, near mid-rail (0.7446 V) and a natural frequency, ω_0, in agreement with the calculated value.

5. Conclusions

PSEC6 has been taped out as of April 2026, and is scheduled for delivery back from TSMC in July 2026. Simulations predict a 4.0 GHz analog input bandwidth and 20 mW per channel; the 10.24 GHz PLL achieves 550 fs RMS jitter (typical corner) at 15.7 mW. The final layout of PSEC6 is shown in Figure 14. The physical testing of PSEC6 will happen when the chip arrives. Designs of the test setup and applications to experiment for PSEC6 are currently under development.

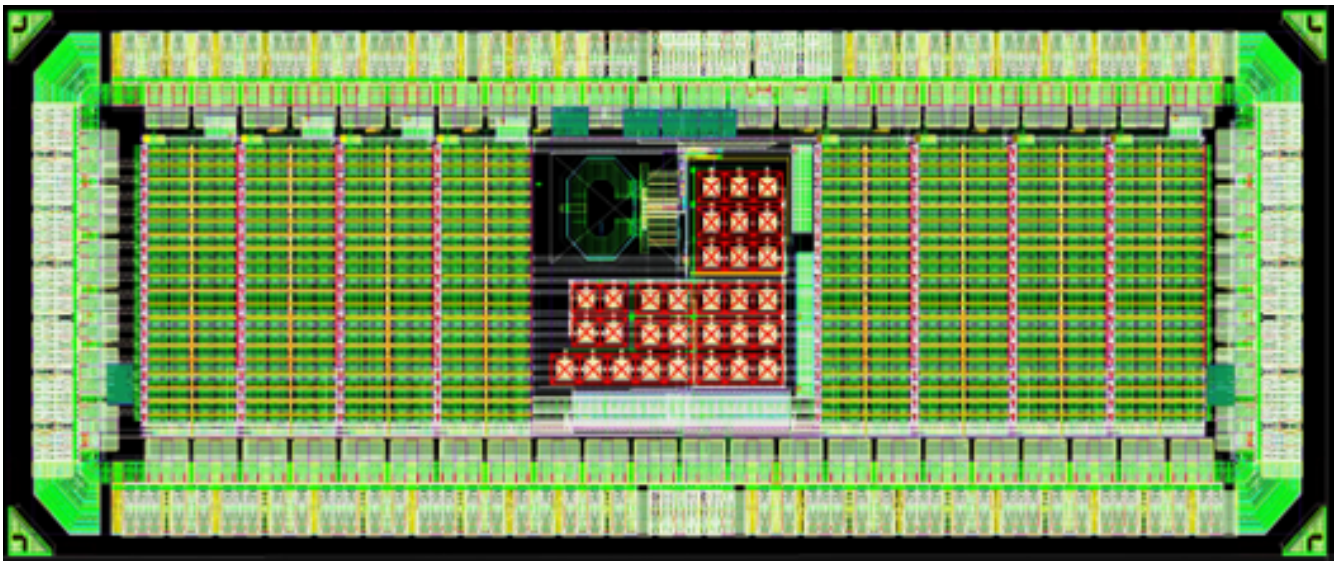

Figure 14: **PSEC6 Layout**: Layout of PSEC6 with guard ring, I/O pads, ESD devices, channels, digital block, and PLL shown. There are eight channels containing SCAs, four on the left half and four on the right half. The PLL is placed in the middle of the chip to minimize the travel distance of the sampling clock. The PLL contains the inductor in the upper left corner and the LPF Metal-Insulator-Metal (MIM) capacitors in the bottom right corner. The power domains of the digital and analog I/O are separated along the I/O ring corners.

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