

PSEC5 Digital Board Outline

Ahan Datta

June 2024

For ACDC Rev C reference, look [here](#).

1 Functionality

The Digital Board (better name needed) will supply the chip with the required inputs to take data. This includes regulated voltages, grounds, ADCs, DACs, and a 40MHz reference clock (on-board 40MHz reference clock compared with chip reference clock using PLL which controls on-chip VCO). Additionally, it will communicate with an external server (need to decide interface).

The board will be split into two components - the “DUT” and the “Control” boards. The DUT board will house all fast components (>5GHz?) which are hard to replace, including the chip, and the Control board will house all other components (~40MHz). We are yet to decide the interface between the two boards.

Each board should have a unique hardware identification chip. We will use this to uniquely tag data when it’s taken to simplify the analysis process.

2 Component List

- ADC ([ad9228](#))
- DAC ([LTC2600](#))
- [K26 Heatsink](#)
- FPGA/FPGA SoM (System on Module) Kria
- 2-channel ADC Buffer ([AD8332ARU](#))
- Multi-Function Gate ([SN74LVC1G97](#)) -DBVTG4?
- **Closing the PLL:**
 - 40MHz Crystal Oscillator ([ASE2-40MHz-E-T](#))
 - OP-AMP ([OPA607QDBVRQ1](#))
 - tiny XOR ([NC7S86M5X](#))

- **Power Circuitry:**

- 2.5V-3.7V DC-DC converter ([LTC3240EDC](#)) ([TPS63031DSKR](#))
- Linear regulators These are linear regulators, [for example](#).

- PSEC5 [1 per DUT Board]

- Samtec HQCD or ERM8 (High mating cycles)

5.12GHz VCO is in the PSEC5 chip. It is divided by 128 in the chip, and 40MHz reference clock is output from the chip. The PFD compares the phase of this clock to that of the on-board PLL clock. The output of the PFD is integrated, digitized, filtered in the FPGA, made analog, and sent to the chip as the control voltage for the PSEC5 VCO.

2.1 Control Board Outline

1. Kria K26
2. ADC
3. 2x DAC
4. 2.5V-3.7V dc-dc converter
5. Linear Regulator
6. Ethernet PHY

2.2 DUT Board Outline

1. Single-Channel DAC ([DAC8411IDCKT](#))
2. PSEC5
3. Single-Channel ADC ([AD4008BCPZ-RL7](#))
4. Multifunction Gate ([SN74LVC1G99](#)) -DBVTG4? NOTE: Need to choose either multifunction or XOR gate.
5. XOR Gate ([NC7S86M5X](#))
6. Op-Amp integrator ([OPA607QDBVRQ1](#))
7. Crystal Oscillator ([ASE2-40MHz-E-T](#))

3 Procedure

3.1 Pedestal Calibration

ch 0-7: fixed DC

Trigger Channel Mask: 00000000 Mode: 10 (Capture 1 edge) Polarity:
00000000 VCO Band: 00011100 PLL Ratio: 128 Slow mode: No

Procedure:

1. Set Disc. $V_{th} = 0$. (No internal trigger generated.)
2. Set Input Buffer V_{bias} .
3. Set Output Buffer V_{bias1} , V_{bias2} .
4. Set Reset $0 \rightarrow 1 \rightarrow 0$. (1 ns pulse.)

CHANNEL STATE: STATE_INIT

5. Write SPI: VCO Digital Band to 00011100. (10.24 GHz. Numbers are subject to PVT variation.)
6. Lock the PLL by tuning the VCO ctrl voltage.
7. (Only necessary with on-chip PLL) Read SPI: PLL locked.
8. Write SPI: Slow mode to 0.
9. Set Signal(ch 0-7) to the desired pedestal DC level
10. Write SPI: Trigger Channel Mask to 00000000. (No internal trigger generated.)
11. Write SPI: Mode to 00000010. (Use 6.4 ns long fast SCA bank.)
12. Write SPI: Disc Polarity to 00000000
13. Write SPI: Instruction to START.

CHANNEL STATE: STATE_INIT -> STATE_SAMPLE_ALL

14. Wait 500 ns. (All capacitor values updated. In theory, this only takes 204.8 ns.)
15. Set Ext. Trigger High. (This stops all Fast and Slow SCA banks.)

CHANNEL STATE: STATE_SAMPLE_ALL -> STATE_STOPPED

16. Set Ext. Trigger Low
17. Write SPI: Instruction to READOUT

CHANNEL STATE: STATE_STOPPED -> STATE_READOUT

18. Feed in Readout CLK (e.g., 40MHz) for 1280 cycles. Feed the same clock to external ADCs (AD9228). Read out from external ADCs at 12 times the clock (in 12-bit mode, 480MHz). This takes 32 μ s at a 40MHz ADC rate.
19. Readout order: (FSCA 63P3, 61P3, ..., 1P3, 2P3, 4P3, ..., 64P3) (FSCA 63P2, 61P2, ..., 1P2, 2P2, 4P2, ..., 64P2) (FSCA 63P1, 61P1, ..., 1P1, 2P1, 4P1, ..., 64P1) (FSCA 63P0, 61P0, ..., 1P0, 2P0, 4P0, ..., 64P0). P means phase. The order of phase is determined by process variation.

3.2 Timebase Calibration

ch 0-7: WR 250MHz Sine wave Trigger Channel Mask: 11111111 Mode: 10 (Capture 1 edge) Polarity: 00000000 VCO Band: 00011100 PLL Ratio: 128 Slow mode: No(Why?)

Procedure:

1. Set Disc. Vth to 700mV.
2. Set Input Buffer Vbias.
3. Set Output Buffer Vbias1, Vbias2.
4. Set Reset High.
5. Set Reset Low.
6. Write SPI: VCO Digital Band to 00011100.
7. Lock the PLL by tuning the VCO ctrl voltage.
8. (Only necessary with on-chip PLL) Read SPI: PLL locked.
9. Write SPI: Slow mode to 0 (Why?).
10. Set Signal(ch 0-7) to the sine wave, DC level = 700mV, Amplitude = 200mV.
11. Write SPI: Trigger Channel Mask to 11111111.
12. Write SPI: Mode to 00000010.
13. Write SPI: Disc Polarity to 00000000.
14. Write SPI: Instruction to START.

15. Wait 500 ns.
16. (Examine one channel.)
 - (a) Assume that we are at the top of the sine wave when the sampling starts.
 - (b) Discriminator output is 1. The trigger is not fired immediately because of the PREMATURE_TRIGGER suppression.
 - (c) First trigger fires after 12.5 ns, at zero crossing of the sine wave. The fast SCA banks are stopped. CA=CB=CC=CD=0000111111(63), because $200\text{ps} \times 63 = 12.6 \text{ ns}$.
 - (d) The slow SCA bank keeps running for an additional 179.2 ns, where it raises STOP_REQUEST.
 - (e) STOP_REQUEST of all channels are ORed to Trig Out of the chip.
17. The FPGA sees the Trig Out and raises Ext Trigger to the chip. This takes a few ns.
18. (The slow SCA bank is stopped. CE = 1111000100(964), assuming the previous step took 1 ns.)
19. Write SPI: Instruction to READOUT.
20. Feed in Readout CLK (e.g., 40MHz) for 1280 cycles. Feed the same clock to external ADCs (AD9228). Read out from external ADCs at 12 times the clock (in 12-bit mode, 480MHz). This takes 32 μs at a 40MHz ADC rate.
21. In the meanwhile, Read SPI: Register 4-59. This takes 11.2 μs at a 40MHz SPI clock.
22. Readout order: (FSCA 63P3, 61P3, ..., 1P3, 2P3, 4P3, ..., 64P3) (FSCA 63P2, 61P2, ..., 1P2, 2P2, 4P2, ..., 64P2) (FSCA 63P1, 61P1, ..., 1P1, 2P1, 4P1, ..., 64P1) (FSCA 63P0, 61P0, ..., 1P0, 2P0, 4P0, ..., 64P0). P means phase. The order of phase is determined by process variation.
23. Determine the time between FSCA samples of the same phase using the ellipse fitting method. We need that information to determine the phase in step 22.
24. Determine the exact phase between P0, P1, P2, and P3 using the ellipse fitting method on the sine data recorded in Fast SCA banks.
25. Determine the exact amplitude of the sine wave in P0, P1, P2, and P3. It may differ because of the source follower mismatch.
26. Determine the time between SSCA samples using the ellipse fitting method.
27. ???

3.3 PID setup

ch 0: WR sin wave (250MHz) ch 1-7: LAPPD pulse

Trigger Channel Mask: 01111111 Mode: 01 (Capture 2 edges) Polarity: 11111111 (Trigger on falling edge) VCO Band: 00111111 PLL Ratio: 128 Slow mode: No

ch 8: WR sin wave (250MHz) ch 9-15: LAPPD pulse

Trigger Channel Mask: 01111111 Mode: 01 (Capture 2 edges) Polarity: 11111111 (Trigger on falling edge) VCO Band: 00011100 PLL Ratio: 128 Slow mode: No

Procedure:

1. Set Disc. Vth to 700mV.
2. Set Input Buffer Vbias.
3. Set Output Buffer Vbias1, Vbias2.
4. Set Reset High.
5. Set Reset Low.
6. Write SPI: VCO Digital Band to 00011100.
7. Lock the PLL by tuning the VCO ctrl voltage.
8. (Only necessary with on-chip PLL) Read SPI: PLL locked.
9. Write SPI: Slow mode to 0.
10. Connect Signal of LAPPD1 to ch 0-7, LAPPD2 to ch 8-15, DC level = 700mV, Amplitude = 200mV.
11. Write SPI: Trigger Channel Mask to 01111111.
12. Write SPI: Mode to 00000010.
13. Write SPI: Disc Polarity to 11111111.
14. Turn the LAPPD HV on.
15. Write SPI: Instruction to START.
 - (a) (Examine one channel.)
 - (b) (Assume that we are at the top of the sine wave when the sampling starts.)
 - (c) (Discriminator output is 1. The trigger is not fired immediately because of the PREMATURE_TRIGGER suppression.)
 - (d) (First trigger fires after 12.5 ns, at zero crossing of the sine wave. The fast SCA banks are stopped. CA=CB=CC=CD=0000111111 (63), because $200\text{ps} \times 63 = 12.6\text{ ns}$.)

- (e) (The slow SCA bank keeps running for an additional 179.2 ns, where it raises STOP_REQUEST.)
 - (f) ((STOP_REQUEST & TRIG_CHANNEL_MASK) of all channels are ORed to Trig Out of the chip.)
16. The FPGA sees the Trig Out and raises Ext Trigger to the chip. This takes a few ns.
 17. (The slow SCA bank is stopped. CE = 1111000100 (964), assuming the previous step took 1 ns.)
 18. Write SPI: Instruction to READOUT.
 19. Feed in Readout CLK (e.g., 40MHz) for 1280 cycles. Feed the same clock to external ADCs (AD9228). Read out from external ADCs at 12 times the clock (in 12-bit mode, 480MHz). This takes 32 μ s at a 40MHz ADC rate.
 20. In the meanwhile, Read SPI: Register 4-59. This takes 11.2 μ s at a 40MHz SPI clock.
 21. Readout order: (FSCA 63P3, 61P3, ..., 1P3, 2P3, 4P3, ..., 64P3) (FSCA 63P2, 61P2, ..., 1P2, 2P2, 4P2, ..., 64P2) (FSCA 63P1, 61P1, ..., 1P1, 2P1, 4P1, ..., 64P1) (FSCA 63P0, 61P0, ..., 1P0, 2P0, 4P0, ..., 64P0). P means phase. The order of phase is determined by process variation.
 22. Use the FSCA timebase and FSCA phase measurement, and counter A values to determine the position of the rising edge in terms of 5GHz clock cycles. sigfig = 6 so that dt \approx 1ps is achieved.
 23. Similarly, use counter C values to determine the position of the other rising edge.
 24. Use the channel 0 SSCA timebase to determine the phase between the sine wave and the 5GHz clock.