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Argonne National Lab

Picosecond Time-of-Flight System Clock Distribution Subsystem

-- PRELIMINARY --

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REVISION HISTORY

- 1) Version 0.1, initial draft of document, 5 August 2007.
- 2) Version 0.2, issued 9 August 2007.
 - a) Replaced Figure 3 sketch with better, to-scale version showing both DAQ and Analog boards.
 - b) Modified clock chip discussion to include new information provided by Jean-Francois.
 - c) Added new clock chip information about TI CDCE62005.
- 3) Version 1.0, issued 16 August, 2007.
 - a) First “real” version after review and input from rest of group.
 - b) Fixed title page to correctly show all authors and institutions involved in this effort.
 - c) Revised System Introduction paragraphs per notes from H. Frisch.
 - d) Updated Figure 1 to clarify and add missing high voltage lines.
 - e) Corrected “link” terminology, explicitly defined each link in system diagram.
 - f) Added short textual description of each link, named each link.
 - g) Added requested table defining each signal in each link, including estimated connector counts.
 - h) Stripped out technical details with formal language from section 2. Created new section 4 to hold technical detail information until such data is moved from this document into separate engineering documents specific to each link or module.
 - i) Added LVDS implementation picture to complement those of LVPECL and CML already in document.
 - j) Added additional introductory information describing the overall functions of the Modules, including information about the Time Stretcher chip, in addition to that of the Links.

1. GENERAL INFORMATION

This document describes the Clock Distribution sub-system of the Picosecond Time-of-Flight system. The Clock Distribution sub-system encompasses the receipt of the system clock from a source external to Time-of-Flight system, through the generation of the Acquire Clock that is provided to the Time Stretcher chips.

1.1 System Introduction

The Picosecond Time-of-Flight electronics system consists of a custom ASIC and several commercial chips integrated with a micro-channel plate (MCP) photo-detector that is designed to measure the arrival time of charged particles with a design goal of one picosecond resolution. Effectively, the system acts as a "digital phototube"; all analog signal processing is performed directly by the circuits mounted on the MCP such that the only interfaces that connect to external data collection systems are digital control, digital data output and power supplies. The Picosecond Time-of-Flight system consists of a series of Modules which are connected by Links, where by the term Link we mean all of the interconnecting signals between two Modules. Figure 1 gives the overall system picture.

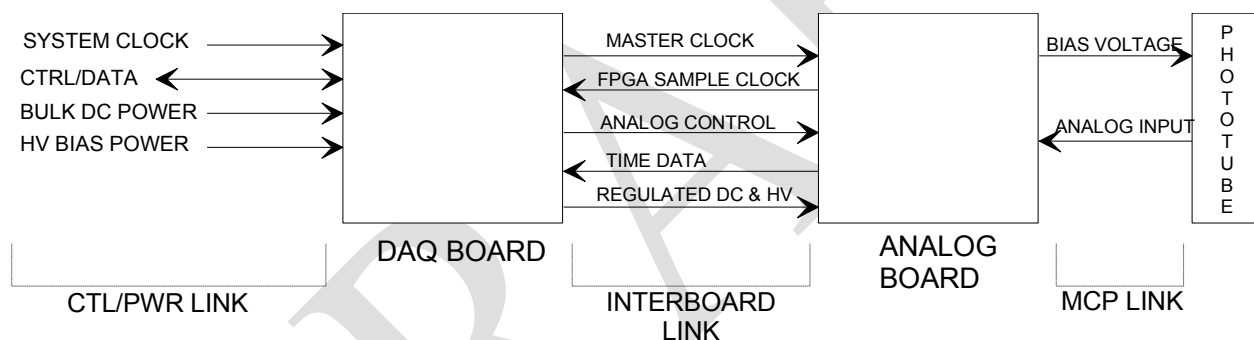


Figure 1 - Overall System Picture

1.1.1 Description of Modules in the System

The DAQ board holds interface chips, power supply regulators and an FPGA. Its purpose is to provide interface to the rest of the data acquisition system and provide infrastructure support to the Analog board. The Analog board connects directly to the MCP phototube. The Analog Board takes the Master Clock and uses a commercial clock distribution chip to create a 1GHz Acquire Clock. It contains a set of "Time Stretcher" chips that receive the fast signals from the anodes of the MCP tube. The Time Stretcher chips create Time Data pulses whose width is proportionate (200:1) to the delay between the arrival of the signal from the MCP and the next (or 2nd next) edge of the Acquire Clock by means of an internal PLL and counter running at 5GHz. This is the "common stop" mode of time digitization. The FPGA on the DAQ board measures the width of these pulses and provides digital data readout of the pulse width upon demand.

1.1.2 Description of Communications Links in the System

The CTL/PWR Link is the interface between the DAQ board and the rest of the experiment electronics. Bulk DC power is input to the DAQ board, where it is regulated for

local use and re-distributed to the Analog Board. High voltage bias for the MCP is provided external to the DAQ board and is routed through the two boards to the MCP without being used on either board. The System Clock is the main clock that is distributed to all picosecond time-of-flight systems, and is the source of all other clocks within this system. The Ctrl/Data signal(s) provide the method by which the experiment controls the Time-of-Flight system and obtains the data transmitted by the DAQ board.

The Interboard Link is a set of mated connectors between the DAQ board and the Analog board. The DAQ board generates the Master Clock from the System Clock, passes regulated DC and high voltage power to the Analog board, and generates any control signals needed by chips on the Analog board. In return, the Analog board generates an FPGA reference clock from the Master Clock and sends varying-width Time Data pulses to the FPGA on the DAQ board.

The Analog board mounts directly upon the MCP tube. The anodes of the tube provide analog signal input to the Analog board, and the tube's high voltage bias is provided by contacts of the Analog board.

1.1.3 Tabular Description of all signals in each Link

The following tables enumerate the conductor counts and signal levels for all the defined signals in each Link. Specific description of the implementation of each Link (e.g. part numbers, connector types, wire gauges, shielding, etc.) are not listed here but are found in separate documentation specific to each Link.

<i>Signal Name</i>	<i>Number of Conductors</i>	<i>Signal Levels</i>	<i>Notes, Special Considerations and/or Protocols</i>
System Clock	2	LVDS	Frequency must be integer divisor of 1GHz; 62.5MHz assumed for tests.
CTRL/DATA	6	LVDS	Pair 1: control data into FPGA Pair 2: readout enable in Pair 3: readout data Control & data are serial.
Bulk DC Power	4	+3.3V and GND	All other voltages in the system are regulated from the bulk +3.3V power.
HV Bias Power	2	3kV and GND	Subminiature connector type may be required due to board size. HV GND is routed separately from return planes of DAQ and Analog boards, but is tied to LV GND at MCP tube.

Table 1 - Enumeration of signals within the CTL/PWR Link

Signal Name	Number of Conductors	Signal Levels	Notes, Special Considerations and/or Protocols
	<i>The total number of conductors in the Interboard Link is determined by the number of pins in the connectors between boards. The counts below are based upon the use of four connectors of 16 pins (total = 64 conductors). Because of arcing concerns, the HV Bias Power is assumed to be carried on a unique fifth connector.</i>		
Master Clock	2	LVDS	Frequency is the same as System Clock in CTL/PWR link.
FPGA Sample Clock	2	3.3V LVPECL	
Analog Control	16	+3.3V and GND	Four status/control pins for the clock chip, four serial bus pins to control the clock chip, eight spares.
HV Bias Power	2	3kV and GND	
Time Data	8 (4 pairs)	LVPECL (2.5V? 1.8V?)	One pair for each of four Time Stretcher chips on the Analog board.
Regulated DC	36	+3.3V, +2.5V/+1.8V	Two power, four return for each of the four Time Stretcher chips. Four power + 8 return for the clock chip.

Table 2 - Enumeration of signals within the Interboard Link

Signal Name	Number of Conductors	Signal Levels	Notes, Special Considerations and/or Protocols
	<i>Conductor counts are subject to change as the development of the Analog Board progresses. The MCP Link is implemented using a special compression connector (elastomer).</i>		
Bias Voltage	2	3kV and GND	
Analog Input	16 + 4	Tiny analog	Conductor count based on 64-channel MCP tube with anodes shorted together in groups of four. Analog input returns (4) are assumed to be grouped one per Time Stretcher chip.

Table 3 - Enumeration of signals within the MCP Link

1.2 Distribution of System Clock and derivatives

The System Clock is received by a differential receiver on the DAQ Board. Within the DAQ Board the received clock is connected to an FPGA. Inside the FPGA a delay-locked-loop circuit (DLL) will repeat the System Clock within the FPGA for use as a control/data bus clock. The output of the DLL will also be driven differentially to the Analog Board. This copy of the 62.5MHz clock (the **Master Clock**) is received by a phase-locked-loop (PLL) on the Analog Board. The PLL multiplies the Master Clock frequency by a factor of 16 to create a local 1GHz **Acquire Clock** that is distributed to each of four Time Stretcher chips, as shown in Figure 2.

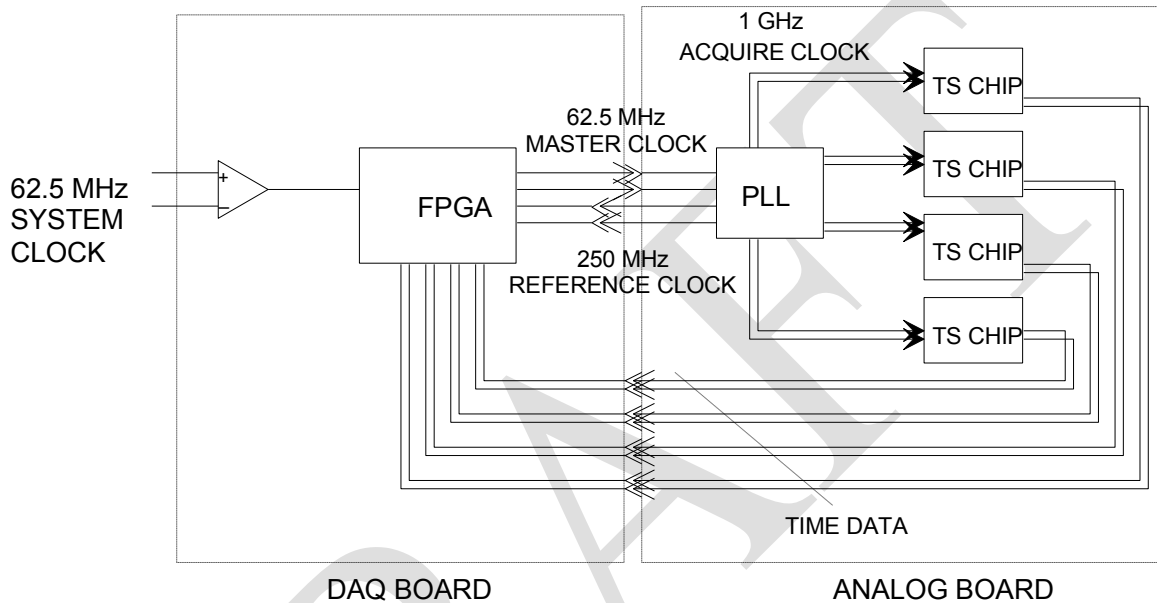


Figure 2 - Detail of clock distribution

Other input frequencies could be used but practically, the input must be an integer divisor of 1GHz. 62.5MHz is used here as an example. The Time Stretcher chips use the 1GHz clock to sample the **Analog Input**, creating the **Time Data** signals that are fed back to the FPGA on the DAQ board.

1.2.1 Master Clock Details

The Master Clock is simply a copy of the System Clock, passed through the FPGA on the DAQ board for jitter reduction using internal resources of the FPGA.

1.2.2 Acquire Clock Details

As the purpose of the system is to measure signals with picosecond timing accuracy, minimization of skew between the multiple copies of the Acquire Clock is critical. Similarly, the Acquire Clock must be delivered with minimal jitter. To achieve this, the PLL is located on the Analog Board to be as close to the time stretcher chips as possible with no intervening connectors that can introduce line discontinuities.

1.2.3 FPGA Reference Clock Details

The FPGA must perform the time-to-digital conversion of the output pulse from the Time Stretcher chips. It makes sense to provide another clock from the PLL to the FPGA that is phase- and frequency-locked to the 1GHz Acquire Clock. While it is possible to run small bits of logic within the FPGA at rates up to 450 MHz, bandwidth limitations on the clock input pins limit the external clock to lesser frequencies. Interconnection delay and input buffer delay will result in some phase shift but it should be relatively static. An alternative would be to use a PLL within the FPGA to generate its own 250MHz clock, but this generates the risk that the phase differential between the FPGA's PLL output and the Acquire Clock may wander over time or be different each time the system is power cycled.

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2. CLOCK SUBSYSTEM THEORY OF OPERATION

The System clock is presumed to come from an external source that provides a large number of delay-matched copies of this signal from a central source. In usual installations many copies of this timing unit are expected to be installed; it is conceivable that the System Clock may be daisy-chained or used in a multi-drop connection, but both of these methods carry considerable risk of increased jitter and noise.

2.1 Power Up & Initialization

The Time-of-Flight system, upon power up or reset, waits for the System Clock to be present before sending the Master Clock to the PLL on the Analog Board. During this time the Acquire Clock will either not be running, or more likely, running at a frequency far lower than the normal speed of 1GHz. The Time Stretcher chips will have to be designed in such a way that lack of clock or one that is far out of range (too low) will not have deleterious effects upon power consumption or recovery to normal operation when the clock is available. As much as possible, the FPGA will try to hold the Analog Board's PLL in a known state until the System Clock is available.

2.1.1 Backup Clock

It may be advisable to consider inclusion of a backup clock source for the FPGA on the DAQ Board to insure that command and control features are still active and functional even in the absence of a System Clock.

2.2 FPGA action upon System Clock

The FPGA will receive the System Clock and use it to drive an internal Delay-locked loop (DLL) or, if available, an internal Phase-locked loop (PLL). The purpose of the DLL (PLL) is to reduce jitter and to provide an internal fan-out of the clock so that it may be used by the FPGA directly. The buffered copy of System Clock, named Master Clock, is transmitted to the PLL on the Analog Board as part of the Interboard Link.

2.3 PLL Action upon Master Clock

The PLL will receive the Master Clock and create from it four identical Acquire Clocks, routed individually to the four time stretcher chips. The Acquire Clocks will be at a frequency 16 times that of the Master Clock (for Master Clock = 62.5MHz, Acquire Clock = 1.0GHz). A fifth output, the Reference Clock, will be created that is at a frequency four times that of the Master Clock (for Master Clock = 62.5 MHz, Reference Clock = 250MHz).

2.3.1 Control of PLL circuit

The PLL circuit is controlled using a two-wire (I₂C) or three-wire (SPI) interface driven by the FPGA on the DAQ board, plus whatever specific control lines are additionally required. The frequency multiplication ratios for both the Acquire clock and the Reference Clock should be programmable to allow for different System Clock frequencies.

2.4 Commercial clock chip compatibility with Acquire/Reference clock specifications

The Analog Devices AD9516-3 will accept an LVDS input and will provide six LVPECL outputs at 1GHz. Jitter is specified to be in the 400-500fs range. Four of the outputs could be used to drive the Time Stretcher chips and one for the FPGA. This part is relatively large. It is packaged in a 64-pin (9mm X 9mm) package.

Another option is the TI CDCE62005. This chip accepts an LVDS input and provides five LVPECL outputs in a 48-pin quad flat package. This is a new chip still in development, but TI has offered engineering samples. The preliminary documentation states that the outputs will work at 1GHz and that the jitter is less than 1ps RMS.

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3. General notes on high speed transmission lines

The clock connections of this system are all high speed transmission lines. Very careful attention to high speed signaling concerns is paramount. This section will provide some basic information to assist designers and users in coping with these concerns.

3.1 LVDS signal levels

LVDS circuit architecture uses current steering to create 1s and 0s by driving a current one way or the other in a pair of conductors, developing voltage across a terminating resistor at the end of the line. The standard has been extended to use in bussed applications, but it was originally designed for, and it still best used in, point-to-point applications.

In normal usage the transmission line is chosen to have an odd-mode characteristic impedance of 100 ohms, and a 100 ohm resistor is used across the conductor pair as the terminator. With typical LVDS currents (5mA), this generates a differential voltage of about 500 millivolts at the input of the receiver. LVDS, unlike other similar high-speed standards, has been codified as an EIA standard (EIA 644). The most common reference to LVDS is the LVDS User's Guide published by National Semiconductor (found at <http://www.national.com/appinfo/lvds/files/ownersmanual.pdf>)

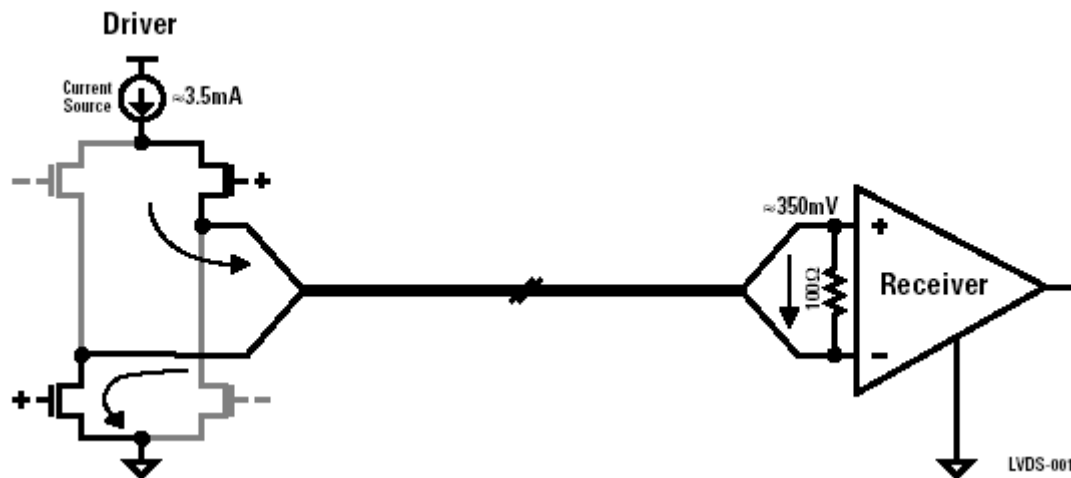


Figure 3 – Typical LVDS implementation

3.2 LVPECL

LVPECL is based on PECL, which is based upon yet older ECL. All “xxECL” interfaces use emitter-follower structures on the output that require pulldown resistors to a voltage appropriate to bias the output structure (and, if well designed, also terminate the line in its characteristic impedance). Generation of the termination voltage can present additional infrastructure requirements. PECL, or Positive ECL, is designed to run from a positive voltage rail and be terminated to the return; this is the opposite of ECL that uses negative voltage. LVPECL uses smaller current swings than PECL, but there is no codified standard.

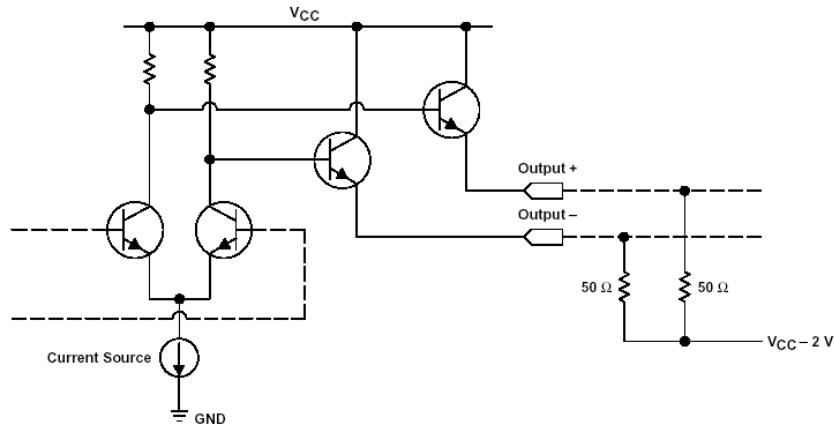


Figure 4 - typical PECL implementation

When implementing an LVPECL circuit, use of the correct termination (or pulldown) voltage and resistance is important to minimize noise in the power supplies and the return plane(s). Additionally, it is sometimes necessary to use resistors in series if the V_{cc} of the transmitter is larger than the V_{cc} of the receiver. For periodic clocks with constant duty cycle, it is often permissible to put the pull-down resistors at the transmitter and AC-couple the differential voltage to the receiver, using a parallel termination of the receiver at the receiver end. This allows the receiver to bias its inputs at whatever voltage is convenient.

3.3 CML

CML, or “current mode logic”, uses a very simple output stage consisting of the uncommitted tails of a simple differential pair of transistors. As such it requires external resistors to bias the circuit and provide termination, just like all ECL derivatives. The pullup resistors must bias the output stage to the common-mode voltage of the receiver.

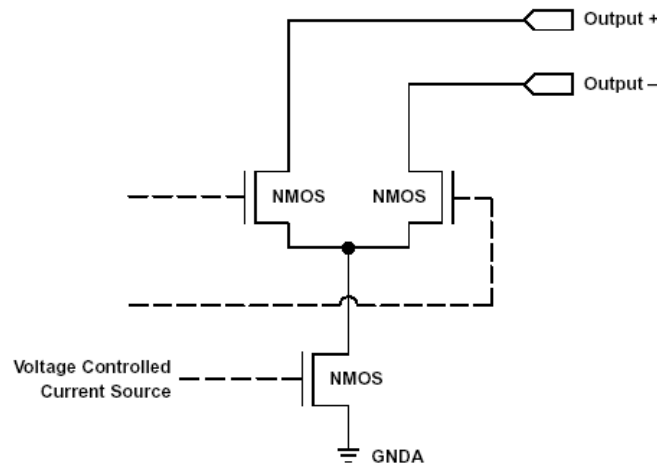


Figure 5 - typical CML implementation

3.4 Printed Circuit Board layout considerations

The high speed of the system requires that differential traces on printed circuit boards be very well matched. Vias and package pins have to be viewed as potentially self-resonant

circuits. Even the mismatch in the length of right-angle connector pins becomes a concern; this means that if the 'blue' conductor of a twisted pair in board 'a' has the longer connector pin path, the *other board at the other end of the line* has to be designed such that the 'red' conductor of the twisted pair gets the longer path. Boards cannot be developed in isolation – the designers at both ends of the interconnect must work together. A useful general reference for interfacing the various signal levels is <http://focus.ti.com/lit/an/slla120/slla120.pdf>. If a copy of the MECL System Design Guide from Motorola can be found, it is also a good reference work, especially chapter 7.

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4. Technical Details

This section is a placeholder for the technical details until they are broken out into their own documents. The expectation is that the engineering implementation of each Link and Module will generate documents specific to each. As is typical with engineering documentation, the language herein is more formal.

4.1 CTL/PWR Link Technical Details

4.1.1 System Clock

- The System Clock shall be delivered at a frequency of 62.50 MHz over a shielded twisted pair with odd-mode characteristic impedance of 100 ohms.
- The System Clock shall conform to all electrical characteristics of the LVDS standard.
- The DAQ board shall provide a termination consisting of two 51 ohm resistors in series placed from one conductor to the other of the differential pair. A small capacitor (10pF) shall connect from the center point of the two resistors to a connection point that can be tied to the shield of the twisted pair delivering the System Clock to the DAQ board.
- It is expected that the shield of the twisted pair delivering the System Clock is grounded at the transmitter end. The DAQ Board shall not normally connect the shield of the twisted pair to anything other than the common-mode return capacitor detailed above, but provision *may* be made to connect that node to the main return plane of the DAQ board through a zero-ohm resistor.
- To protect the inputs of the FPGA of the DAQ board, a discrete LVDS receiver IC shall be used to receive the System Clock. A differential-in, differential-out buffer is preferred to minimize clock jitter.

4.2 InterBoard Link Technical Details

4.2.1 Master Clock Physical Specifications

- The Master Clock shall conform to all electrical characteristics of the LVDS standard. The Master Clock shall always be the same electrical signal levels as the System Clock to provide for simpler testing of Analog and DAQ boards as separate entities.
- The Master Clock shall be routed on the DAQ board and on the Analog board as an edge-coupled stripline with characteristic impedance (odd-mode) of 100 ohms.
- Connection of the Master Clock from the DAQ board to the analog board shall be made using two adjacent pins of a 1mm X 1mm pin & socket connector, shielded on either side by a pin & socket connected to the power supply return of the PLL.
 - It is expected that there will be four unique connectors between the DAQ board and the Analog board (one for each TS chip). Each of these four connectors will have a few pins allocated to the PLL. One of the four

connectors will carry the Master Clock. The other three connectors will be used for control of the PLL and for the Reference Clock.

- The Analog board shall provide a termination consisting of a single 100 ohm resistor placed from one conductor to the other of the differential pair.

4.2.2 Mechanical details of Interboard Link

Figure 3 shows a sketch of how the four connectors might be arrayed on the Analog board using 64-pin QFPs. The mating connectors would be placed on the solder (bottom) side of the DAQ board. For comparison a top-side sketch of the DAQ board is also provided.

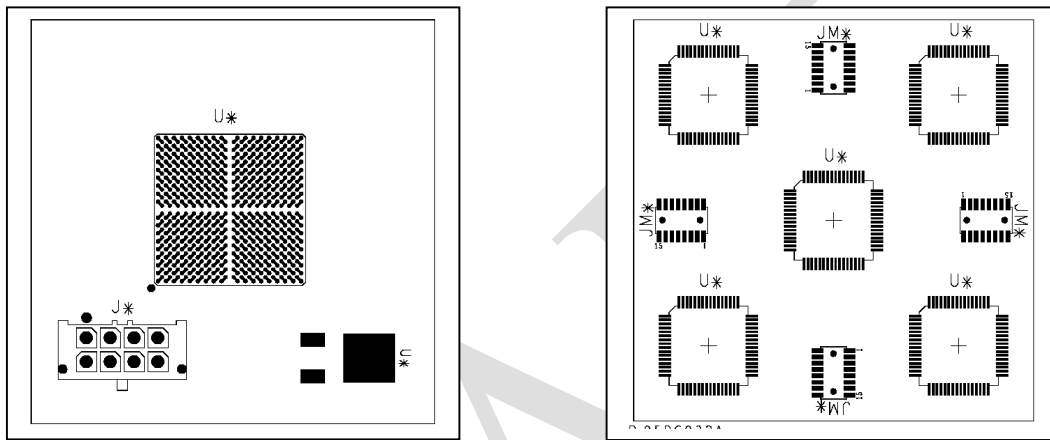


Figure 6 – Concept sketches of DAQ and Analog Boards

4.2.3 Proposed Pin-Out of Interboard Link Connectors

There are four surface-mount connectors used to implement all of the Interboard Link save for the high voltage connection. Each of these connectors is a sixteen-pin, 1mm pitch, dual-row connector. Each connector is subdivided into three sections:

- A set of pins assigned to the Time Stretcher portion of the interface
- A pair of reserved pins (spares)
- A set of pins assigned to the Clock Chip in the center of the Analog board.

The functions of the pins assigned to the Time Stretcher chips are the same in all four connectors. The functions of the pins assigned to the Clock Chip vary with position to allow for all the control signals required. The definitions herein are based upon use of the AD9516-3 clock chip, but should not significantly vary should some other part be used.

Connector A	Connector B	Connector C	Connector D
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Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	TS Power	1	TS Power	1	TS Power	1	TS Power
2	TS PwrReturn	2	TS PwrReturn	2	TS PwrReturn	2	TS PwrReturn
3	TS PwrReturn	3	TS PwrReturn	3	TS PwrReturn	3	TS PwrReturn
4	Time Data +	4	Time Data +	4	Time Data +	4	Time Data +
5	TS PwrReturn	5	TS PwrReturn	5	TS PwrReturn	5	TS PwrReturn
6	Time Data -	6	Time Data -	6	Time Data -	6	Time Data -
7	TS Power	7	TS Power	7	TS Power	7	TS Power
8	TS PwrReturn	8	TS PwrReturn	8	TS PwrReturn	8	TS PwrReturn
9	RESERVED	9	RESERVED	9	RESERVED	9	RESERVED
10	RESERVED	10	RESERVED	10	RESERVED	10	RESERVED
11	Clock PwrReturn	11	Clock PwrReturn	11	Clock PwrReturn	11	Clock PwrReturn
12	Clock PwrReturn	12	Clock PwrReturn	12	Clock PwrReturn	12	Clock PwrReturn
13	Clock LD	13	Clock Status	13	Clock Sync	13	Clock Reset*
14	Clock Power	14	Clock Power	14	Clock Power	14	Clock Power
15	Master Clock +	15	FPGA Reference Clock +	15	Clock CS*	15	Clock SCLK
16	Master Clock -	16	FPGA Reference Clock -	16	Clock SDI	16	Clock SDO

Table 4 - Pin out of Interboard Link Connectors

4.2.4 FPGA Reference Clock Physical Specifications

- The FPGA Reference Clock shall be implemented as either an LVPECL or LVDS interface.
- The Reference Clock shall be routed on the DAQ board and on the Analog board as an edge-coupled stripline with characteristic impedance (odd-mode) of 100 ohms. If LVPECL signals are used, each line shall, viewed singly, have an impedance of 50 ohms to return.
- The Reference clock is a point-to-point connection driven from the PLL of the Analog board to the FPGA of the DAQ board.

- Connection of the Reference Clock from the Analog board to the DAQ board shall be made using two adjacent pins of a 1mm X 1mm pin & socket connector. These two pins shall be similarly implemented to that of the Master Clock.
- The DAQ board shall provide termination appropriate to the signal standard implemented for the Reference Clock.

4.3 Acquire Clock Physical Specification (signal within Analog Board, to be incorporated into the Analog Board module specification)

- The Acquire Clock shall be implemented as an LVPECL interface using signal swings compatible with the power supply rails of the Time Stretcher chips.
- The four copies of the Acquire Clock shall be routed on the Analog board as edge-coupled striplines with characteristic impedance (odd-mode) of 100 ohms. Each line shall, viewed singly, have an impedance of 50 ohms to return.
- Each single copy of the Acquire clock is a point-to-point connection driven from the PLL to one Time Stretcher chip on the Analog board.
- All four copies of the Acquire Clock shall be routed with equivalent electrical length transmission lines, with all lines having the same number of bends. No vias should be used in the routing of the Acquire clock.
- The Time Stretcher chip shall provide termination appropriate to the signal standard implemented for the Acquire Clock.