Sampling front-ends Chips for Pico-second Timing with Micro-Channel Plate devices

Jean-Francois Genat

University of Chicago

Research Techniques Seminar
Fermilab, Dec. 15th 2009
With help from


and many others...
Introduction

**Micro-Channel Plates**

The fastest devices to date

**timing in the pico-second range**

**Deep sub-micron CMOS technologies**

Pulse sampling at 1-10 GHz

**large front-end at affordable power, room and cost**

- Micro-channel Plate signals
- Associated signal processing for pico-second timing
- A 130nm CMOS sampling-digitizing ASIC
Outline

• Applications of Pico-second Timing
• Micro-Channel Plate devices
• Pico-second electronics and Waveform analysis
• Sampling Electronics
• Pico-second timing SCA in 130nm CMOS technology
• Perspective
10-100 Picosecond Time of Flight applications at HEP Colliders

Particle identification

1-100ps Time of Flight

Henry Frisch

Time-of-Flight Difference in Psec (L=1.5m)

Delta - t (psec)

Delta_{e\pi}, Delta_{\pi K}, Delta_{p K}

3Delta_{e\pi}, 3Delta_{\pi K}, 3Delta_{p K}

Particle Momentum (GeV)

Henry Frisch

Jean-Francois Genat, Fermilab December 15th 2009
Particle ID from Waveform analysis

Response to Pions

Data from the Hadron Tile Calorimeter at LHC-ATLAS

Pion signals have shorter lifetime: shorter signals and faster rise-time

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Lepton Flavor Physics

Example: Deep Underground Science and Engineering Laboratory (DUSEL) detector

Double $\beta$ decay, Solar neutrinos, Gravitational waves

100% coverage and 3D photon vertex reconstruction.

Need for >10,000 square meters at 100 ps resolution
100ps Time of Flight:

Positron Emission Tomography [4]

\[ \Delta x = c \Delta t/2 \]
\[ \Delta t = 50\text{ps}, \Delta x = 7.5\text{mm} \]
A possible TOF PET detector

Micro-Channel Micro-PET (MCMP)

N.B.: NOT TO SCALE

Individual Crystals

Sample

Micro-Channel Plate panels

Transmission Line Anode (2mm pitch: 1 H and 1 V)

Photocathodes

Sampling Electronics

Henry Frisch
Outline

• Applications of Pico-second Timing
• **Micro-Channel Plate devices**
• Pico-second electronics and Waveform analysis
• Sampling Electronics
• Pico-second timing SCA in 130nm CMOS technology
• Perspective
## Timing-imaging Devices

### Multi-anodes PMTs
- **Dynodes**

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Quantum Eff.</td>
<td>30%</td>
</tr>
<tr>
<td>Collection Eff.</td>
<td>90%</td>
</tr>
<tr>
<td>Rise-time</td>
<td>0.5-1ns</td>
</tr>
<tr>
<td>Timing resolution (1PE)</td>
<td>150ps</td>
</tr>
<tr>
<td>Pixel size</td>
<td>2x2mm²</td>
</tr>
<tr>
<td>Dark counts</td>
<td>1-10Hz</td>
</tr>
<tr>
<td>Dead time</td>
<td>5ns</td>
</tr>
<tr>
<td>Magnetic field</td>
<td>no</td>
</tr>
<tr>
<td>Radiation hardness</td>
<td>no</td>
</tr>
</tbody>
</table>

### Silicon-PMTs [10]
- **Quenched Geiger in Silicon**

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Quantum Eff.</td>
<td>90%</td>
</tr>
<tr>
<td>Collection Eff.</td>
<td>70%</td>
</tr>
<tr>
<td>Rise-time</td>
<td>250ps</td>
</tr>
<tr>
<td>Timing resolution (1PE)</td>
<td>100ps</td>
</tr>
<tr>
<td>Pixel size</td>
<td>50x50µm²</td>
</tr>
<tr>
<td>Dark counts</td>
<td>1-10MHz/pixel</td>
</tr>
<tr>
<td>Dead time</td>
<td>100-500ns</td>
</tr>
<tr>
<td>Magnetic field</td>
<td>yes</td>
</tr>
<tr>
<td>Radiation hardness</td>
<td>1kRad=noisex10</td>
</tr>
</tbody>
</table>

### Micro-Channel Plates [1]
- **Micro-Pores**

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Quantum Eff.</td>
<td>30%</td>
</tr>
<tr>
<td>Collection Eff.</td>
<td>70%</td>
</tr>
<tr>
<td>Rise-time</td>
<td>50-500ps</td>
</tr>
<tr>
<td>Timing resolution (1PE)</td>
<td>20-30ps</td>
</tr>
<tr>
<td>Pixel size</td>
<td>1.5x1.5mm²</td>
</tr>
<tr>
<td>Dark counts</td>
<td>1Hz-1 kHz/cm²</td>
</tr>
<tr>
<td>Dead time</td>
<td>1µs</td>
</tr>
<tr>
<td>Magnetic field</td>
<td>15kG</td>
</tr>
<tr>
<td>Radiation hardness</td>
<td>good (a-Si, Al₂O₃)</td>
</tr>
</tbody>
</table>

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Timing Resolution: Single Photo-electron Time Transit Spread:

$$\sigma^2_t = \sigma^2_{1st\text{ gap}} + \sigma^2_{pore} + \sigma^2_{2nd\text{ gap}}$$

The thinner the device, the better the Timing Resolution.

Jean-Francois Genat, Fermilab December 15th 2009
MCP Device Simulations: first gap

Monte-Carlo: $10^6$ single photoelectrons events
Simulation of the first gap: photocathode - pores input
Angular distribution: $\text{asin} \{ \text{rand}[-1,1] \}$

Gap 2 mm

RMS: 5.05228 ps

5ps contribution to TTS
(20-30ps total measured)

Lionel de Sa

Full device simulations:
Valentin Ivanov
Zeke Insepov
Two-micron space resolution using analog charge division technique

High precision analog measurements.

*But integration time = 200ns!*

---

Fig. 4. A profile along a line cut across the MCP pores of Fig. 3. The spatial resolution of the readout is ~2μm rms, capable of resolving every single MCP pore.
Micro-Channel Plate signals

Single Photon
16-averaged
Sampling: 18 GS/s
TTS= 10ps

From Photek

11 mm diameter Micro-Channel Plate signal
Signal full bandwidth: 10 GHz
Typical Timing resolution:
Single Photoelectron Time Transit Spread: 10ps

Data taken at Argonne

2” x 2” Micro-Channel Plate signal
Signal full bandwidth: 2 GHz

30ps
MCP Signal in the frequency domain

Fourier spectrum of a 2”x 2” MCP signal

\[ \sigma_t = \sigma_x \frac{dx(t)}{dt} \]

Noise as small as possible

Slope as steep as possible

2 GHz
Pico-second timing with delay lines: 2D position + time

- Delay lines readout and pulse sampling provide
  - Fast timing (2-10ps)
  - One dimension with delay lines readout 100mm-1mm
    Transverse dimension can be obtained from centroids

Less electronics channels for large area sensors

\[ \frac{1}{2} (t_1 + t_2) = \text{time} \]
\[ v(t_1 - t_2) = \text{longitudinal position} \]
\[ \Sigma \alpha_i a_i / \Sigma \alpha_i = \text{transverse position} \]
25 μm pore MCP signal at the output of a ceramic transmission line
Laser 408nm, 50Ω, no amplification
Delay Line readout  Position resolution

158 PEs

<table>
<thead>
<tr>
<th>HV</th>
<th>2.3 kV</th>
<th>2.4 kV</th>
<th>2.5 kV</th>
<th>2.6 kV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Std time diff</td>
<td>12.8 ps</td>
<td>2.8 ps</td>
<td>2.2 ps</td>
<td>1.95 ps</td>
</tr>
<tr>
<td>Std position</td>
<td>640 µm</td>
<td>140 µm</td>
<td>110 µm</td>
<td>97 µm</td>
</tr>
</tbody>
</table>

Oscilloscope TDS6154C Tektronix

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Delay Line readout  Position resolution

With Edward May and Eugene Yurtsev  (Argonne)
Delay Line readout  Position resolution

Best result at 158PEs

Position resolution (velocity=8.25ps/mm):
- 50PEs: 4.26ps, 213μm
- 158PEs: 1.95ps, 97μm
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Timing resolution [5]

\[ \sigma_t = \sigma_x \frac{dx(t)}{dt} \]

Time spread proportional to 1/rise-time and noise

Identical signals, noise added

Single Threshold
Timing techniques

**ANALOG**

Constant-fraction

Constant fraction

Leading edge

Leading edge errors

**DIGITAL**

Sample, digitize,

Fit to the known waveform

Pulse sampling and Waveform analysis

Multi-threshold

Extrapolated time
Constant fraction [6]

Measure pulse amplitude: threshold at a given fraction a delayed version of the pulse

3-parameter (at least !) technique

- Absolute Threshold
- Fraction threshold
- Delay

Analog delay difficult to integrate (cable in most implementations)

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Multi-threshold

Multi-threshold: sample several times over thresholds

Best results:

- Number of thresholds     4-8
- Thresholds values        equally spaced
- Order of the fit:        2d order optimum
Digital Waveform Analysis

Fit to waveform and derivative templates

Psec Timing and Charge
Methods compared (simulation) [11]

Time resolution vs Number of photo-electrons

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Picosecond Digital Electronics for Micro-Channel Plate Detectors

*Store the full detector information as with a digital oscilloscope:*

- Detector + electronics noise >> quantization noise (LSB/√12)
- Sampling frequency > 2 x full Analog Bandwidth (Shannon-Nyquist)

Ideal approach:

Digitize on the fly, if the two above conditions can be fulfilled. If not, loss of precision due to A/D conversion and/or loss of timing information.
Picosecond Digital Electronics for Micro-Channel Plate Detectors

A/D state of the art:

- 8-bit 1GS/s
- 10-bit 300 MS/s
- 16-bit 160 MS/s

Need at least 5 GS/s sampling rate, 10-12bit

There is no!

Fast analog storage

and slower digitization, if rate allows, or dead-time acceptable

Apply the best timing algorithm suited to the detector, get the charge for free ...!
Fast analog storage [7-9]

Example:

Analog
5 GS/s analog storage,
- Internal Analog buffer or
- Use other channels on-chip with a fast input multiplexer

ADC
8-ch 12-bit 80 MS/s (AD9222-80)
Ok up to 2% occupancy
Sampled Micro-Channel Plate signals

Assume: a typical noise at 1mV (detector+system)
LSB set to 1mV for a 1V dynamic range (quantization noise 300µV),
50-200ps rise-time

Fast timing:

10 bit, 2.5-10 GHz full analog bandwidth  > 5-20 GS/s sampling rate

Readout electronics

Deep sub-micron CMOS ASICs:

- ☺ faster: larger analog bandwidth, sampling rate
- ☺ improved radiation hardness
- ☻ cheap, 1-10$/ch
- ☹ less dynamic range

Jean-François Genat, Fermilab December 15th 2009
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Fast Sampling Electronics

- Integration in custom ASIC for large scale detectors $\sim 10^{4-6}$ channels,
- Self or external trigger,
- Low power,
- Full digital (serial) interface,
- High reliability and availability,
- Low cost.
## Sampling Chips

<table>
<thead>
<tr>
<th></th>
<th>Sampling GS/s</th>
<th>Bandwidth GHz</th>
<th>Dyn. range bits</th>
<th>Depth</th>
<th>PLL</th>
<th>ADC bits</th>
<th>Trigger</th>
<th>Techno</th>
</tr>
</thead>
<tbody>
<tr>
<td>G. Varner (Hawaii) [9]</td>
<td>6</td>
<td>1.0</td>
<td>10</td>
<td>1024</td>
<td>no</td>
<td>12</td>
<td>experience</td>
<td>.25µm</td>
</tr>
<tr>
<td>S. Ritt (PSI) [8]</td>
<td>6</td>
<td>.8</td>
<td>11.5</td>
<td>256</td>
<td>3.9ps</td>
<td>no</td>
<td>no</td>
<td>.25µm</td>
</tr>
<tr>
<td>D. Breton/E. Delagnes (Orsay/Saclay) [7]</td>
<td>2.5</td>
<td>.5</td>
<td>13.4</td>
<td>250</td>
<td>20ps</td>
<td>no</td>
<td>no</td>
<td>.35µm</td>
</tr>
</tbody>
</table>

**ASIC Deep Sub-Micron (< .13µm) CMOS processes allow today:**

Sampling: 10-20 GHz  
Bandwidth: > 1.5 GHz  
Dyn. Range: 10bit
### Sampling Chips Survey

<table>
<thead>
<tr>
<th>Feature</th>
<th>Hawaii</th>
<th>Varner</th>
<th>Saclay/Orsay</th>
<th>Delagnes/ Breton</th>
<th>PSI</th>
<th>S.Ritt</th>
<th>This proposal</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Blab1</td>
<td>Lab1-2</td>
<td>Lab 3</td>
<td>Hamac</td>
<td>Matacq</td>
<td>Sam</td>
<td>Planned</td>
</tr>
<tr>
<td>Bandwidth (3db)</td>
<td>300 MHz</td>
<td>900 MHz</td>
<td>50 MHz</td>
<td>200-300 MHz</td>
<td>300 MHz</td>
<td>650 MHz</td>
<td></td>
</tr>
<tr>
<td>Channels</td>
<td>1</td>
<td>8</td>
<td>9</td>
<td>8</td>
<td>1</td>
<td>2</td>
<td>12 6 2 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>8 4 2 1</td>
</tr>
<tr>
<td>Triggered mode</td>
<td>Yes</td>
<td></td>
<td>Yes</td>
<td>Common stop</td>
<td></td>
<td></td>
<td>Channel trigger</td>
</tr>
<tr>
<td>Resolution</td>
<td>10 bit</td>
<td></td>
<td>13.3 bit</td>
<td>13.4 bit</td>
<td>11.6 bit</td>
<td>11.6 bit</td>
<td>11.5 bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>8-10-bit</td>
</tr>
<tr>
<td>Samples</td>
<td>128 rows of 512</td>
<td>256</td>
<td>144</td>
<td>2520</td>
<td>256</td>
<td>2048</td>
<td>1024-12288</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1024-8192</td>
</tr>
<tr>
<td>Clock</td>
<td>33 MHz</td>
<td></td>
<td>40 MHz</td>
<td>100 MHz</td>
<td></td>
<td></td>
<td>fsamp/2048</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>20-40 MHz</td>
</tr>
<tr>
<td>Max latency</td>
<td>560 us</td>
<td>2.2ms</td>
<td>50us</td>
<td></td>
<td></td>
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<tr>
<td>Input Buffers</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
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<td>Differential inputs</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
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<tr>
<td>Input impedance</td>
<td>50 Ohms</td>
<td>50 Ohms</td>
<td>50 Ohms Ext</td>
<td>10 MOhm/3pF</td>
<td>50 Ohms</td>
<td></td>
<td></td>
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<tr>
<td>Readout clock</td>
<td>500 MHz</td>
<td></td>
<td>5 MHz</td>
<td>5 MHz</td>
<td>16 MHz</td>
<td></td>
<td></td>
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<td>Locked delays</td>
<td>Ext DAC</td>
<td></td>
<td>Ext DAC</td>
<td>Ext DAC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>On-chip ADC</td>
<td>12-b +500MHz TDC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R/W simultaneous</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Power/ch</td>
<td>15mW/1.6W</td>
<td></td>
<td>36 mW</td>
<td>250-500 mW</td>
<td>150 mW</td>
<td></td>
<td>2-8mW</td>
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<tr>
<td>Dynamic range</td>
<td>1mV/1V</td>
<td></td>
<td>0.26mV/2.75V</td>
<td>175 uV-2V</td>
<td>0.65mV-2 V</td>
<td></td>
<td>0.35mV/1.1V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>.35mV/1V</td>
</tr>
<tr>
<td>Xtalk</td>
<td>Inter-rows 0.1%</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1V</td>
</tr>
<tr>
<td></td>
<td>4.5ps</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>&lt; 0.5%</td>
</tr>
<tr>
<td>Sampling jitter</td>
<td>4.5ps</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>6ps</td>
</tr>
<tr>
<td>Power supplies</td>
<td>-tbd/+2.5V</td>
<td></td>
<td>-tbd/2.5V</td>
<td></td>
<td></td>
<td></td>
<td>2.5V</td>
</tr>
<tr>
<td>Process</td>
<td>TSMC 25</td>
<td></td>
<td>TSMC .25</td>
<td>TSMC .25</td>
<td>HP/DMILL .8</td>
<td>AMS .8</td>
<td>AMS .35</td>
</tr>
<tr>
<td>Chip area</td>
<td>5.25 mm²</td>
<td></td>
<td>10 mm²</td>
<td>2.5mm²</td>
<td>19.8mm²</td>
<td>30mm2</td>
<td>25mm²</td>
</tr>
<tr>
<td>Temp coeff</td>
<td>0.2%/-C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>5e-5/-C</td>
</tr>
<tr>
<td>Cost/channel</td>
<td>500$/40</td>
<td>10$/2k</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10-15$</td>
</tr>
</tbody>
</table>
Existing ASICs: Labrador 3 [9]

Gary Varner
U-Hawaii

250nm CMOS

CH1

CH2

6.4 ps RMS
(4.5ps single)
Waveform Digitizing Chip DRS4 [8]

- UMC 0.25 μm rad. hard
- 9 chn. each 1024 bins, cascadable up to 8192
- Sampling speed 0.2 ... 5 GS/s
- Bandwidth 950 MHz
- 17.5 mW/chn @ 2.5V
- On-chip PLL stabilization
- Readout speed using ext. ADC: 30 ns * n_{samples}
- SNR: 69 dB calibrated
- Aperture jitter: 4 ps at 5 GS/s calibrated

250nm CMOS
The SAM (Swift Analog Memory) ASIC [7]

D. Breton/E. Delagnes
Orsay/Saclay

- 2 differential channels
- 256 cells/channel
- BW > 450 MHz
- Sampling Freq 400MHz->3.2GHz
- High Readout Speed > 16 MHz
- Smart Read pointer
- Few external signals
- Many modes configurable by a serial link.
- Auto-configuration @ power on
- AMS 0.35 µm => low cost for medium size prod

6000 ASICs manufactured, tested and delivered in Q2 2007
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130nm CMOS Sampling ASIC

This chip is developed by U-Chicago and U-Hawaii

It includes

- 4 channels of full sampling (256 cells)
- 1 channel of sampling cell to observe the sampling window

Test structures:

- Sampling cell,
- ADC Comparator,
- Ring Oscillator
Sampling ASIC

- Prototype chip in 130nm CMOS technology (IBM 8RF-DM)
- 4-channel sampling, >10-15GSa/s
- 1-2 GHz analog bandwidth, 50 Ohms
- 40-80 MHz clock
- 256 cells (<100ps/cell, 12.5-25ns range)
- Free running delays (no PLL)
- Sampling window 500ps-2ns
- Dynamic range .7V
- Crosstalk <1%
- On-chip parallel 12-bit ADC (2 µs min conversion time)
- Free running delays (No PLL)
- Linearity < 1% on the full dynamic range
- Read clock up to 50 MHz (one cell/period, 22 µs total readout time)
- One reference channel (sampling window)
- 1.2V power supply
- Power < 40 mW/channel
- Process IBM 8RF-DM (130nm CMOS)

- 4 x 4 mm²

Chicago-Hawai’i

Sent July 2009, received Oct 21st
Sequence of operations

-1 **Write:** The timing generator runs continuously, outputs clock phases 100ps spaced. Each phase closes a write switch during one sampling window.

-2 **A/D conversion** after a trigger that opens all the write switches and starts all A/D conversions in parallel. Data available after 2 µs (2GHz counters)

-3 **Read** occurs after conversion (data can still be taken as in Phase 1)
Block diagram

Timing Generator

Channel # 0 (256 sampling caps + 12-b ADC)

Channel # 3

Channel #4 (Sampling window)

Digital out

Read control

Read

Clock

Ch 0

Ch 1

Ch 2

Ch 3

Analog in

Calibration

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10 GS/s Timing Generator

Delay control voltages

40 MHz clock

100ps step delays

256 cells

Sampling window control voltage

To switched capacitor array
Timing Generator
Voltage Controlled Delay Cell

- 256 voltage controlled delay cells of 100-200ps
- 20-40 MHz clock propagated

Voltage Controlled Delay Cell

Test structure:
Ring Oscillator: Two delay cells + inverter
Sampling Cell

Principle

“Write” state

3 dB analog bandwidth is \( \frac{1}{2\pi R_{in} C_{storage}} \)

“Sampling window”

Number of switches closed x sampling period

Thermal \( kT/C \) switching noise = 250\( \mu \)V = one 12-bit ADC count
Analog bandwidth and Sampling window

On chip:

\[ V_{in} \]
\[ R_{in} \]
\[ C_{store} \]

Sampling window = Number of switches closed at a time \times sampling period

\[
\text{Sampling Window}_{10^{-3}} = \log(10^{-3}) \times \text{rise-time} / 2.2 = 1/3 \text{ dB Analog Bandwidth}
\]

In practice, \( R_{in} \) and \( C_{store} \) are minimum, but limited by the stray capacitor of the switch, and the leakage current of the switch in the open state.

\[ R_{in} = 1.5k\Omega, \quad C_{store} = 70 \text{ fF} \]

3dB Analog Bandwidth = \( 2 \pi R_{in} C_{store} = 1.5 \text{ GHz} \)

Sampling window \( 10^{-3} > 625\text{ps} = 7 \text{ samples at 10 GS/s} \)

Off chip: Inductance of the wire bonds and pad capacitance: Bump-bonding

Gary Varner

Jean-Francois Genat, Fermilab December 15th 2009
Sampling cell design

Need a voltage buffer to read the small storage capacitor (70fF)

The gate of the source follower transistor is part of the storage capacitor (40+30fF)

\[ V_{out} = V_{in} - V_T - (V_{pol} - V_T) \sqrt{\frac{W}{L \cdot W_{pol}}} \]

Non-linearity < 8/1000
Sampling Capacitance 70fF
Switch resistance: 1.5kΩ
Analog bandwidth 1.5GHz
Wilkinson:

All cells digitized in one conversion cycle
- Ramp generator
- Comparators
- Counter
- Clocked by the ring oscillator at 1-2 GHz
One sampling cell

One channel

CMOS 130nm    IBM    4 x 4 mm²
Pictures

Received October 21\textsuperscript{st} 2009

Die to be bump-bonded on PCB
Tests

- First tests of packaged chips (presented here)
  - DC power vs biases,
  - Sampling cell response vs input
  - ADC’s comparator
  - Leakages (voltage droop)
  - Digital Readout

- Fine tests to come... (chip is just being bump-bonded to PCB)
  - Analog bandwidth
  - Resolution, signal-to-noise
  - Sampling cell response vs sampling window
  - Crosstalk
  - Max sampling rate
  - Full ADC
  - Linearities, dynamic range, readout speed
Tests: Sampling cell

Ok, except a saturation for voltage inputs > 750 mV
Very close to simulation
Tests: Sampling cell Leakages

1 - input LOW, write switch CLOSED
2 - input HI, switch CLOSED
3 - input HI, switch OPEN
4 - input LOW, switch OPEN

Leakage current is 7 pA
Much smaller than in simulation
Tests: Ring Oscillator

- Measured up to 1.5 GHz
- Observation limited by the 12 bit down-counter
- Can presumably run faster internally
Tests: Digital readout

Token passing readout to multiplex the 1024 data words onto the output bus
Tests Summary

Test structures measured as expected from simulations in terms of:

- Dynamic range:
  Sampling cell runs ok within 0-700mV as simulated
- Speed:
  Ring Oscillator up to 1.5 GHz
- Readout logic ok

One problem with I/O pads:
DC path to ground through protection diodes, but I/O’s can be easily overdriven.

Full sampling channels have still to be measured
Next Design

• Measure and fully understand the first version
• Test with actual MCP signals for pico-second timing

• Include:
  - Input trigger discriminator
  - Phase lock (Temperature, voltage supply, process)
  - Increase the dynamic range to 1V
  - Improve the analog bandwidth to 2GHz
  - Increase the sampling rate up to 20 GS/s
  - Improve the readout frequency to $8 \times 40 = 320$ MHz

• 130nm CMOS runs at MOSIS: Feb 1st, May 10th
20 GHz Timing generator [12]

40-160 MHz Clock in

<table>
<thead>
<tr>
<th>Delay (ps)</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
</tr>
<tr>
<td>200</td>
<td></td>
</tr>
<tr>
<td>200</td>
<td></td>
</tr>
<tr>
<td>200</td>
<td></td>
</tr>
<tr>
<td>200</td>
<td></td>
</tr>
<tr>
<td>250</td>
<td>32-64 cells</td>
</tr>
<tr>
<td>300</td>
<td></td>
</tr>
<tr>
<td>350</td>
<td></td>
</tr>
</tbody>
</table>

50ps step delays

To switched capacitor array
Outline

• Applications of Pico-second Timing
• Micro-Channel Plate devices
• Pico-second electronics and Waveform analysis
• Sampling Electronics
• Pico-second timing SCA in 130nm CMOS technology
• Perspective
Perspective

• The 4-channel 130nm CMOS ASIC:
  First tests ok, more test results to come shortly...

• Next chip: Upgrade with channel discriminator, internal PLL, improve analog bandwidth, sample rate, multi-gain input stages (QIE-like)

• Other ASIC design at the University of Chicago:
  An integrated Front-End for the Hadron Tile Calorimeter upgrade at ATLAS
  Include: 3-gain input stage, Integrator, 12-bit ADC

  130nm CMOS OK for these designs so far.

Latest technologies (90nm) are faster, but require multi-gain to cope with the reduced voltage supply range:

  Multi-gain switched capacitor arrays?
References


Jean-Francois Genat, Fermilab December 15th 2009
Thanks for your attention!