Fast Timing Electronics

Fast Timing Workshop

DAPNIA Saclay, March 8-9th 2007

Jean-François Genat LPNHE Paris

Outline

- Fast detectors, fast signals
- Time pick-off
- Time to Digital conversion
- State of the art
- Technologies
- Conclusion

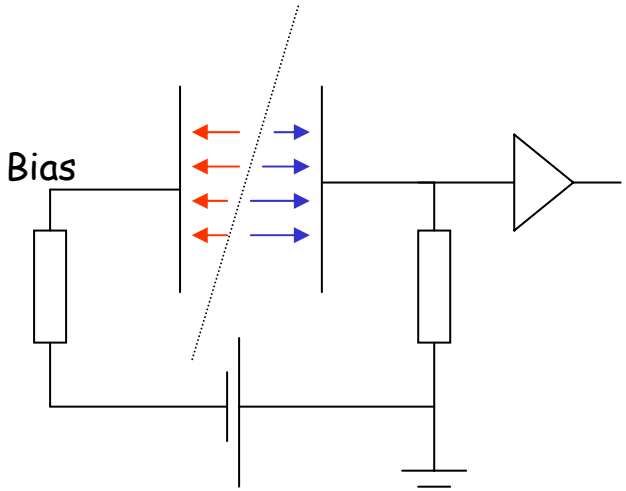
Fast detectors, fast signals

Detector Signals:

Moving charges (in an electric field):

$$i(t) = n(t)\, q\, v(t)$$

Rise-time $i'(t) = q\,[\, n(t)\, v'(t) + n'(t)\, v(t)]$



Maximize

n	electron multiplication	PMTs, MCPs
dv/dt	qE/m	electric field (in vacuum)
dn/dt	primary ionisation, multiplication	
v	t . qE /m	electric field

- Vacuum devices
- Electron multiplication
- Low capacitance
- High electric fields

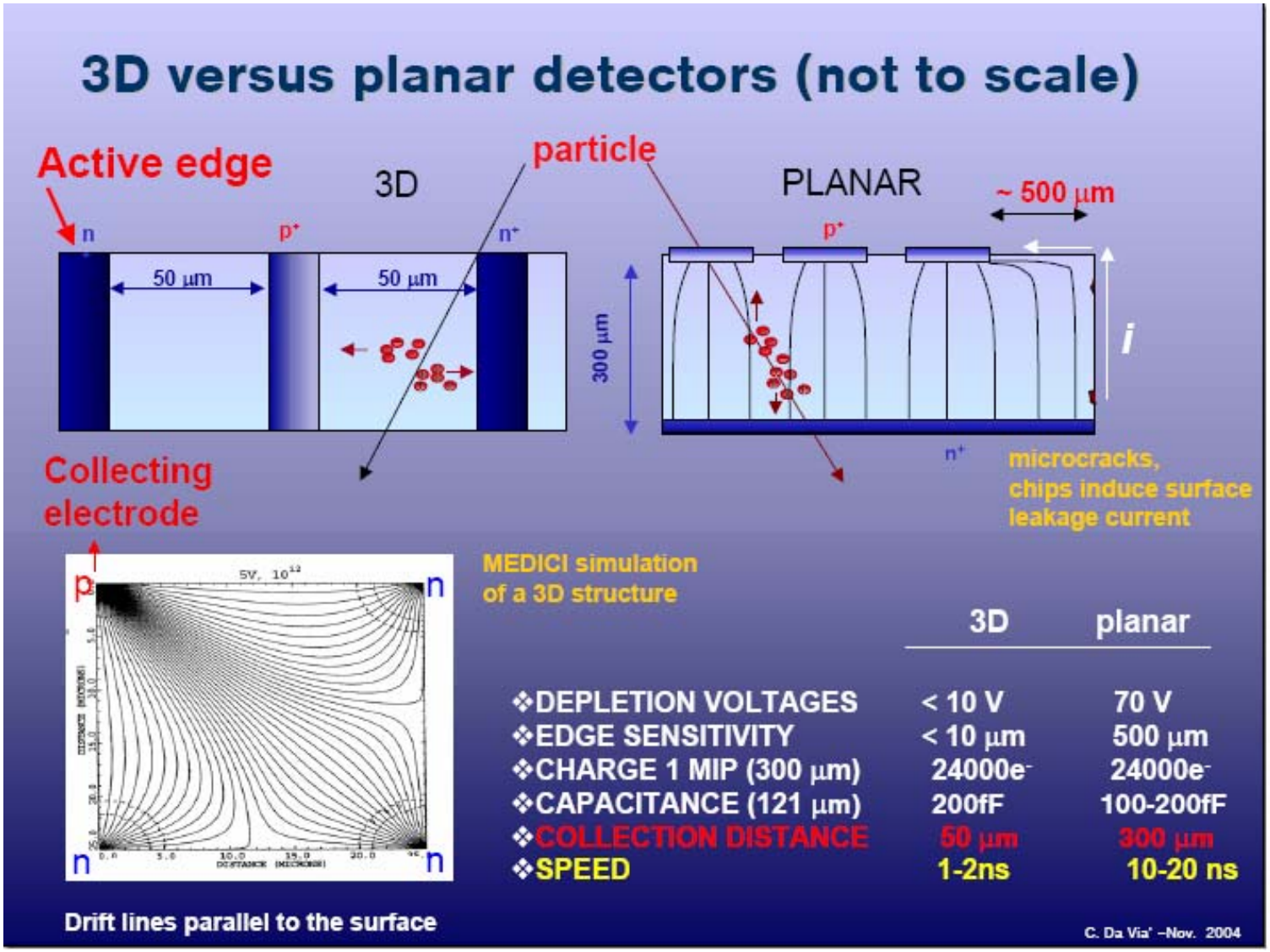
Fast detectors

Sub-nanosecond: 10-100 ps rise-time

Fast

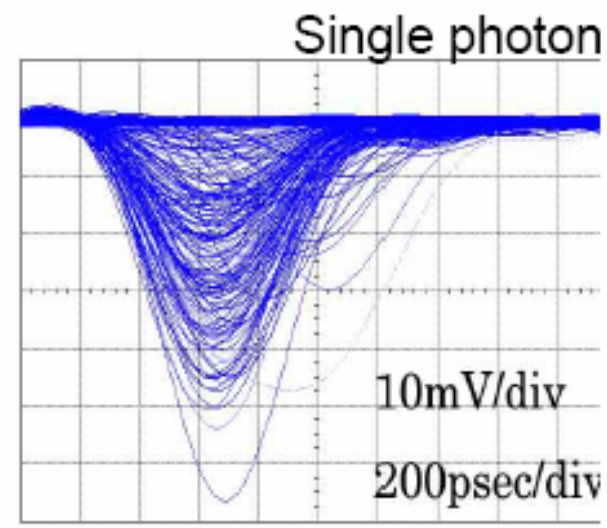
	Signals	Rise-time	Time resolution
Solid state			
• APDs	10^2	300 ps	50 ps
• Silicon PMs	10^7	700 ps	200 ps
• 3D Silicon	10^4	500ps	?
Very fast			
• Multi-anode/mesh PMTs	10^7	200ps	50 ps
• MCP PMTs	10^6	150 ps	20-30 ps
• Multi anodes MCP PMTs		30 ps ?	1 ps ?

3D Silicon detectors vs Planar

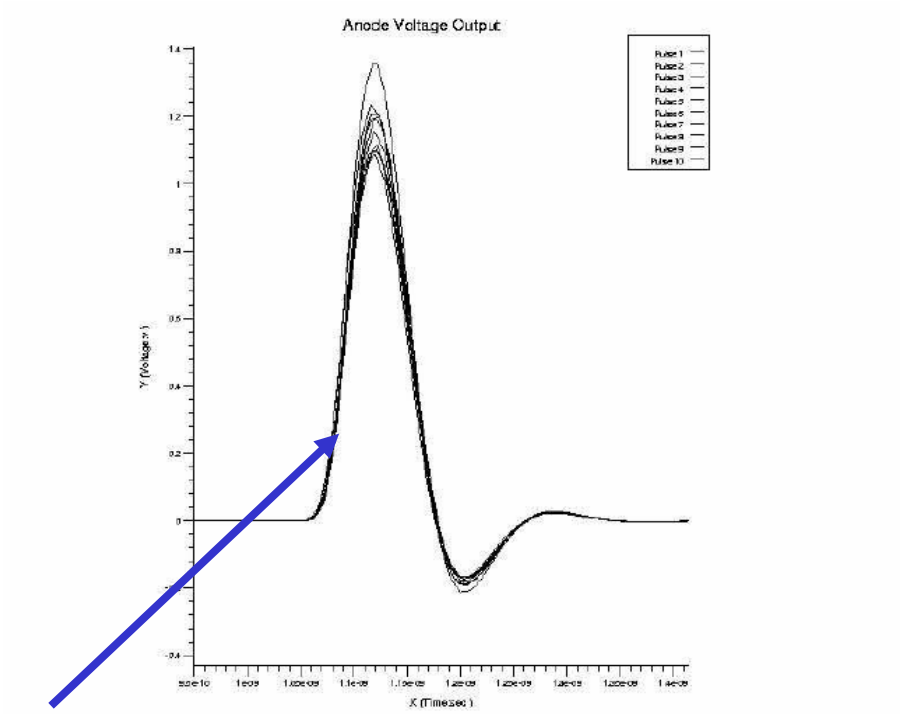


Cinzia Da Via, Brunel, UK 11/2004

MCP PMT single photon signals



Actual MCP PMTs signals
K. Inami et al
Univ. Nagoya
Tr = 500ps
tts= 30ps



MCP PMTs segmented anode signals simulation
tts = 860 fs
M. Sanders & H. Frisch,
Univ. Chicago, Argonne

N photo-electrons improves as $\sqrt{N}$

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Fast timing

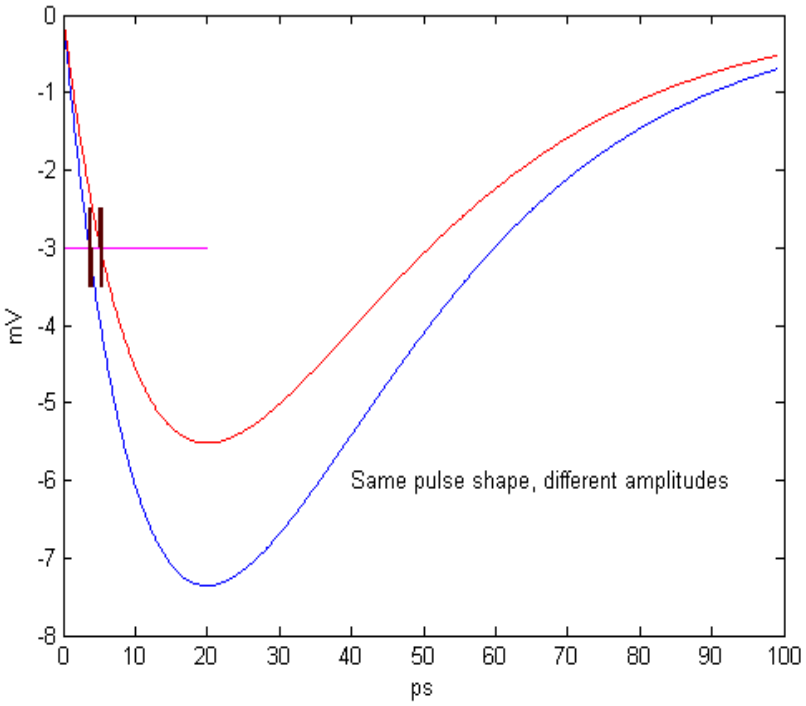
Electronics gain-bandwidth should match:

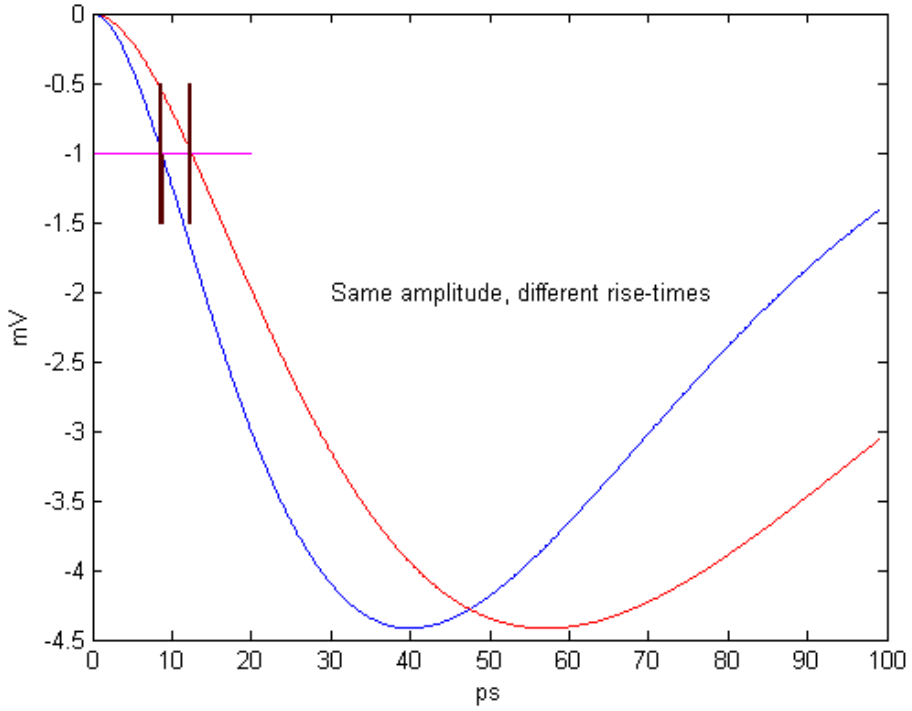
- Detector sensitivity
- Detector rise-time

Example: Multi-anodes MCP PMTs:

Rise-time: 25ps
Corresponding Bandwidth: 15 GHz

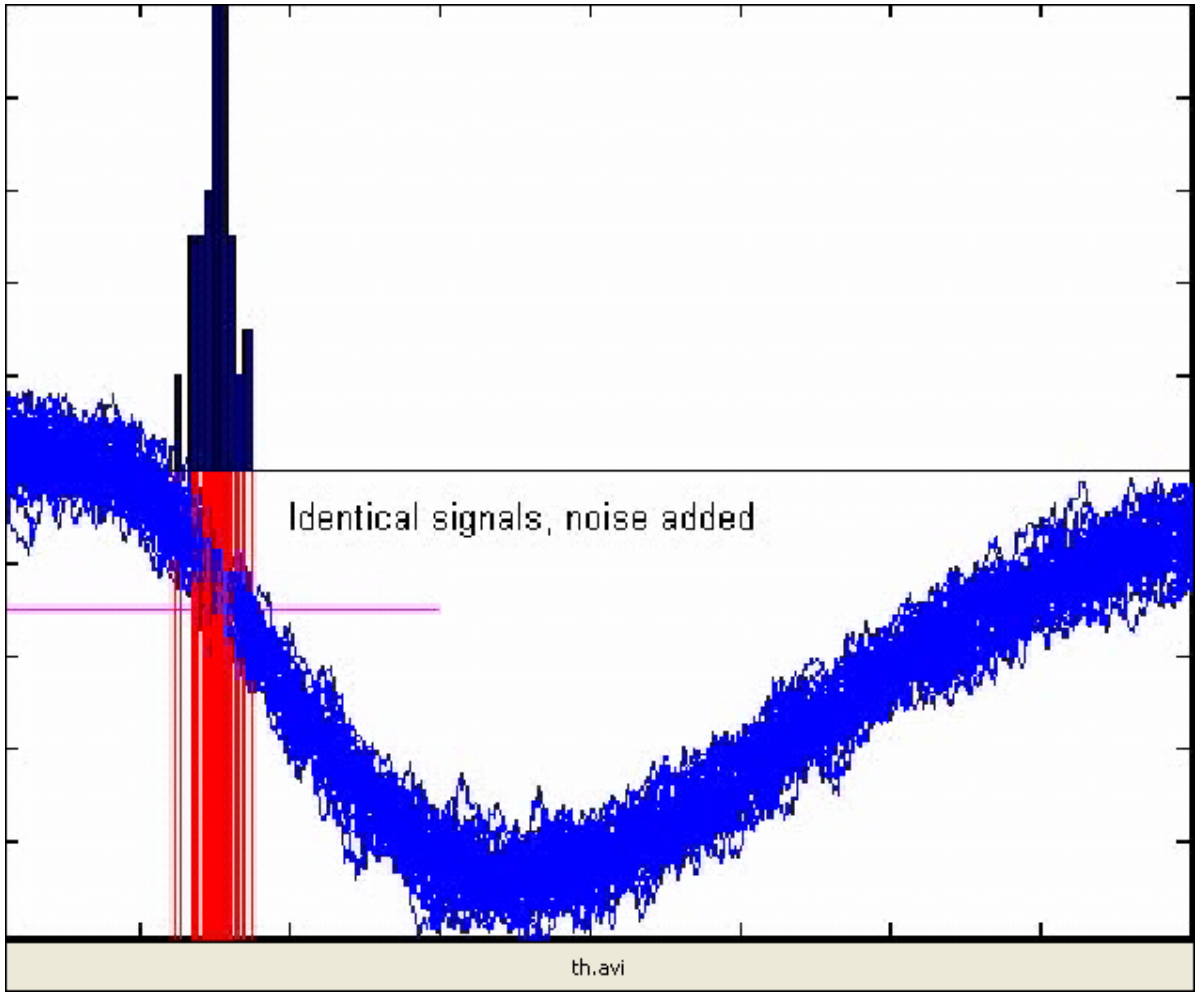
Effects of amplitude, rise-time





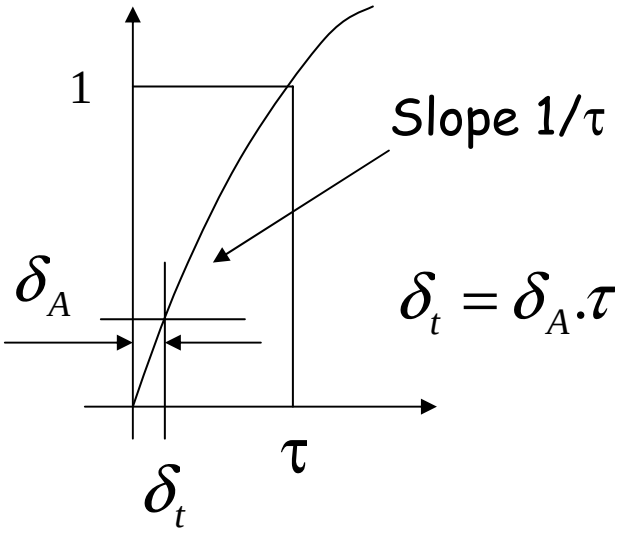
Amplitude and/or Rise-time spectra translate into time spread

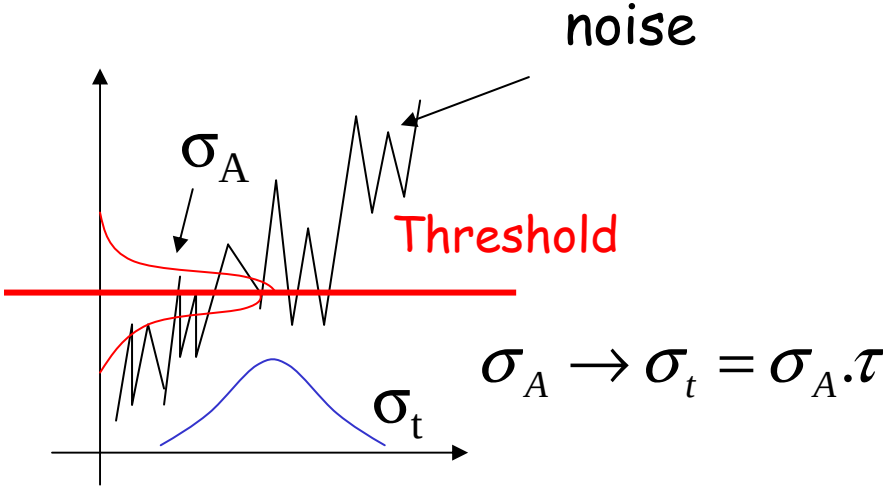
Effect of noise



Time spread proportional to rise-time

Leading edge

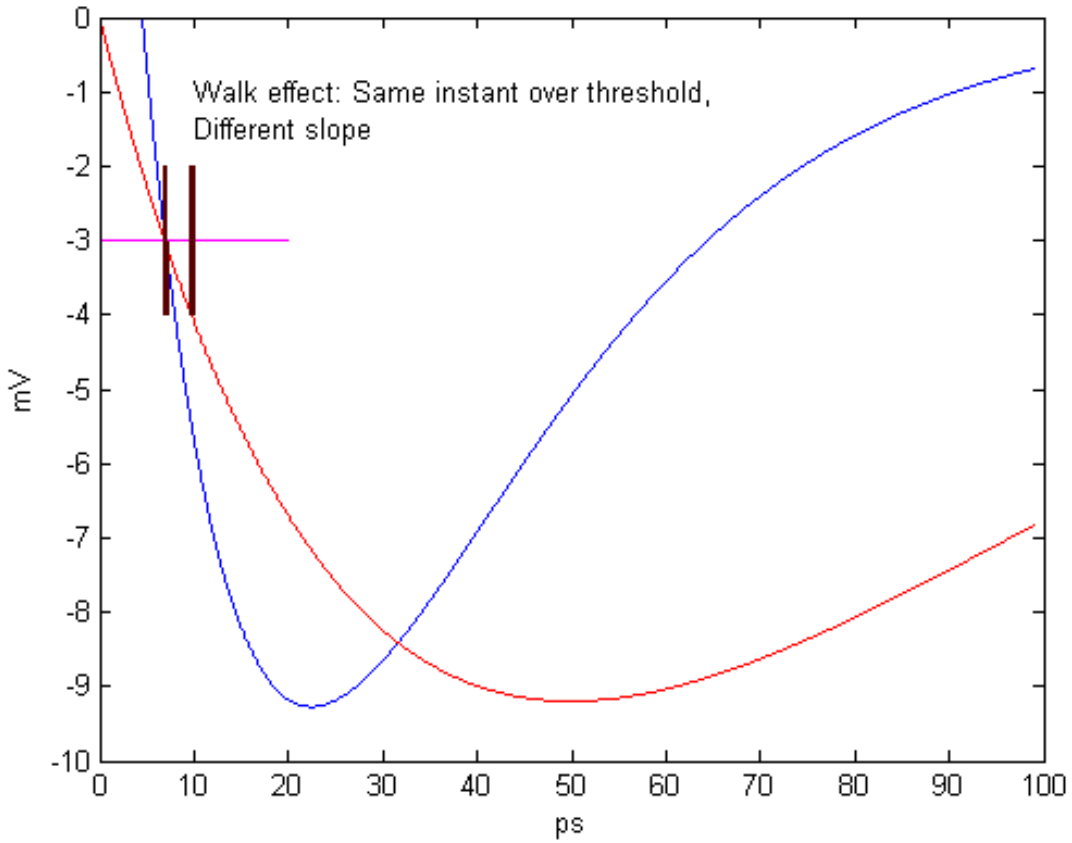




Effects of noise

Time spread proportional to rise-time

Other effects



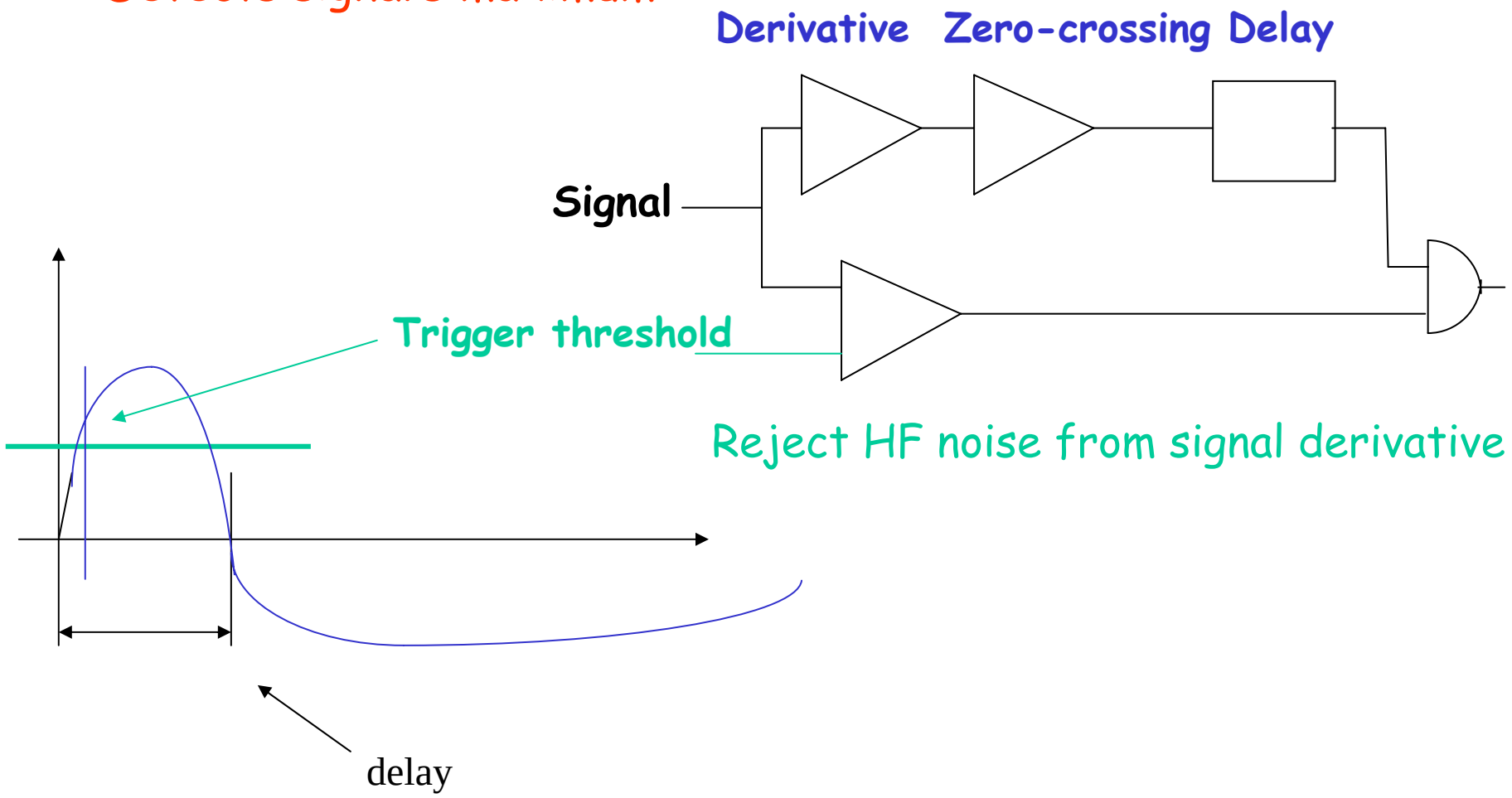
Walk: Discriminator delay depends on slope across threshold

→ (detector rise-time ⊕ amplifier)

Use appropriate (gain x bandwidth) technology

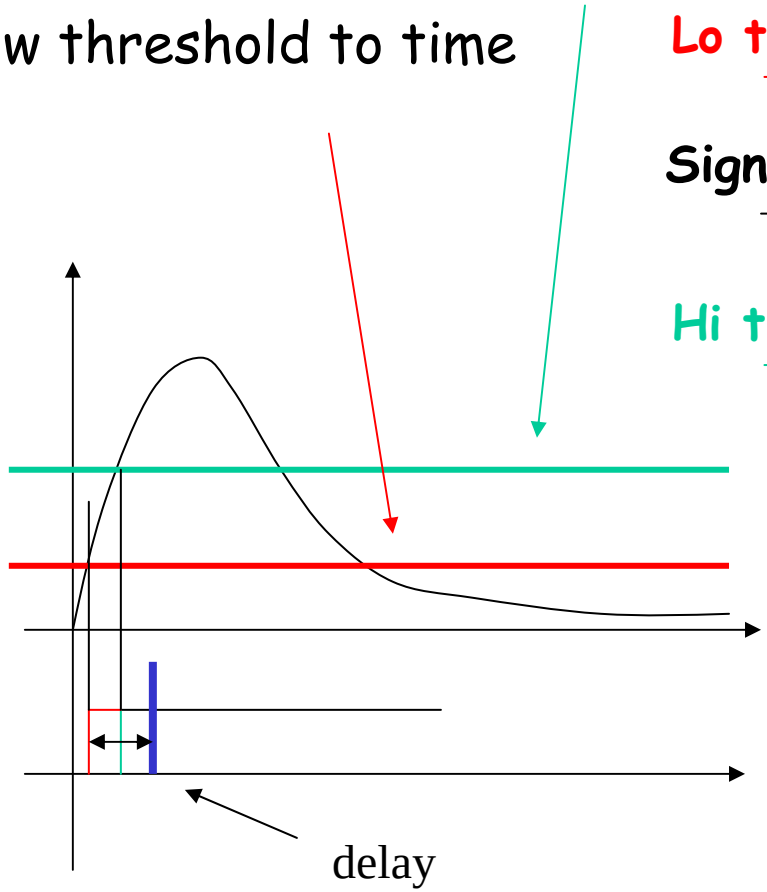
Zero crossing

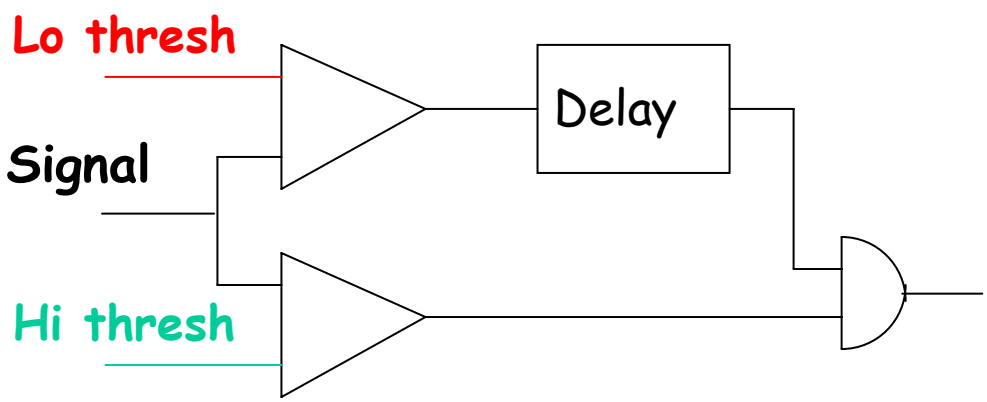
- Use zero-crossing of signal derivative
  Detects signal's maximum



Double Threshold

- High Threshold to trigger
- Low threshold to time

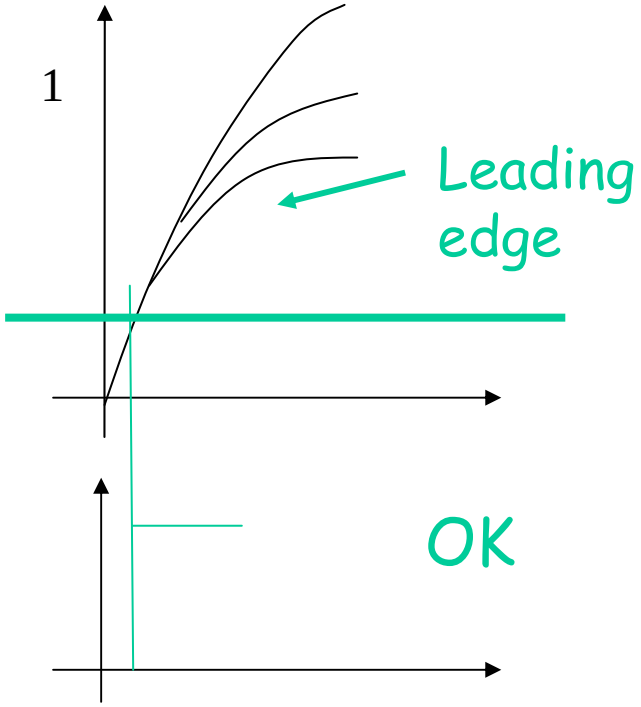


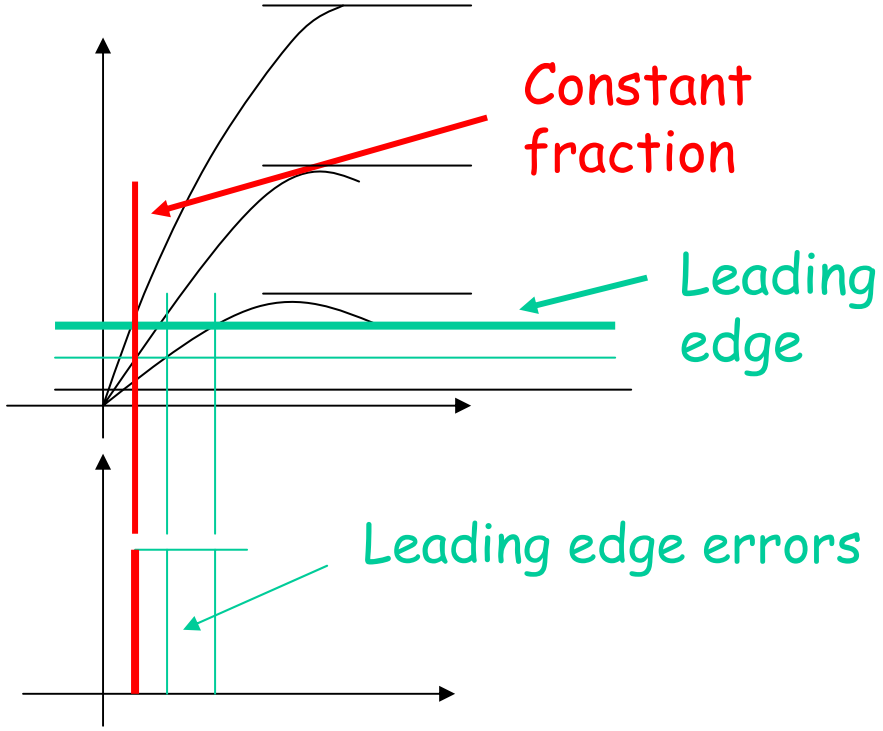


Avoids noise on low threshold
Decision on very first signal rise

Constant Fraction

If rise-time proportional to amplitude, use constant-fraction

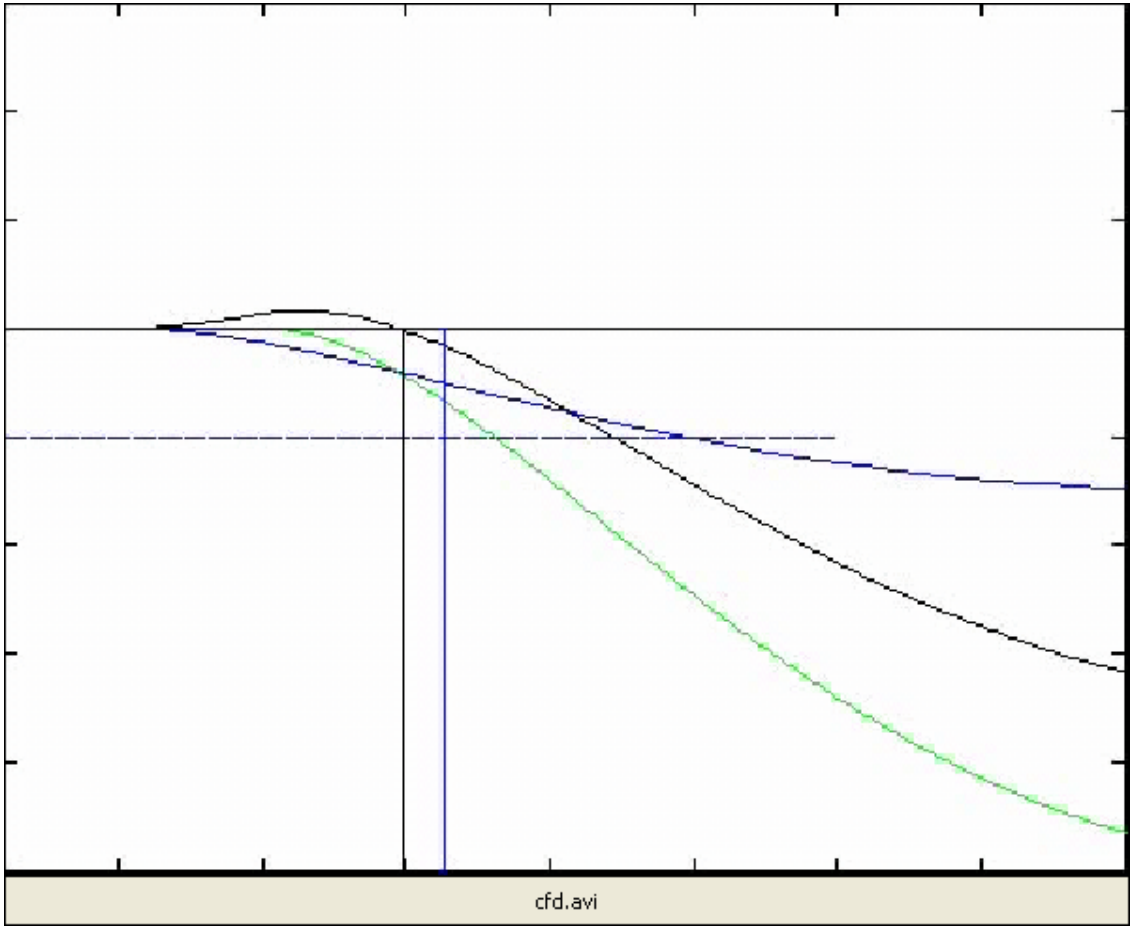




If no rise-time dependence with amplitude. Leading edge OK But detector presumably saturated, and slown down !

If pulse shape independent of amplitude, use Constant fraction

Leading Edge vs CFD



Constant Fraction

Three main parameters:

- Trigger threshold
- Delay
- Fraction

Maximize slope at zero-crossing
Carefully optimize wrt signals properties

H. Spieler [IEEE NS 29 June 1982 pp1142-1158]
T.J. Paulus [IEEE NS 32 June 1985 pp 1242-1249]

Leading edge + ADC

- If peak amplitude is measured, leading edge can be compensated off-line

Results compare with CFD technique (IEEE NSS 2006 San Diego)

Pulse sampling

Digitize samples over pedestal and signal

Fast analog sampler + ADC: [E. Delagnes, Saclay, this workshop]

Assuming the signal waveform is known from the detector and electronics properties:

→ Least square fit yields:

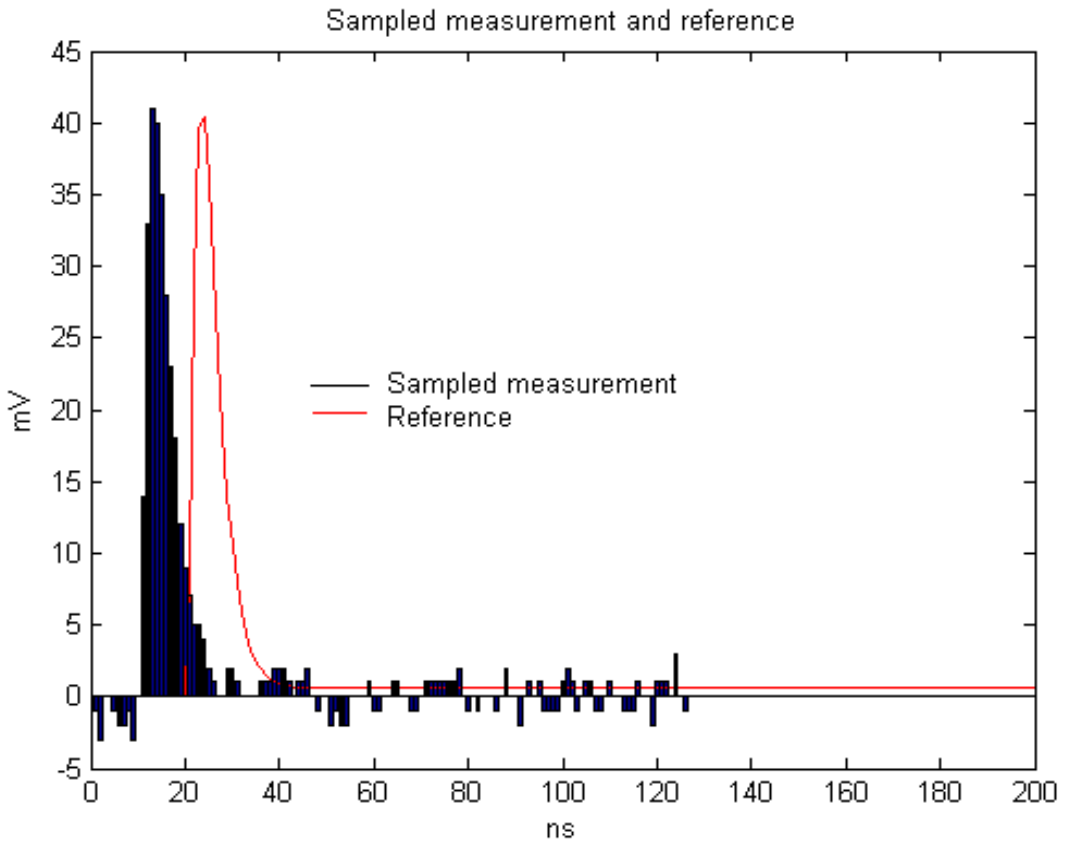
- Amplitude
- Time

Iterate with new values until convergence

LSQF: [W.E. Cleland and E.G. Stern. NIM A 338 pp 467-497]

- ***All samples contribute to timing estimation***
- ***Very robust to noise***

Pulse sampling



MATLAB Simulation with Silicon signals

Better compared to CFD by a factor of two depending on noise properties and signal waveform statistics

- MATLAB simulation package (JFG)

System issues

- Drifts due to environmental conditions
- Power supplies drifts and noise
- Cables/fibers instabilities

  - Cable has shorter group delay, and even higher bandwidth, may pick-up noise

  - Micro-coax makes a come-back

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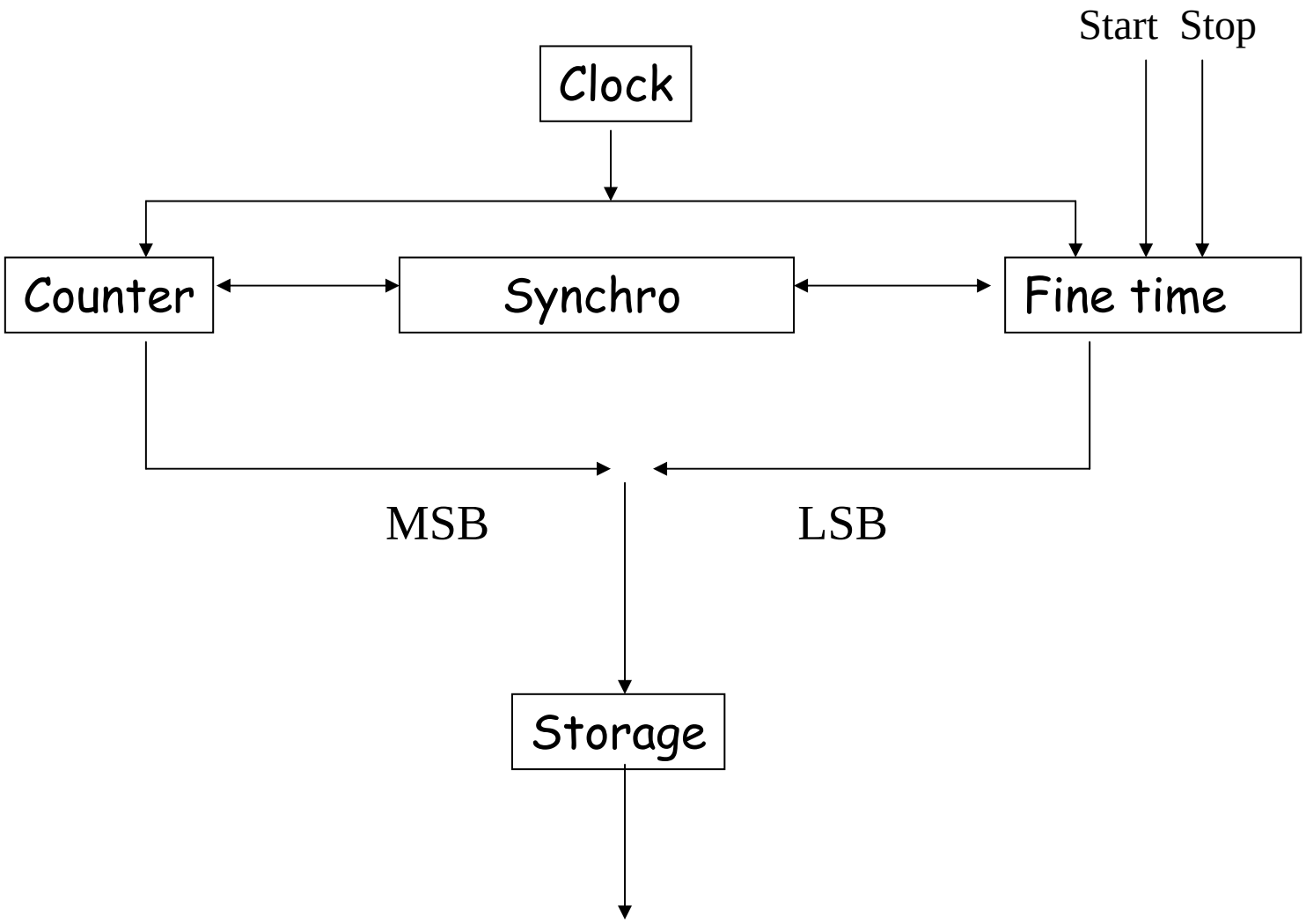
Time to Digital Coding

- "Coarse" (< 1 GHz) time coding use counters
- "Fine" (1-1000ps) time coding uses either

Time to Amplitude coding and ADC
or Digital delay lines phased locked on clock (DLL)

Both techniques can be differential or not
If short time range only is required, single TAC or DLL OK.

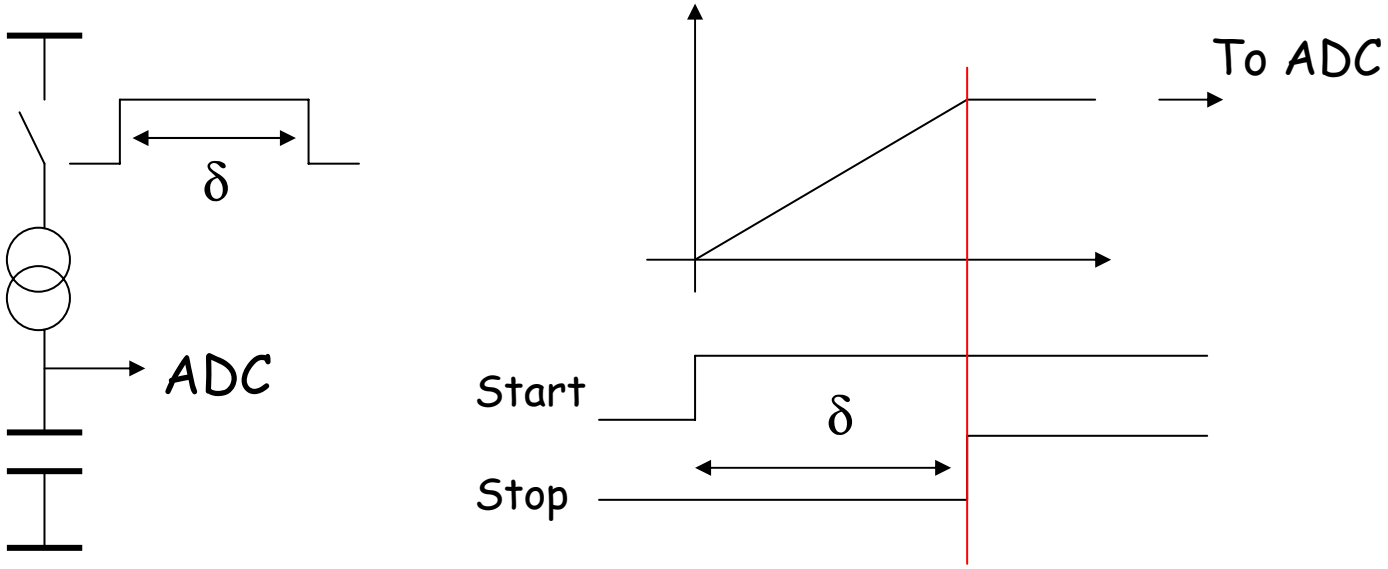
Architecture



Fine timing: Time to Amplitude Converter

- A voltage ramp is triggered on 'Start', stopped on "Stop"
  Stop can be a clock edge

- Amplitude is coded with a conventional ADC

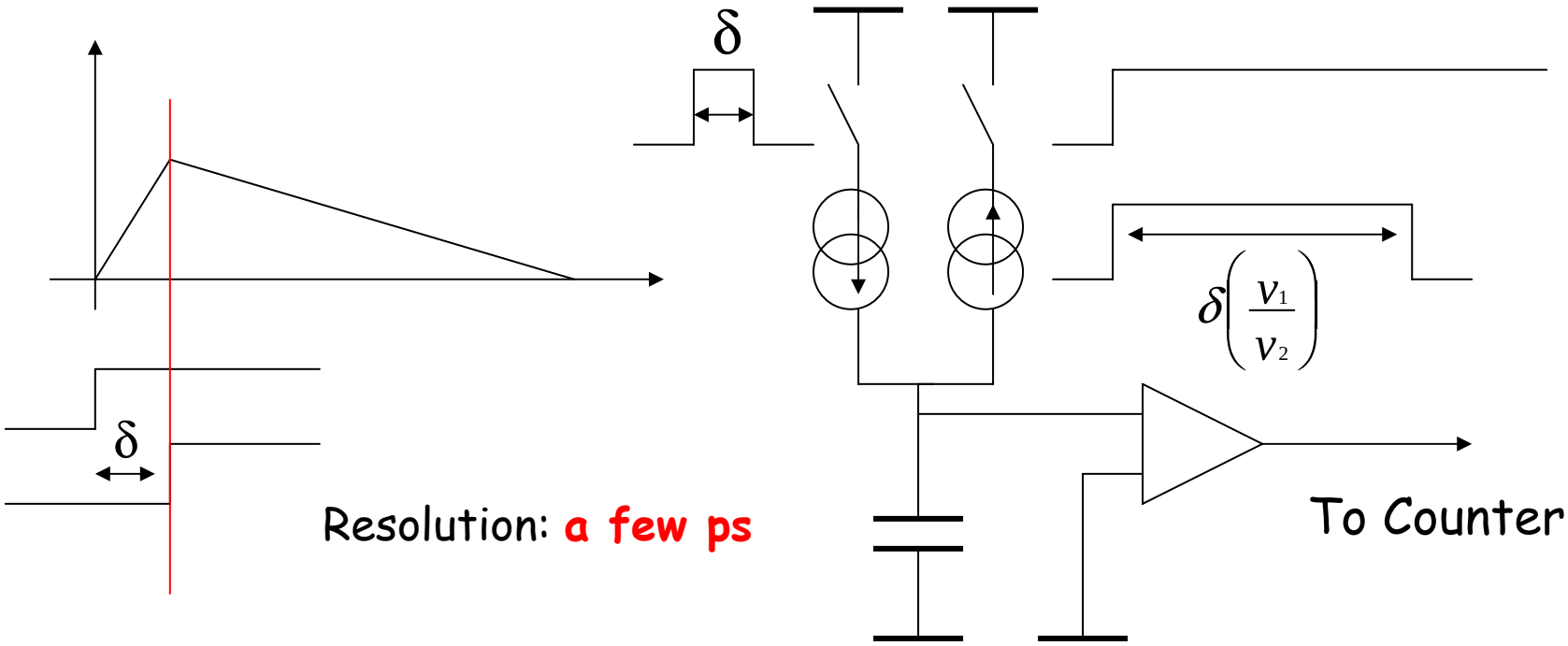


Differential TAC

Différential:

Same as above, ramp goes up at rate ν_1, down at rate $\nu_2 << \nu_1$

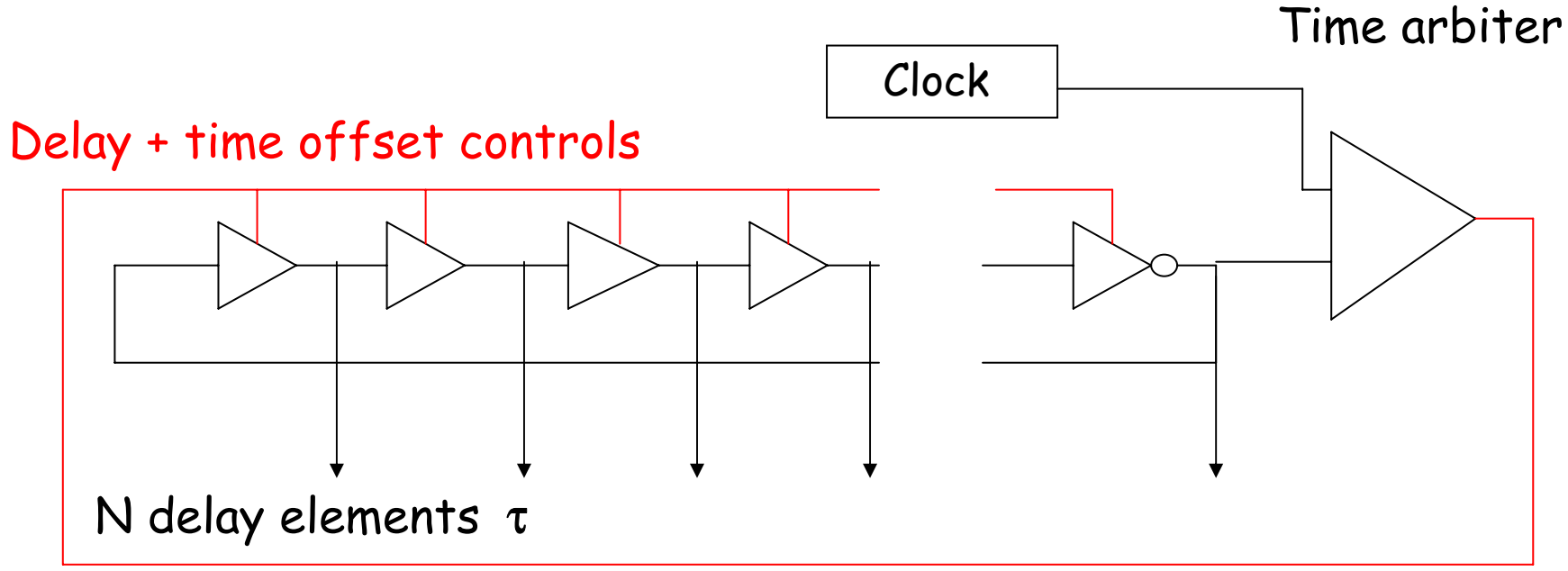
Time is stretched by $\frac{\nu_1}{\nu_2}$, measured using a regular counter



Fine timing: Digital Delay Lines

- Locked ring oscillator
  Loop of voltage controlled delay elements locked on a clock.

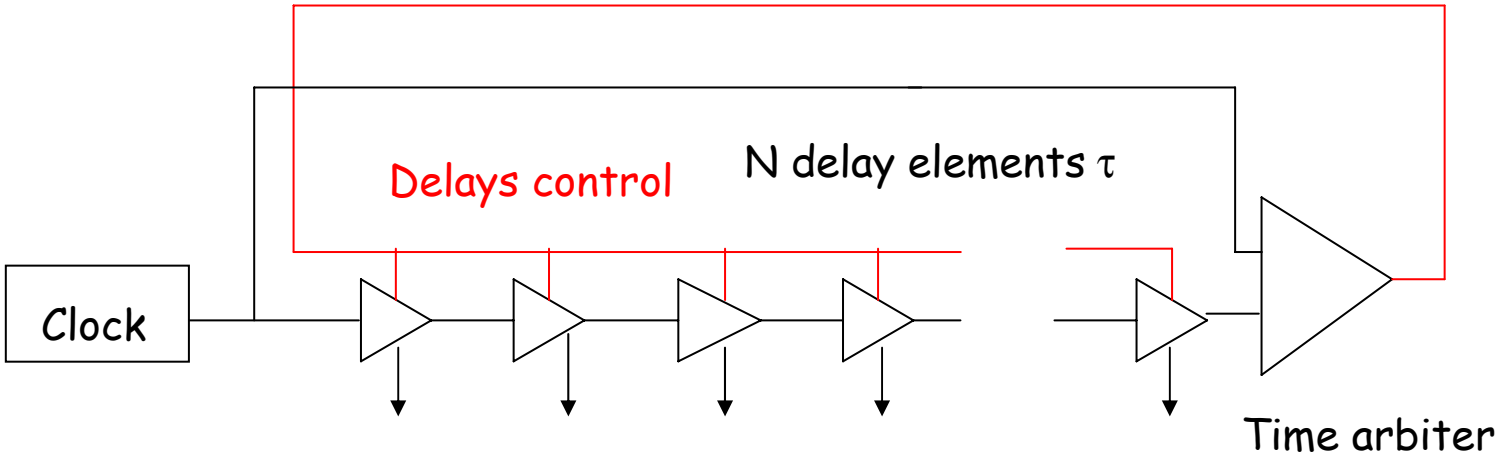
- Generation of subsequent logic transitions distant by τ.
  τ can be as small as 10-100 ps



Total delay N τ is in the range of half a clock period

Digital Delay Lines: DLL

Delay locked loop

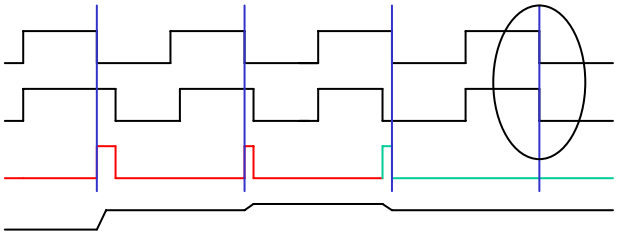


Clock feeds the digital delay line
Phase arbiter locks delays on clock period

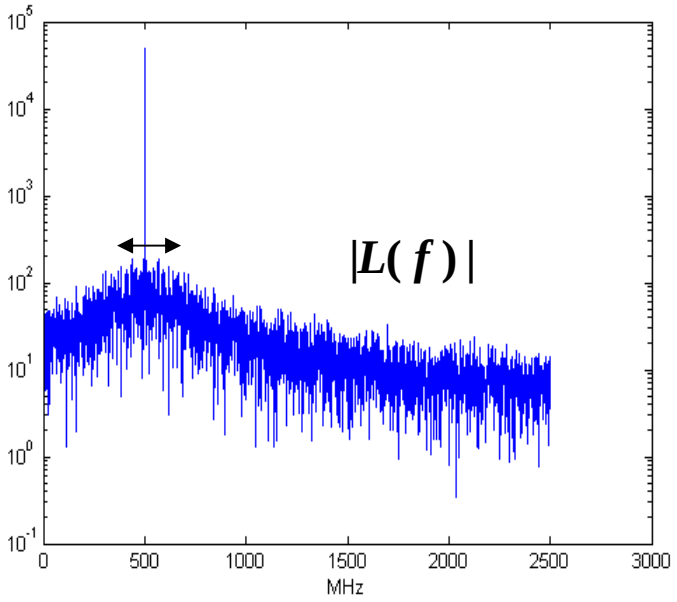
[M. Bazes IEEE JSSC 20 p 75]

Phase noise

Due to any analog noise source in the oscillator (thermal, 1/f…)

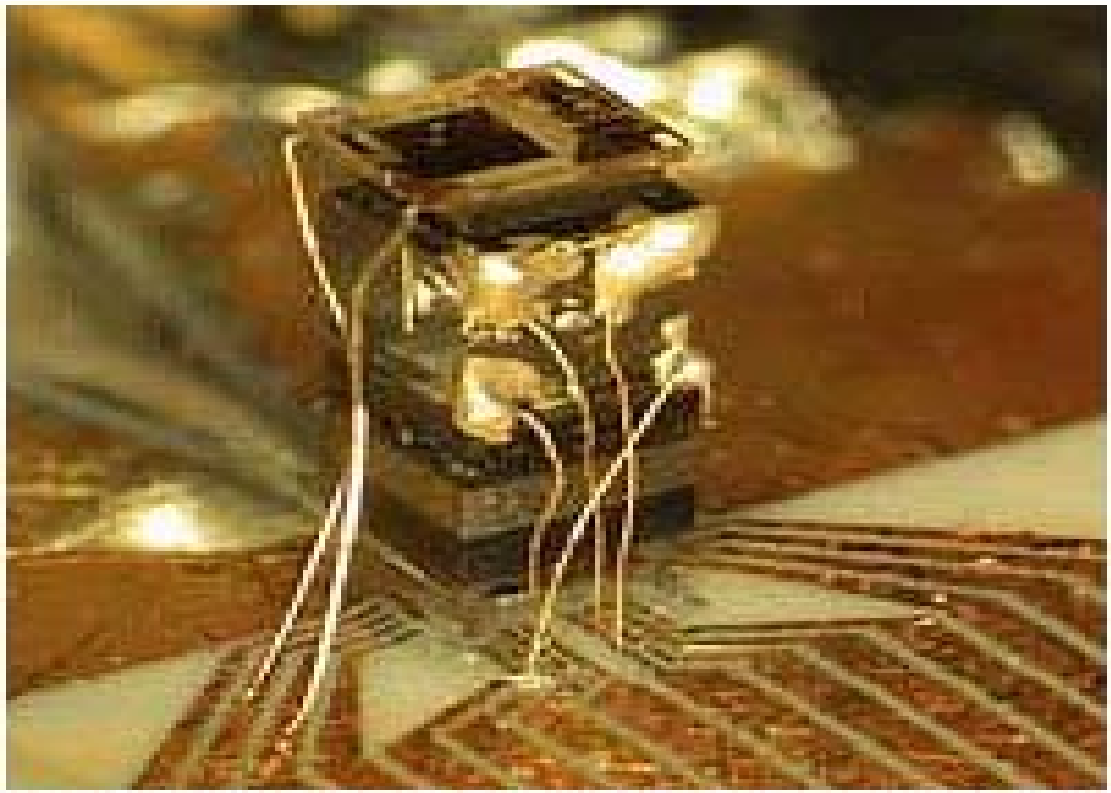


Power Spectrum:



$$j = \frac{f}{2\pi f_0(\Delta f)}\sqrt{\int_{\Delta f} 10^{L(f)/10}\,df}$$

Atomic Clock Chip



Courtesy: NIST

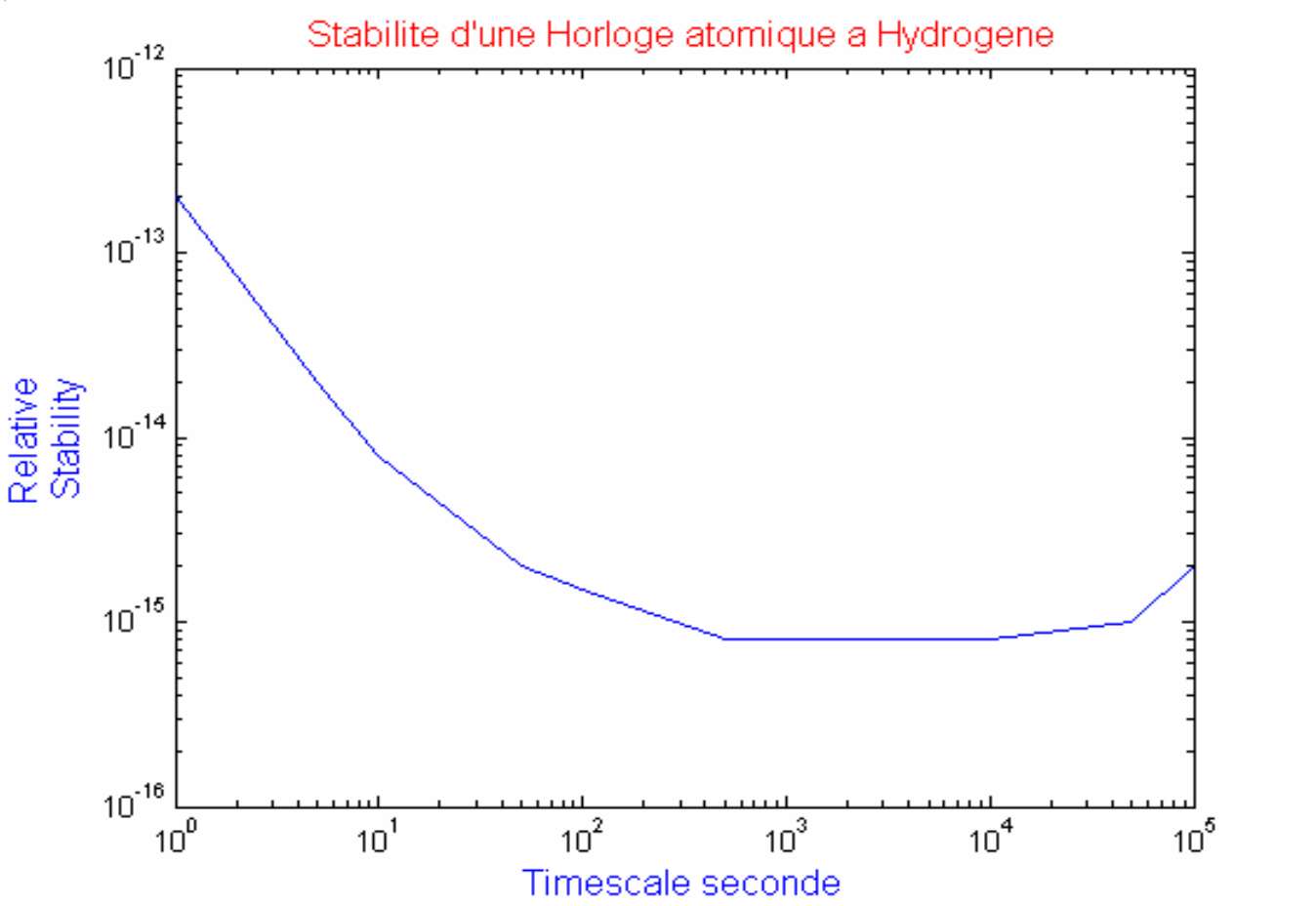
A few mm^3

The 'physics package' of the chip-scale atomic clock includes (from the bottom) a laser, a lens, an optical attenuator to reduce the laser power, a waveplate that changes the polarization of the light, a cell containing a vapor of cesium atoms, and (on top) a photodiode to detect the laser light transmitted through the cell. The tiny gold wires provide electrical connections to the electronics for the clock.

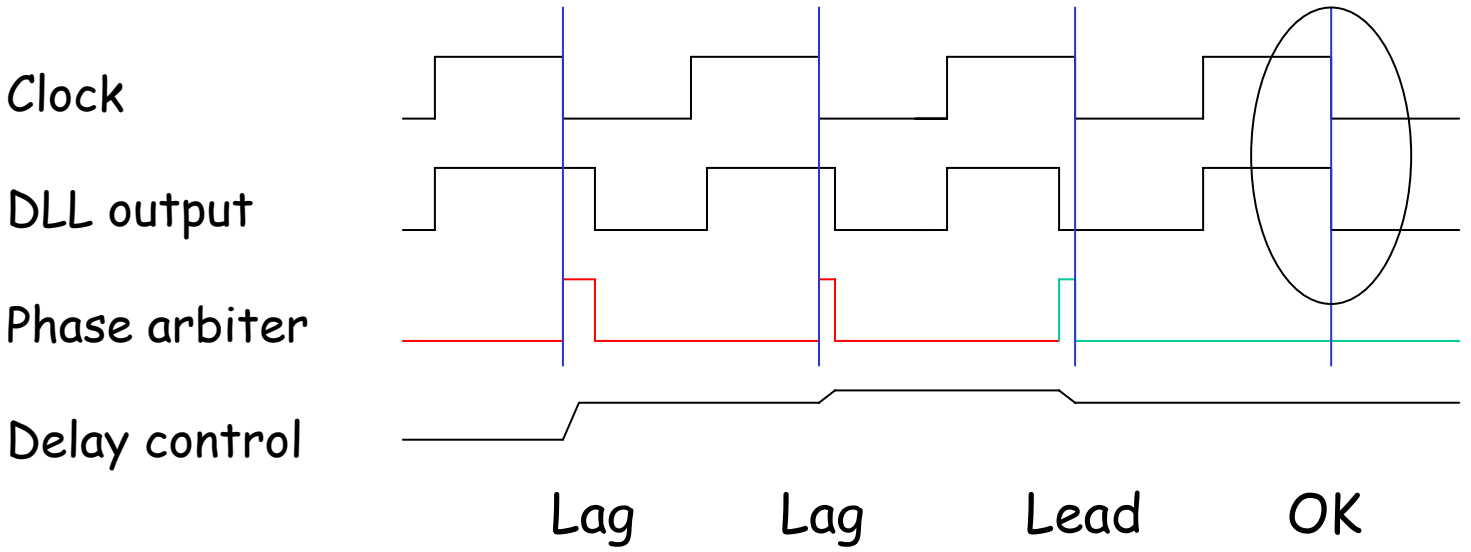
Stability

Short time stability: < 1s
Long term > 1s

Hydrogen: 1fs/s



Phase lock

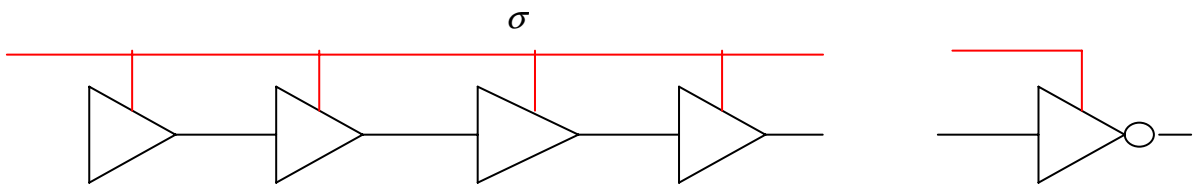


Feedback can be analog (RC filter) or digital using the TDC digital response itself

Delay elements

Active RC element: R resistance of a switched on transistor
C total capacitance at the connecting node

Typically RC = 1-100 using current IC technologies



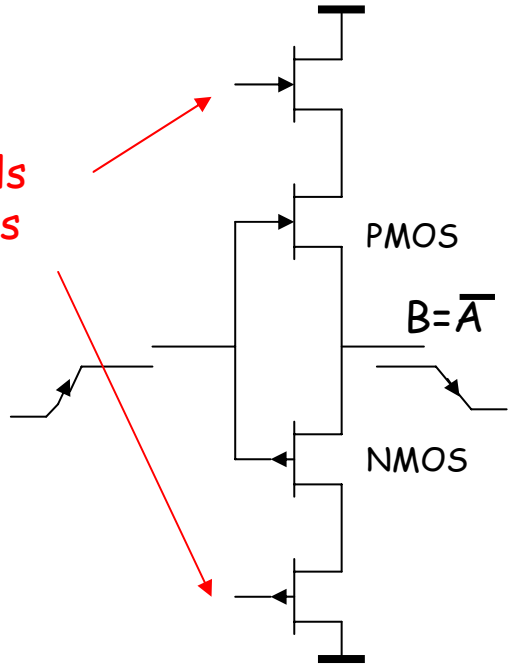
N delay elements τ

$\sigma_N = \sigma\sqrt{N}$ σ is technology dependent: the fastest, the best !

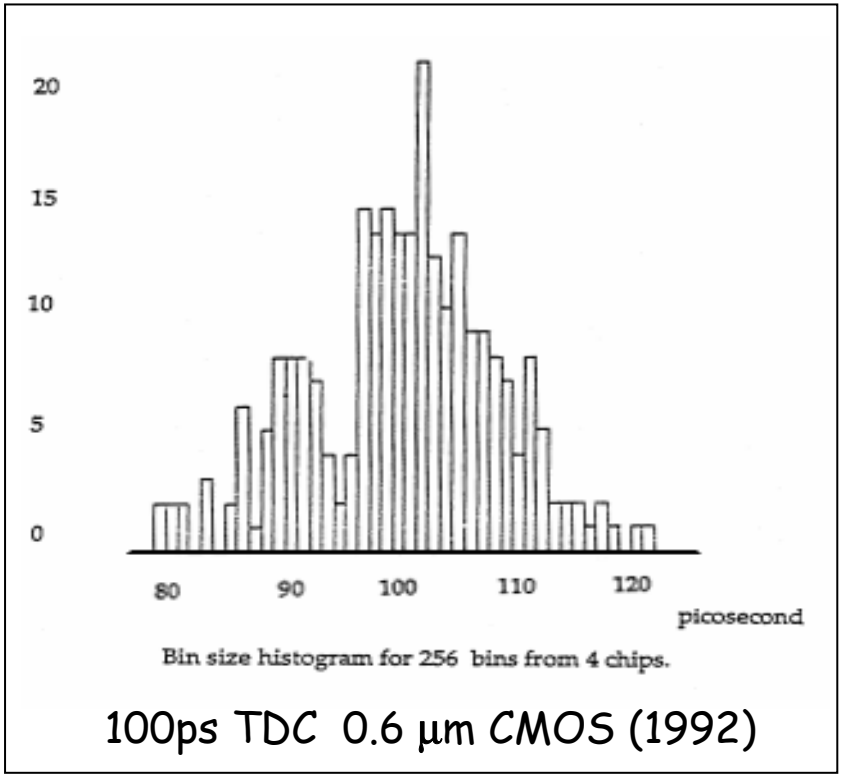
Within a chip σ ~ 1 %
a wafer σ ~ 5-10%
a lot σ ~ 10-20%

[Mantyniemi et al. IEEE JSSC 28-8 pp 887-894]

Time controlled delay element: Starved CMOS inverter



Propagation delay $\tau \sim$ 10-100 ps



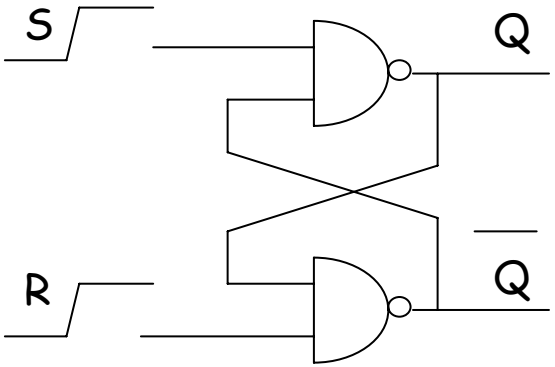
100ps TDC 0.6 µm CMOS (1992)

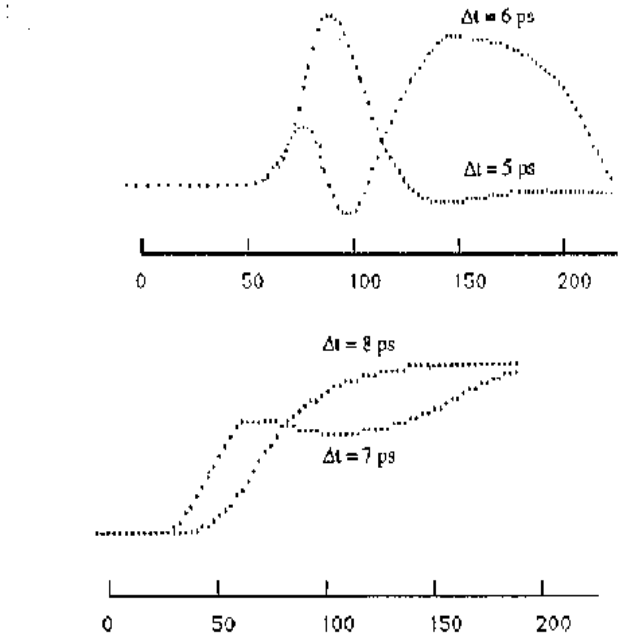
CMOS Technology 90nm: $\tau >\sim$ 20 ps

45nm < L < 250nm : 65 nm in production today

Time arbitration

SR flip-flop in the "forbidden" state (8 transistors)





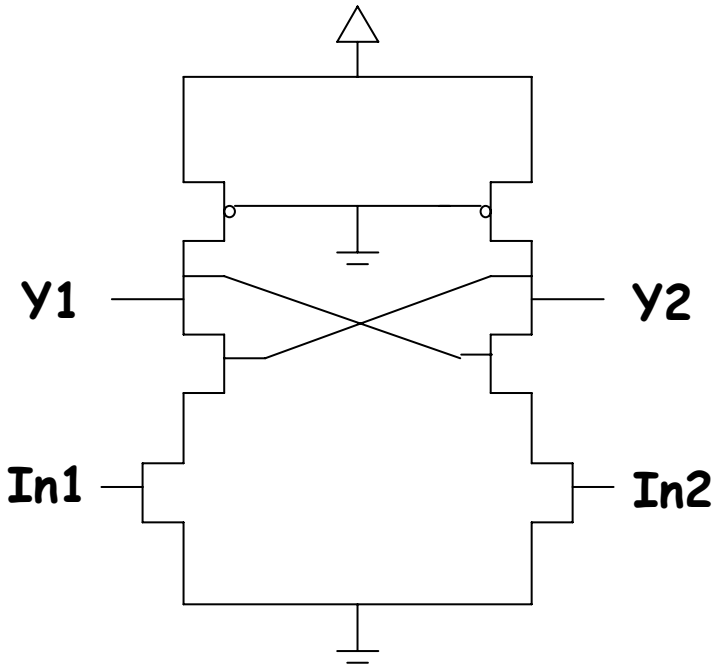
Final state depends upon first input activated:

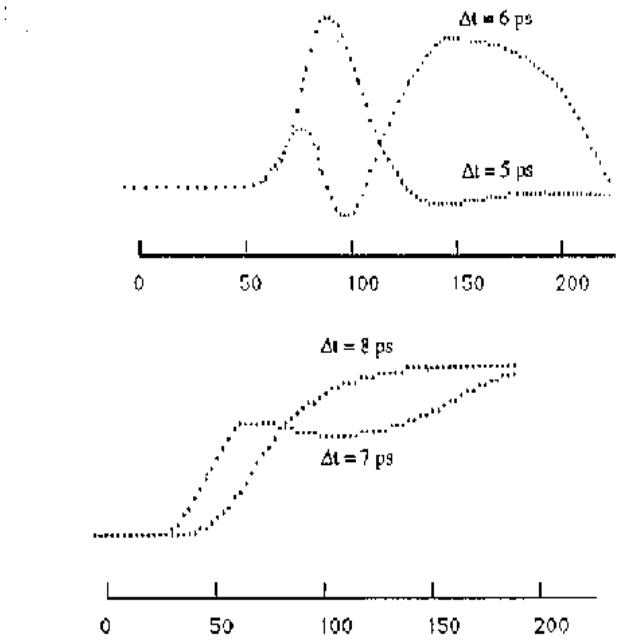
R prior S: $\overline{Q}$=1 , Q=0

R after S: $\overline{Q}$=0, Q=1

Issue: metastable states if S and R "almost" synchronous

Time arbitration





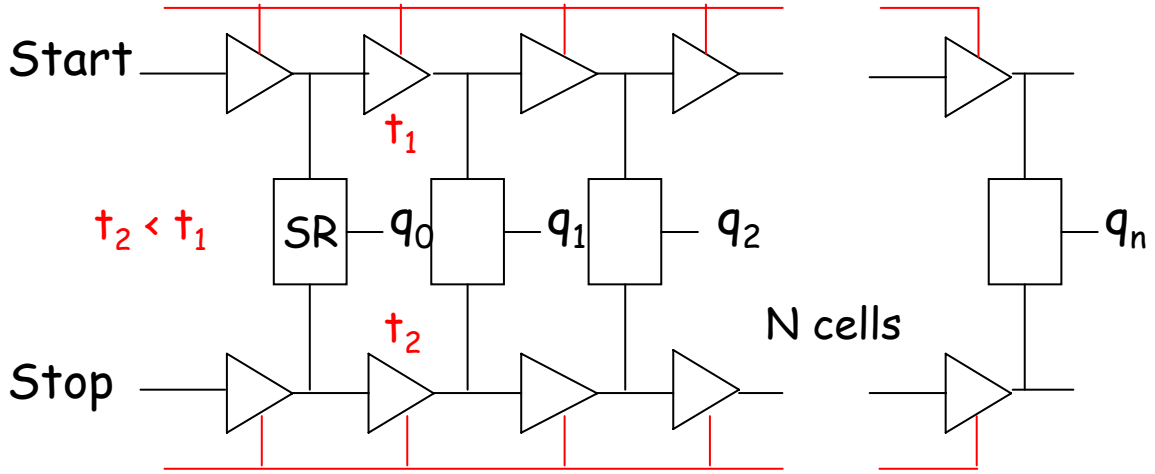
Six transistors implementation in CMOS

Same metastability issues

[V. Gutnik et al. MIT IEEE 2000 Symp. on VLSI Circuits]

Differential Delay Lines Time Vernier

Fast Stop, catches slow Start
Time quantum t_1-t_2 as small as technology spreads allow



$$N_{bit} = \frac{1}{2} Log_2 (T / \sigma)$$

N_{bit} = number of bits for ½ LSB precision
T = full-scale (maximum time interval to be measured)
σ = delay elements spread

Differential Delay Lines Time Vernier

Work for DELPHI (LEP) Outer Detector (1984):

500 ps binning, 150ps resolution TDC using digital delay lines
2 µm Gate Array technology

This work scaled today : 150 ps x 65nm / 2000nm = 4.8 ps

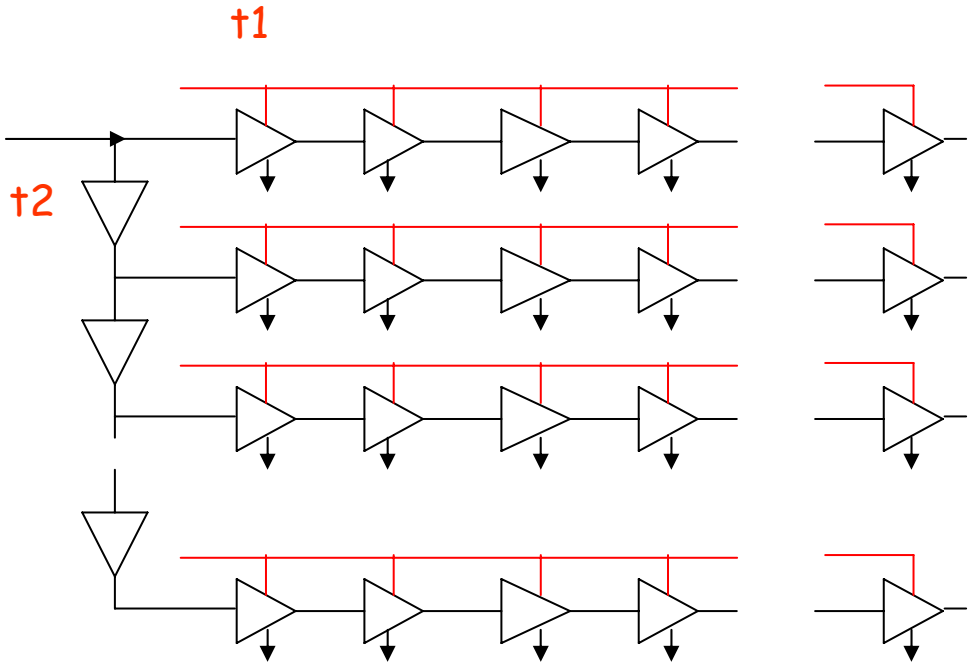
Digital delay lines:

Very short coding delay (no stretch, no ADC delay)

Multipulse Time Vernier

Multipulse version:
- Generate vernier references at any time
- Arbiter with incoming start and stops

Clock propagated



J. Christiansen (CERN)

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Picosecond chips

Digital

- Vernier delay lines offer 5–100 ps resolution for multi-channel chips

  Full custom: 25ps J. Christiansen, CERN

  8ps J. Jansson, A. Mantyniemi, J Kostamovaara, Olou Univ Finland

Analog

- 10ps TAC chip available from ACAM (2 channels) if channel rate < 500 kHz, 40ps @40 MHz

- Analog full-custom chips: Argonne is designing disc + TAC full-custom chips for 1 ps in SiGe 250nm HBT technology
  [F. Tang, this workshop]

Picosecond electronics

- Picosecond resolution hardware

The TCSPC Power Package SPC-134

Four-Channel Time-Correlated Single Photon Counting Module

Four Fully Parallel TCSPC Channels
Ultra-High Data Throughput
Overall Saturated Count Rate 40 MHz
Channel Saturated Count Rate 10 MHz (Dead Time 100ns)
Dual Memory Architecture: Readout during Measurement
Reversed Start/Stop: Repetition Rates up to 200 MHz
Electrical Time Resolution down to 8 ps FWHM / 5 ps rms
Channel Resolution down to 813 fs
Up to 4096 Time Channels / Curve
Measurement Times down to 0.1 ms
Instrument Software for Windows 2000 / NT / XP
Direct Interfacing to most Detector Types
Single Decay Curve Mode
Oscilloscope Mode
Seqential Recording Mode
Spectrum Scan Mode with 8 Independent Time Windows
Continuous Flow Mode
FIFO / Time Tag Mode for FCS, FIDA, FILDA, BIFL

Becker & Hickl Germany

5ps rms @ 200 MHz

Some Costs

.

Becker & Hickl	SPC 134	4-channel 1ps	CFD +TDC	system	7 kEuros/ch
ACAM	TDC-GPX	2-channel 10-30ps	TDC	chip	80 Euros
ORTEC	935	4-Channel 30ps	CFD	NIM	

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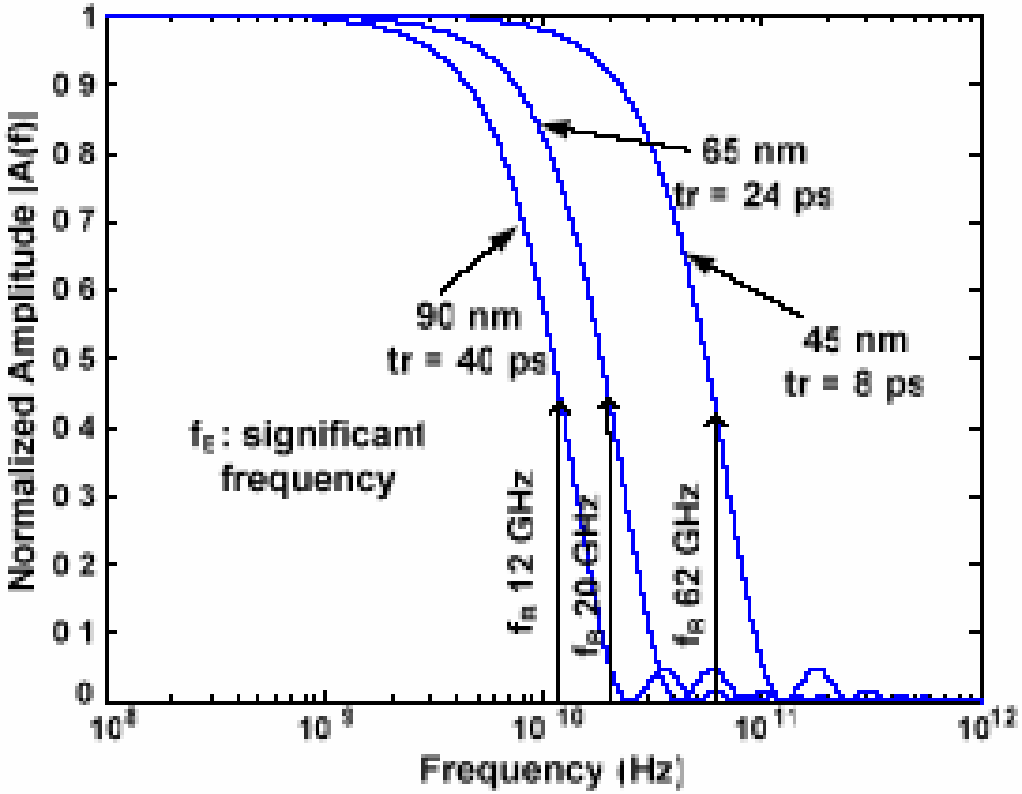
CMOS Technologies

CMOS

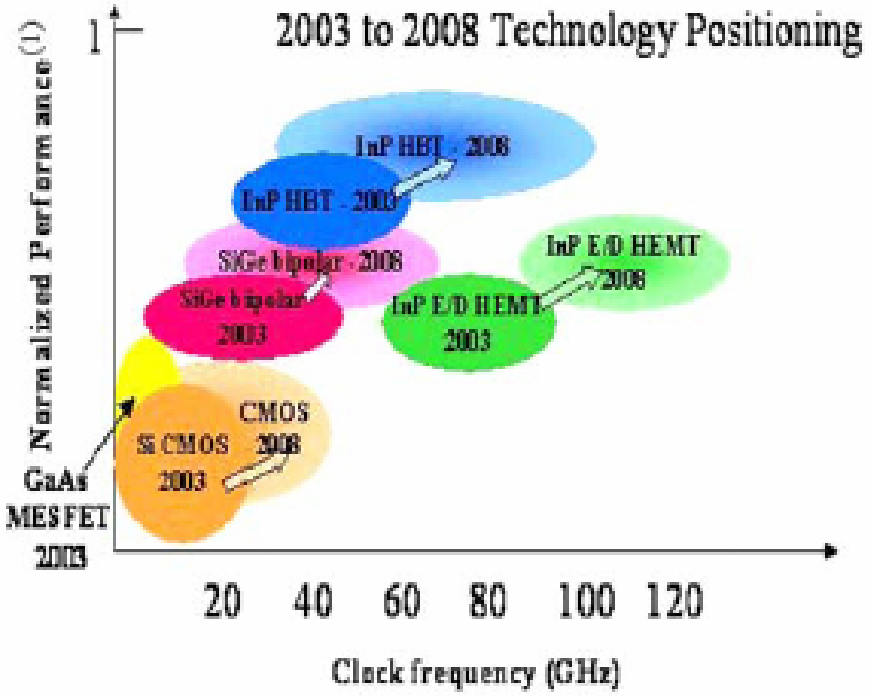


CMOS from 90 to 45 nm technology nodes (ITRS 2005)

Technologies

SiGe HBTs 220 GHz MPW from IHP IBM

- Ned Spencer (UCSC) LHC [Perugia FEE 2006]
- Fukun Tang (Univ Chicago) Picosecond timing [this workshop]



ITRS from 2003 to 2008 (2005)

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3D imaging using fast Timing with APDs array

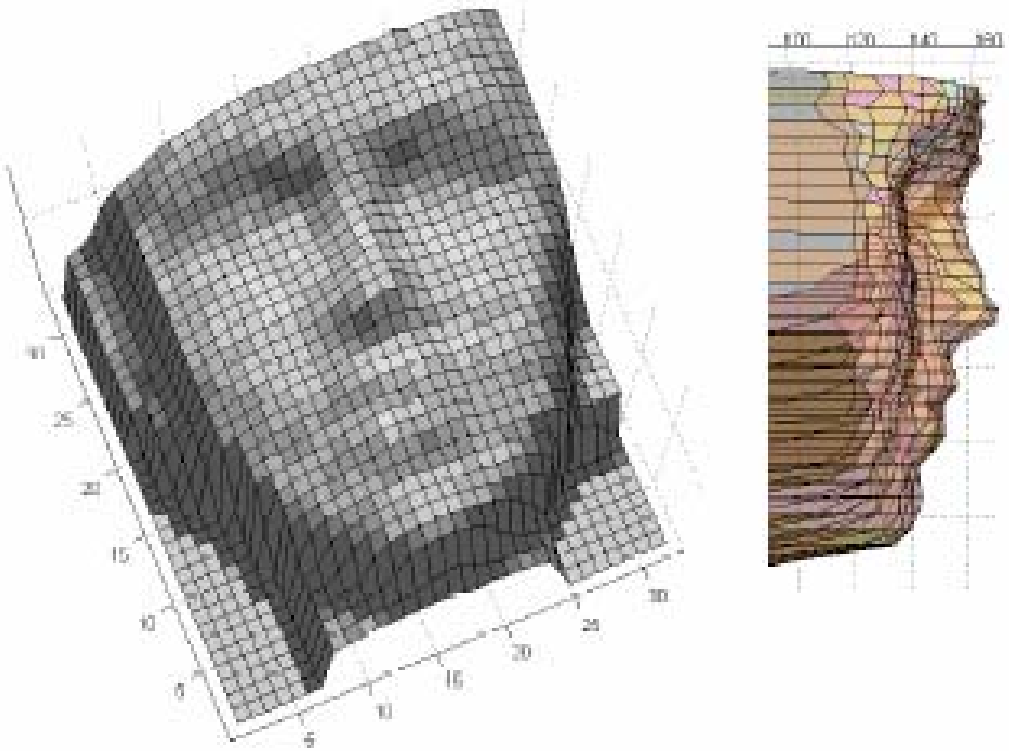
- C. Niclass et al. [EPF Lausanne, Switzerland, 2006]

  Close to SiPM devices (Geiger mode, self-quenching by pulse current avalanche through MOS transistor)

  On chip readout electronics

- tts from APDs < 50 ps

- Overall 300 ps resolution (TDC dominated) resulting in a 1.8mm spatial resolution using 10^2 to 10^4 points



Human face depth map and profile (in mm)

Today, 10 ps is integrated
1 ps under work, looks promising from very fast VLSI technologies

The End