Signal and Noise Characterization of MCP-PMT's

Jean-Francois Genat

University of Chicago

Large-Area-Picosecond-Photo-Detectors electronics for Particle Physics and Medical Imaging

LPC Clermont-Ferrand, January 28th 2010
With the help of


and many others...
Micro-Channel Plates Signals and Noise Characterization

Signals: - The MCP devices are faster than a PMT...

Noise : - The MCP device are very silent...
# Timing-Imaging Devices

<table>
<thead>
<tr>
<th>Multi-anodes PMTs</th>
<th>Silicon-PMTs [10]</th>
<th>Micro-Channel Plates [1]</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Dynodes</strong></td>
<td>Quenched Geiger in Silicon</td>
<td>Micro-Pores</td>
</tr>
</tbody>
</table>

| Quantum Eff.     | 30%               | 90%            | 30%               |
| Collection Eff.  | 90%               | 70%            | 70%               |
| Rise-time        | 0.5-1ns           | 250ps          | 50-500ps          |
| Timing resolution (1PE) | 150ps       | 100ps          | 20-30ps           |
| Pixel size       | 2x2mm$^2$         | 50x50µm$^2$    | 1.5x1.5mm$^2$    |
| Dark counts      | 1-10Hz            | 1-10MHz/pixel  | 1Hz-1kHz/cm$^2$  |
| Dead time        | 5ns               | 100-500ns      | 1µs               |
| Magnetic field   | no                | yes            | 15kG              |
| Radiation hardness |                   | 1kRad=noisex10 | good (a-Si, Al$_2$O$_3$) |

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Jean-Francois Genat, Large Area Picosecond Photo-Detectors Electronics, LPC Clermont-Ferrand, January 28$^{th}$ 2010
Outline

• Micro-Channel Plate devices
• MCP signals
• Origin of noise
• Measurements
• Conclusion
Timing-Imaging Devices
Micro-Channel Plate Detectors [1-3]

**Timing Resolution:** Single Photo-electron Time Transit Spread:

\[ \sigma_t^2 = \sigma_{1\text{st\,gap}}^2 + \sigma_{\text{pore}}^2 + \sigma_{2\text{nd\,gap}}^2 \]

The thinner the device, the better the Timing Resolution

Jean-Francois Genat, Large Area Picosecond Photodetectors Electronics, Clermont-Ferrand, January 28th 2010
Position resolution using analog charge division

Position

Fig. 4. A profile along a line cut across the MCP pores of Fig. 3. The spatial resolution of the readout is \( \sim 2\mu m \) rms, capable of resolving every single MCP pore.

High precision analog measurements.

But integration time = 200ns
Outline

• Micro-Channel Plate devices
• MCP signals
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• Conclusion
MCP signals

Segmented anodes, Burle-Photonis

Glass + ALD MCPs (from Matt Wetstein, ANL)

Single Photon
16-averaged
Sampling: 18 GS/s

Time response curves for two models of PMT110 with different MCP pore diameters.
MCPs signal development: pulse

MCP signal rising edge: \( qE = ma \)
\[ l = 1\text{mm}, \ E=100\text{V/mm}, \ tr=250\text{ps} \]

Slown down by: \( RC = 50\ \Omega \cdot 5\text{pF} = 250\text{ps} \)

Fast rise-time: thin 2d gap, low LC parasitics
MCP Device Simulations: Photo-cathode gap

Monte-Carlo: $10^6$ single photoelectrons events
Simulation of the first gap: photocathode - pores input

Angular distribution: $\text{asin} \{\text{rand}[-1,+1]\}$

Gap 2 mm

RMS: 5.05228 ps

5 ps contribution to TTS
(20-30 ps total measured)

Lionel de Sa

Full device simulations:
Valentin Ivanov
Zeke Insepov
MCP signal development: “shaping”

MCP signal rising edge: \[ qE = ma \]
\[ l = 1\text{mm}, E=200\text{V/mm}, \text{tr}=250\text{ps} \]

\[ \text{tr} = l \sqrt{2m/qV} \]

Effect of parasitics:
\( C=\)capacitance of the detector
\( R=50 \ \Omega \)

\[ i_1(t) = i_0 t / (t + RC) \]

Fast rise-time:  thin 2d gap,  low LC parasitics
MCP Signal development

Effect of first order passive:

\[ i_1(t) = \frac{i_0 t}{t + RC} \]

Rise time is RC dependent at first order.

Jean-François Genat, Large Area Picosecond Photo-Detectors Electronics, Clermont-Ferrand, January 28th 2010
Single PE Signals

From Dolgoshein et al.                                       From Paul Hink (Burle-Photonis)

Fig. 3. SiPM application for sci fiber MIP detection (at room temperature): comparison with APD [6] (room temperature) and VLPC [7] (6.5 K).

From Dolgoshein et al.                                       From Paul Hink (Burle-Photonis)

MCP: Gain fluctuations in the pores: “noise” as loss of energy information

Detailed analysis from Alla Shymanska (Auckland University of Technology, New Zealand) See below

Jean-Francois Genat, Large Area Picosecond Photo-Detectors Electronics, Clermont-Ferrand, January 28th 2010
Outline

• Micro-Channel Plate devices
• MCP signals
• Origin of noise
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• Conclusion
Usually, the internal background count, or dark noise, in the current generation of MCPs is uniformly distributed across the plate with a value of 0.2 cts/sec/sq-cm. This is rather high compared to rates seen in the most commonly used proportional counters. However, it is more indicative of the sophistication of scintillator rejection techniques and the ignorance of MCP noise than any intrinsic behavior. Also, contamination by potassium and rubidium cause the background to be higher in MCPs. Better manufacturing will therefore lead to reductions in the dark noise.

Gain fluctuations (pic SiPM)
Heejong
Matt’s pulses
Noise

Usually, the internal background count, or dark noise, in the current generation of MCPs is uniformly distributed across the plate with a value of 0.2 cts/sec/sq-cm. This is rather high compared to rates seen in the most commonly used proportional counters. However, it is more indicative of the sophistication of scintillator rejection techniques and the ignorance of MCP noise than any intrinsic behavior. Also, contamination by potassium and rubidium cause the background to be higher in MCPs. Better manufacturing will therefore lead to reductions in the dark noise.
Impulse Noise

Property of the glass:

Understood as contamination from Potassium and Rubidium

Siegmund, O.H.W.; Vallerga, J.; Wargelin, B.
Nuclear Science, IEEE Transactions on
Volume 35, Issue 1, Feb 1988 Page(s): 524 - 528
Gain fluctuations

Statistical nature of the amplification process: SEE, number of bounces

Valentin Ivanov
Zeke Insepov

Alla Shymanska

Mathematical and Computer Simulations of Stochastic Processes of Electron Multiplication.

*School of Computing and Mathematical Sciences,\nAuckland University of Technology, Private Bag 92006, Auckland 1142, New Zealand*

Abstract

This paper is devoted to a theoretical investigation of stochastic processes of an electron multiplication. The developed method is based on Monte Carlo simulations and theorems about series and parallel amplification stages proposed here. Splitting a stochastic process into a number of different stages, enables a contribution of each stage to the entire process to be easily investigated. In such approach, Monte Carlo simulations are used only once for one simple stage. The use of the theorems provides a high calculation accuracy with minimal cost of computations. The method is especially efficient for optimization problems which require computer simulations. In this paper the method is used to investigate the effect of variations in channel diameters on noise characteristics of micro-channel electron multipliers.
Outline

• Micro-Channel Plate devices
• MCP signals
• Origin of noise
• Measurements
• Conclusion
Measured baseline fluctuations and dark counts with Burle-Photonis MCP-PMT's

Jean-Francois Genat and Edward May

Dec 2009 – Jan 2010
Experimental conditions

10 and 25 µm 2” x 2” Burle-Photonis MCP tested

- 25 µm MCP      HV: 1.7-2.0 kV

Signals taken on one anode pad, all other pads grounded:

- 10 µm MCP      HV: 2.2-2.5 kV

Signals taken on one anode pad, all other pads grounded:

Discriminator ORTEC 9327, threshold set at 2.5mV

408nm laser light set at 100 Photo-Electrons
TDS 6154C 18GHz abw from Tek

100ps measured rise time degradation due to wiring.

Jean-Francois Genat, Large Area Picosecond Photo-Detectors Electronics, Clermont-Ferrand, January 28th 2010
Conclusion: At full efficiency (25µm 2000V, 10µm 2400V), dark counts rates are:

- 25Hz (25µm)
- 20Hz (10µm)
Conclusions: Gain is $40\text{mV}/100 = 0.4\text{mV/PE}$ (25µm) at 2100 V
$5\text{mV}/100 = 50\ \mu\text{V/PE}$ (10µm) at 2500V

10µm somewhat faster rise time, longer trailing edge, presumably due to the four anode pads connected together.
MCPs  Efficiency and  Baseline noise

Efficiency plateau and baseline noise (left: 25 µm, right 10 µm)
Plateaux are 250V for both MCPs

10 µm MCP showed double and triple after-pulses (not included in the count rates)
Conclusions

MCP PMTs show signals, baseline fluctuations and dark counts similar to regular Photomultiplier tubes

With:

Faster signals (device is thinner, consequently better timing resolution)

rise-time 250-500ps rise time compared to 500ps-1ns

Less noise compared to “good” PM Tubes:

dark counts 10-100 compared to 100-1000 Hz/cm²

The rise-time does not depend upon amplitude
Timing resolution [5]

\[ \sigma_t = \sigma_x / \frac{dx(t)}{dt} \]

Time spread proportional to 1/rise-time and noise
Micro-Channel Plate signals

Single Photon
16-averaged
Sampling: 18 GS/s

TTS = 10 ps

Time response curves for two models of PMT110 with different MCP pore diameters.

From Photek

11 mm diameter Micro-Channel Plate signal
Signal full bandwidth: 10 GHz

Typical Timing resolution:
Single Photoelectron Time Transit Spread: 10 ps

Data taken at Argonne

2” x 2” Micro-Channel Plate signal
Signal full bandwidth: 2 GHz

30 ps

Jean-Francois Genat, Large Area Picosecond Photo-Detectors Electronics, Clermont-Ferrand, January 28th 2010
25 µm pore MCP signal at the output of a ceramic transmission line
Laser 408nm, 50Ω, no amplification
Response to Pions

Data from the Hadron Tile Calorimeter at LHC-ATLAS

Pion signals have shorter lifetime: shorter signals and faster rise-time

Jean-Francois Genat, Fermilab December 15th 2009
Outline

- Applications of Pico-second Timing
- Micro-Channel Plate devices
- Pico-second electronics and Waveform analysis
- Sampling Electronics
- Pico-second timing SCA in 130nm CMOS technology
- Perspective
## Timing-imaging Devices

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<table>
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<tr>
<th>Feature</th>
<th>Multi-anodes PMTs</th>
<th>Silicon-PMTs</th>
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<tbody>
<tr>
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<td>30%</td>
<td>90%</td>
<td>30%</td>
</tr>
<tr>
<td>Collection Eff.</td>
<td>90%</td>
<td>70%</td>
<td>70%</td>
</tr>
<tr>
<td>Rise-time</td>
<td>0.5-1ns</td>
<td>250ps</td>
<td>50-500ps</td>
</tr>
<tr>
<td>Timing resolution (1PE)</td>
<td>150ps</td>
<td>100ps</td>
<td>20-30ps</td>
</tr>
<tr>
<td>Pixel size</td>
<td>2x2mm²</td>
<td>50x50µm²</td>
<td>1.5x1.5mm²</td>
</tr>
<tr>
<td>Dark counts</td>
<td>1-10Hz</td>
<td>1-10MHz/pixel</td>
<td>1Hz-1 kHz/cm²</td>
</tr>
<tr>
<td>Dead time</td>
<td>5ns</td>
<td>100-500ns</td>
<td>1µs</td>
</tr>
<tr>
<td>Magnetic field</td>
<td>no</td>
<td>yes</td>
<td>15kG</td>
</tr>
<tr>
<td>Radiation hardness</td>
<td></td>
<td></td>
<td>good (a-Si, Al₂O₃)</td>
</tr>
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Jean-Francois Genat, Fermilab December 15th 2009
Timing (and Imaging) Devices
Micro-Channel Plate Detectors [1-3]

Timing Resolution: Single Photo-electron Time Transit Spread:

\[ \sigma_i^2 = \sigma_{1st\, gap}^2 + \sigma_{pore}^2 + \sigma_{2nd\, gap}^2 \]

The thinner the device, the better the Timing Resolution.
MCP Device Simulations: first gap

Monte-Carlo: $10^6$ single photoelectrons events
Simulation of the first gap: photocathode - pores input
Angular distribution: \( \text{asin} \{ \text{rand}[-1,1] \} \)

Gap 2 mm

RMS: 5.05228 ps

5ps contribution to TTS
(20-30ps total measured)

Lionel de Sa

Full device simulations:
Valentin Ivanov
Zeke Insepov
Two-micron space resolution using analog charge division technique

High precision analog measurements.

But integration time = 200ns!

Fig. 4. A profile along a line cut across the MCP pores of Fig. 3. The spatial resolution of the readout is ~2 \( \mu \)m rms, capable of resolving every single MCP pore.
Micro-Channel Plate signals

Single Photon
16-averaged
Sampling: 18 GS/s

TTS= 10ps

From Photek

11 mm diameter Micro-Channel Plate signal
Signal full bandwidth: 10 GHz

Typical Timing resolution:
Single Photoelectron Time Transit Spread: 10ps

Data taken at Argonne

2” x 2” imaging MCP (BURLE/PHOTONIS)

2” x 2” Micro-Channel Plate signal
Signal full bandwidth: 2 GHz

30ps

Jean-Francois Genat, Fermilab December 15th 2009
Delay Line readout  Position resolution

50 PEs

25 µm pore MCP signal at the output of a ceramic transmission line
Laser 408nm, 50Ω, no amplification
## Delay Line readout

### Position resolution

<table>
<thead>
<tr>
<th>HV (kV)</th>
<th>Std time diff (ps)</th>
<th>Std position (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.3</td>
<td>12.8</td>
<td>640</td>
</tr>
<tr>
<td>2.4</td>
<td>2.8</td>
<td>140</td>
</tr>
<tr>
<td>2.5</td>
<td>2.2</td>
<td>110</td>
</tr>
<tr>
<td>2.6</td>
<td>1.95</td>
<td>97</td>
</tr>
</tbody>
</table>

**Oscilloscope**

TDS6154C

Tektronix

Jean-Francois Genat, Fermilab December 15th 2009
Delay Line readout  Position resolution

With Edward May and Eugene Yurtsev  (Argonne)
Delay Line readout  Position resolution

Best result at 158PEs

Position resolution (velocity=8.25ps/mm) :  
- 50PEs  4.26ps  213µm
- 158PEs  1.95ps  97µm
Outline

• Applications of Pico-second Timing
• Micro-Channel Plate devices
• Pico-second electronics and Waveform analysis
• Sampling Electronics
• Pico-second timing SCA in 130nm CMOS technology
• Perspective
Timing resolution [5]

\[ \sigma_t = \sigma_x / \frac{dx(t)}{dt} \]

Time spread proportional to 1/rise-time and noise
**Timing techniques**

**ANALOG**

- **Constant-fraction**
  - Constant fraction
  - Leading edge
  - Leading edge errors

**DIGITAL**

- Sample, digitize,
  - Fit to the known waveform

---

**Multi-threshold**

- Extrapolated time

---

Jean-Francois Genat, Fermilab December 15th 2009
Measure pulse amplitude: threshold at a given fraction a delayed version of the pulse

3-parameter (at least !) technique

- Absolute Threshold
- Fraction threshold
- Delay

Analog delay difficult to integrate (cable in most implementations)
Multi-threshold

Multi-threshold: sample several times over thresholds

Best results:

- Number of thresholds: 4-8
- Thresholds values: equally spaced
- Order of the fit: 2d order optimum
Digital Waveform Analysis

Fit to waveform and derivative templates

Psec Timing and Charge
Methods compared (simulation) [11]

Time resolution vs Number of photo-electrons

Jean-Francois Genat, Fermilab December 15th 2009
Picosecond Digital Electronics for Micro-Channel Plate Detectors

*Store the full detector information as with a digital oscilloscope:*

- Detector + electronics noise >> quantization noise (LSB/√12)
- Sampling frequency > 2 x full Analog Bandwidth (Shannon-Nyquist)

**Ideal approach:**

Digitize on the fly, if the two above conditions can be fulfilled.
If not, loss of precision due to A/D conversion and/or loss of timing information.

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Jean-Francois Genat, Fermilab December 15th 2009
Picosecond Digital Electronics for Micro-Channel Plate Detectors

A/D state of the art:

- 8-bit 1GS/s
- 10-bit 300 MS/s
- 16-bit 160 MS/s

Need at least 5 GS/s sampling rate, 10-12 bit
There is no!

Fast analog storage

and slower digitization, if rate allows, or dead-time acceptable

Apply the best timing algorithm suited to the detector, get the charge for free ...!

Jean-Francois Genat, Fermilab December 15th 2009
Fast analog storage [7-9]

Example:

Analog
5 GS/s analog storage,
- Internal Analog buffer
- Use other channels on-chip with a fast input multiplexer

ADC
8-ch 12-bit 80 MS/s (AD9222-80)
Ok up to 2% occupancy
Sampled Micro-Channel Plate signals

Assume: a typical noise at 1mV (detector+system)
LSB set to 1mV for a 1V dynamic range (quantization noise 300µV),
50-200ps rise-time

Fast timing:

10 bit, 2.5-10 GHz full analog bandwidth > 5-20 GS/s sampling rate

Readout electronics

Deep sub-micron CMOS ASICs:

- faster: larger analog bandwidth, sampling rate
- improved radiation hardness
- cheap, 1-10$/ch
- less dynamic range
Outline

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Fast Sampling Electronics

- Integration in custom ASIC for large scale detectors $\sim 10^{4-6}$ channels,
- Self or external trigger,
- Low power,
- Full digital (serial) interface,
- High reliability and availability,
- Low cost.
## Sampling Chips

<table>
<thead>
<tr>
<th>Sampling</th>
<th>Bandwidth</th>
<th>Dyn. range</th>
<th>Depth</th>
<th>PLL</th>
<th>ADC</th>
<th>Trigger</th>
<th>Techno</th>
</tr>
</thead>
<tbody>
<tr>
<td>GS/s</td>
<td>GHz</td>
<td>bits</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>G. Varner (Hawaii) [9]</td>
<td>6</td>
<td>1.0</td>
<td>10</td>
<td>1024</td>
<td>no</td>
<td>12</td>
<td>experience</td>
</tr>
<tr>
<td>S. Ritt (PSI) [8]</td>
<td>6</td>
<td>.8</td>
<td>11.5</td>
<td>256</td>
<td>3.9ps</td>
<td>no</td>
<td>no</td>
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<tr>
<td>D. Breton/E. Delagnes (Orsay/Saclay) [7]</td>
<td>2.5</td>
<td>.5</td>
<td>13.4</td>
<td>250</td>
<td>20ps</td>
<td>no</td>
<td>no</td>
</tr>
</tbody>
</table>

### ASIC Deep Sub-Micron (< 0.13µm) CMOS processes allow today:

- Sampling: 10-20 GHz
- Bandwidth: > 1.5 GHz
- Dyn. Range: 10bit
# Sampling Chips Survey

<table>
<thead>
<tr>
<th></th>
<th>Hawaii</th>
<th>Varner</th>
<th>Saclay/Orsay</th>
<th>Delagnes/Breton</th>
<th>PSI</th>
<th>S.Ritt</th>
<th>This proposal</th>
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<tbody>
<tr>
<td>Blab1</td>
<td>Lab1-2</td>
<td>Lab 3</td>
<td>Hamac</td>
<td>Matacq</td>
<td>Sam</td>
<td>Planned</td>
<td>DRS3</td>
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</table>

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th></th>
<th></th>
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</thead>
<tbody>
<tr>
<td>Sampling</td>
<td>100 MHz-6 GHz</td>
<td>20 MHz-3.7 GHz</td>
<td>40 MHz</td>
<td>0.7-2.5 GHz</td>
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<td>10 GHz</td>
<td>10 MHz-5 GHz</td>
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<td>Bandwidth (3dB)</td>
<td>300 MHz</td>
<td>900 MHz</td>
<td>50 MHz</td>
<td>200-300 MHz</td>
<td>300 MHz</td>
<td>650 MHz</td>
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<tr>
<td>Channels</td>
<td>1</td>
<td>8</td>
<td>9</td>
<td>8</td>
<td>1</td>
<td>2</td>
<td></td>
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<tr>
<td>Triggered mode</td>
<td>Yes</td>
<td>Common stop</td>
<td>Yes</td>
<td>Common stop</td>
<td>Common stop</td>
<td>Channel trigger</td>
<td>8-10-bit</td>
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<tr>
<td>Resolution</td>
<td>10 bit</td>
<td>13.3 bit</td>
<td>13.4 bit</td>
<td>11.6 bit</td>
<td>11.6 bit</td>
<td>11.5 bit</td>
<td></td>
</tr>
<tr>
<td>Samples</td>
<td>128 rows of 512</td>
<td>256</td>
<td></td>
<td>144</td>
<td>2520</td>
<td>256</td>
<td>2048</td>
</tr>
<tr>
<td>Clock</td>
<td>33 MHz</td>
<td>40 MHz</td>
<td>100 MHz</td>
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<td></td>
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<tr>
<td>Max latency</td>
<td>560 us</td>
<td>2.2ms</td>
<td>50us</td>
<td></td>
<td></td>
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<tr>
<td>Input Buffers</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>No</td>
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<tr>
<td>Differential inputs</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
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<tr>
<td>Input impedance</td>
<td>50 Ohms</td>
<td>50 Ohms</td>
<td>50 Ohms Ext</td>
<td>10 MOhm/3pF</td>
<td>50 Ohms</td>
<td></td>
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<tr>
<td>Readout clock</td>
<td>500 MHz</td>
<td></td>
<td></td>
<td>5 MHz</td>
<td>5 MHz</td>
<td>16 MHz</td>
<td>33 MHz</td>
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<tr>
<td>Locked delays</td>
<td>Ext DAC</td>
<td>Ext DAC</td>
<td>Ext DAC</td>
<td>Yes</td>
<td>Ext PLL</td>
<td>Int PLL</td>
<td></td>
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<tr>
<td>On-chip ADC</td>
<td>12-b +500MHz TDC</td>
<td></td>
<td></td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>R/W simultaneous</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Power/ch</td>
<td>15mW/1.6W</td>
<td></td>
<td></td>
<td>36 mW</td>
<td>250-500 mW</td>
<td>150 mW</td>
<td>2.8mW</td>
</tr>
<tr>
<td>Dynamic range</td>
<td>1mV/1V</td>
<td></td>
<td></td>
<td>0.26mV/2.75V</td>
<td>175 uV-2V</td>
<td>0.65mV-2 V</td>
<td>0.35mV/1.1V</td>
</tr>
<tr>
<td>Xtalk</td>
<td>Inter-rows 0.1%</td>
<td>10%</td>
<td></td>
<td>0.30%</td>
<td>&lt; 0.5%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sampling jitter</td>
<td>4.5ps</td>
<td></td>
<td></td>
<td>25ps</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power supplies</td>
<td>-tbd/+2.5V</td>
<td>-tbd/2.5V</td>
<td>-tbd/2.5V</td>
<td>-1.7/3.3V</td>
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<tr>
<td>Process</td>
<td>TSMC 25</td>
<td>TSMC .25</td>
<td>TSMC .25</td>
<td>HP/DMILL .8</td>
<td>AMS .8</td>
<td>AMS .35</td>
<td>AMS .18</td>
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<td>Chip area</td>
<td>5.25 mm2</td>
<td>10 mm2</td>
<td>2.5mm2</td>
<td>19.8mm2</td>
<td>30mm2</td>
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<tr>
<td>Temp coeff</td>
<td>0.2%/°C</td>
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<tr>
<td>Cost/channel</td>
<td>500$/40</td>
<td>10$/2k</td>
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</table>

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55
Existing ASICs: Labrador 3 [9]

Gary Varner
U-Hawaii

250nm CMOS

6.4 ps RMS
(4.5ps single)
Waveform Digitizing Chip DRS4 [8]

- UMC 0.25 µm rad. hard
- 9 chn. each 1024 bins, cascadable up to 8192
- Sampling speed 0.2 ... 5 GS/s
- Bandwidth 950 MHz
- 17.5 mW/chn @ 2.5V
- On-chip PLL stabilization
- Readout speed using ext. ADC: 30 ns * n_samples
- SNR: 69 dB calibrated
- Aperture jitter: 4 ps at 5 GS/s calibrated

250nm CMOS

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The SAM (Swift Analog Memory) ASIC

- 2 differential channels
- 256 cells/channel
- BW > 450 MHz
- Sampling Freq 400MHz->3.2GHz
- High Readout Speed > 16 MHz
- Smart Read pointer
- Few external signals
- Many modes configurable by a serial link.
- Auto-configuration @ power on
- AMS 0.35 µm => low cost for medium size prod

6000 ASICs manufactured, tested and delivered in Q2 2007
Outline

- Applications of Pico-second Timing
- Micro-Channel Plate devices
- Pico-second electronics and Waveform analysis
- Sampling Electronics
- **Pico-second timing SCA in 130nm CMOS technology**
- Perspective
130nm CMOS Sampling ASIC

This chip is developed by U-Chicago and U-Hawaii

It includes

- 4 channels of full sampling (256 cells)
- 1 channel of sampling cell to observe the sampling window

Test structures:

- Sampling cell,
- ADC Comparator,
- Ring Oscillator
Sampling ASIC

- Prototype chip in 130nm CMOS technology (IBM 8RF-DM)
  - 4-channel sampling, >10-15GSa/s
  - 1-2 GHz analog bandwidth, 50 Ohms
  - 40-80 MHz clock
  - 256 cells (<100ps/cell, 12.5-25ns range)
  - Free running delays (no PLL)
  - Sampling window 500ps-2ns
  - Dynamic range .7V
  - Crosstalk <1%
  - On-chip parallel 12-bit ADC (2 µs min conversion time)
  - Free running delays (No PLL)
  - Linearity < 1% on the full dynamic range
  - Read clock up to 50 MHz (one cell/period, 22 µs total readout time)
  - One reference channel (sampling window)
  - 1.2V power supply
  - Power < 40 mW/channel
  - Process IBM 8RF-DM (130nm CMOS)

- 4 x 4 mm²

Chicago-Hawai’i

Sent July 2009, received Oct 21st

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Sequence of operations

-1 **Write:** The timing generator runs continuously, outputs clock phases 100ps spaced. Each phase closes a write switch during one sampling window.

-2 **A/D conversion** after a trigger that opens all the write switches and starts all A/D conversions in parallel. Data available after 2 µs (2GHz counters).

-3 **Read** occurs after conversion (data can still be taken as in Phase 1)
Block diagram

Clock

Timing Generator

Channel # 0 (256 sampling caps + 12-b ADC)

Ch 0
Ch 1
Ch 2
Ch 3

Analog in

Read control

Calibration

Channel #4 (Sampling window)

Digital out

Read

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10 GS/s Timing Generator

40 MHz clock

100ps step delays

256 cells

Sampling window control voltage

To switched capacitor array
Timing Generator
Voltage Controlled Delay Cell

- 256 voltage controlled delay cells of 100-200ps
- 20-40 MHz clock propagated

Voltage Controlled Delay Cell

Test structure:
Ring Oscillator: Two delay cells + inverter
**Sampling Cell**

**Principle**

```
\begin{align*}
\text{"Write" state} & : 3 \text{ dB analog bandwidth is } \frac{1}{2\pi R_{in} C_{storage}} \\
\text{"Sampling window"} & : \text{Number of switches closed } \times \text{ sampling period}
\end{align*}
```

- Thermal $kT/C$ switching noise $= 250\mu V = \text{one 12-bit ADC count}$
Analog bandwidth and Sampling window

**On chip:**

\[ \text{Sampling window} = \text{Number of switches closed at a time} \times \text{sampling period} \]

\[ \text{Sampling Window}_{10^{-3}} = -\log(10^{-3}) \times \text{rise-time} / 2.2 = 1 / 3 \text{ dB Analog Bandwidth} \]

In practice, \( R_{in} \) and \( C_{store} \) are minimum, but limited by the stray capacitor of the switch, and the leakage current of the switch in the open state.

\[ R_{in} = 1.5k\Omega, \quad C_{store} = 70 \text{ fF} \]

3dB Analog Bandwidth = \( 2 \pi R_{in} C_{store} = 1.5 \text{ GHz} \)

\[ \text{Sampling window}_{10^{-3}} > 625 \text{ps} = 7 \text{ samples at 10 GS/s} \]

**Off chip:**

Inductance of the wire bonds and pad capacitance: Bump-bonding

---

*Gary Varner*

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Sampling cell design

Need a voltage buffer to read the small storage capacitor (70fF)

The gate of the source follower transistor is part of the storage capacitor (40+30fF)

\[ V_{out} = V_{in} - V_T - (V_{pol} - V_T) \sqrt{\frac{W}{L} \frac{L_{pol}}{W_{pol}}} \]

Non-linearity < 8/1000
Sampling Capacitance 70fF
Switch resistance: 1.5kΩ
Analog bandwidth 1.5GHz
Wilkinson:

- All cells digitized in one conversion cycle
- Ramp generator
- Comparators
- Counter
- Clocked by the ring oscillator at 1-2 GHz
One sampling cell

One channel

CMOS 130nm   IBM   4 x 4 mm²
Pictures

Received October 21st 2009

Die to be bump-bonded on PCB
Tests

- First tests of packaged chips (presented here)
  - DC power vs biases,
  - Sampling cell response vs input
  - ADC’s comparator
  - Leakages (voltage droop)
  - Digital Readout

- Fine tests to come... (chip is just being bump-bonded to PCB)
  - Analog bandwidth
  - Resolution, signal-to-noise
  - Sampling cell response vs sampling window
  - Crosstalk
  - Max sampling rate
  - Full ADC
  - Linearities, dynamic range, readout speed
Tests: Sampling cell

Ok, except a saturation for voltage inputs > 750 mV
Very close to simulation
Tests: Sampling cell Leakages

1 - input LOW, write switch CLOSED
2 - input HI, switch CLOSED
3 - input HI, switch OPEN
4 - input LOW, switch OPEN

Leakage current is 7 pA
Much smaller than in simulation
Tests: Ring Oscillator

- Measured up to 1.5 GHz
- Observation limited by the 12 bit down-counter
- Can presumably run faster internally
Tests: Digital readout

Token passing readout to multiplex the 1024 data words onto the output bus
Tests Summary

Test structures measured as expected from simulations in terms of:

- Dynamic range:
  Sampling cell runs ok within 0-700mV as simulated
- Speed:
  Ring Oscillator up to 1.5 GHz
- Readout logic ok

One problem with I/O pads:
DC path to ground through protection diodes, but I/O’s can be easily overdriven.

Full sampling channels have still to be measured
Next Design

• Measure and fully understand the first version
• Test with actual MCP signals for pico-second timing

• Include:
  
  - Input trigger discriminator
  - Phase lock (Temperature, voltage supply, process)
  - Increase the dynamic range to 1V
  - Improve the analog bandwidth to 2GHz
  - Increase the sampling rate up to 20 GS/s
  - Improve the readout frequency to $8 \times 40 = 320$ MHz

• 130nm CMOS runs at MOSIS: Feb 1\textsuperscript{st}, May 10\textsuperscript{th}
20 GHz Timing generator [12]

40-160 MHz Clock in

0ps

200ps 200ps 200ps

200ps

50ps step delays

250ps

300ps

350ps

To switched capacitor array

32-64 cells

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Perspective

• The 4-channel 130nm CMOS ASIC:
  First tests ok, more test results to come shortly...

• Next chip: Upgrade with channel discriminator, internal PLL, improve analog bandwidth, sample rate, multi-gain input stages (QIE-like)

• Other ASIC design at the University of Chicago:
  An integrated Front-End for the Hadron Tile Calorimeter upgrade at ATLAS
  Include: 3-gain input stage, Integrator, 12-bit ADC

  130nm CMOS OK for these designs so far.

Latest technologies (90nm) are faster, but require multi-gain to cope with the reduced voltage supply range:

  Multi-gain switched capacitor arrays?
References

Thanks for your attention!