Signal and Noise Characterization of MCP-PMT's

Jean-Francois Genat

University of Chicago

Large-Area-Picosecond-Photo-Detectors electronics
for Particle Physics and Medical Imaging

LPC Clermont-Ferrand, January 28th 2010

With the help of

John T. Anderson, Klaus Attenkofer, Mircea Bogdan, Dominique Breton, Gary Drake,
Eric Delagnes, Henry J. Frisch, Herve Grabas, Mary K. Heintz, Edward May, Samuel Meehan,
Eric Oberla, Larry L. Ruckman, Fukun Tang, Gary S. Varner, Jaroslav Va'Vra

and many others…

Introduction

Micro-Channel Plates Signals and Noise Characterization

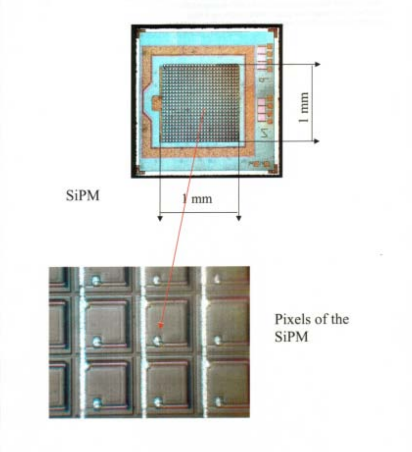
Signals: - The MCP devices are faster than a PMT…

Noise : - The MCP device are very silent…

Timing-Imaging Devices

Multi-anodes PMTs
Dynodes

Silicon-PMTs [10]
Quenched Geiger in Silicon



Micro-Channel Plates [1]
Micro-Pores

Quantum Eff.	30%	90%	30%
Collection Eff.	90%	70%	70%
Rise-time	0.5-1ns	250ps	50-500ps
Timing resolution (1PE)	150ps	100ps	20-30ps
Pixel size	2x2mm^2	50x50μm^2	1.5x1.5mm^2
Dark counts	1-10Hz	1-10MHz/pixel	1Hz-1kHz/cm^2
Dead time	5ns	100-500ns	1μs
Magnetic field	no	yes	15kG
Radiation hardness		1kRad=noisex10	good (a-Si, Al$_2$O$_3$)

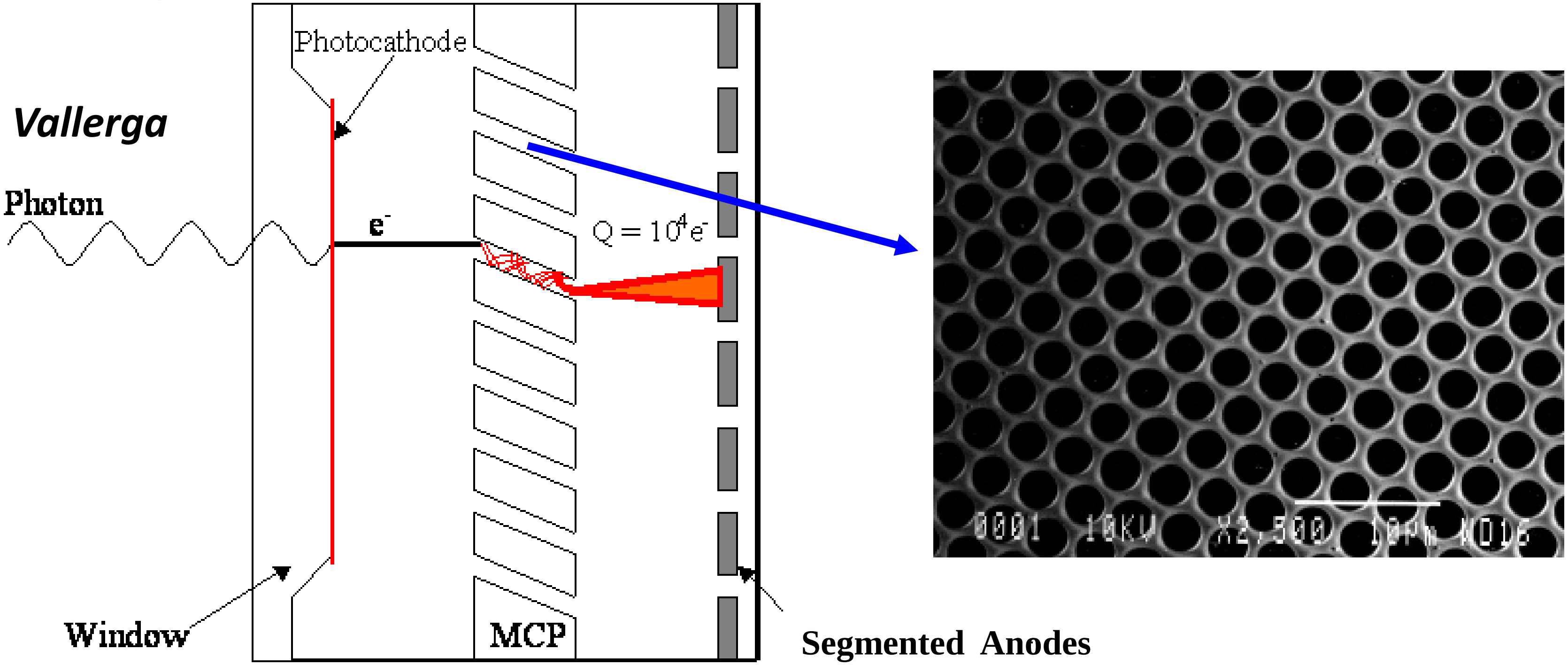
Outline

- Micro-Channel Plate devices
- MCP signals
- Origin of noise
- Measurements
- Conclusion

Timing-Imaging Devices
Micro-Channel Plate Detectors [1-3]

Timing

J. Vallerga



Timing Resolution: Single Photo-electron Time Transit Spread: $\sigma_t^2=\sigma_{1stgap}^2+\sigma_{pore}^2+\sigma_{2ndgap}^2$

The thinner the device, the better the Timing Resolution

Position resolution using analog charge division

R. Bellazzini et al. / Nuclear Instruments and Methods in Physics Research A 591 (2008) 125–128

Position

High precision analog measurements.

But integration time= 200ns

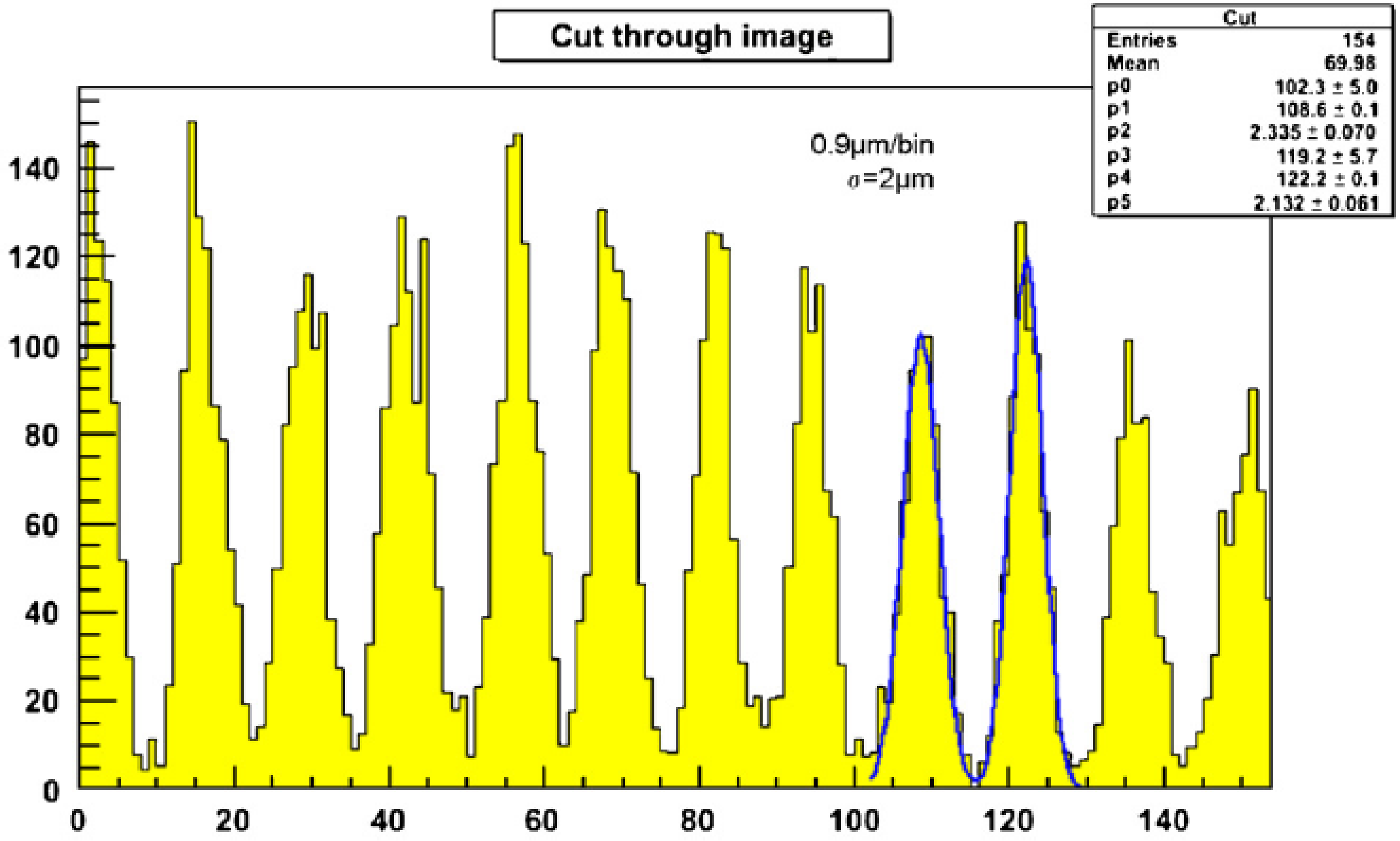


Fig. 4. A profile along a line cut across the MCP pores of Fig. 3. The spatial resolution of the readout is ~2 μm rms, capable of resolving every single MCP pore.

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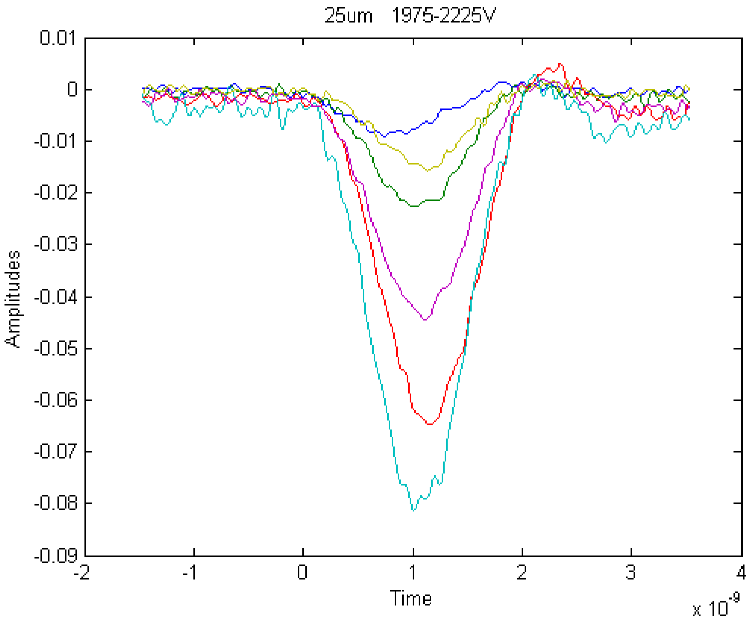
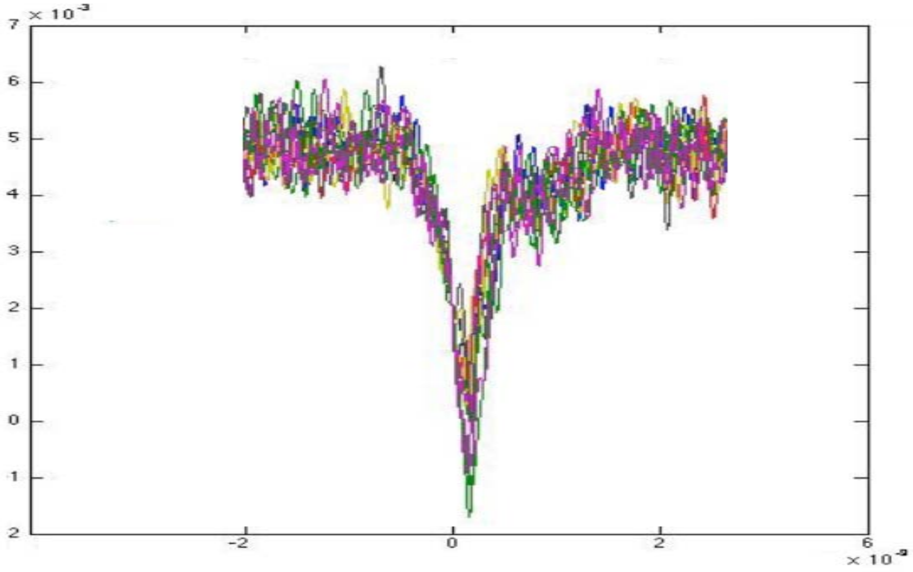
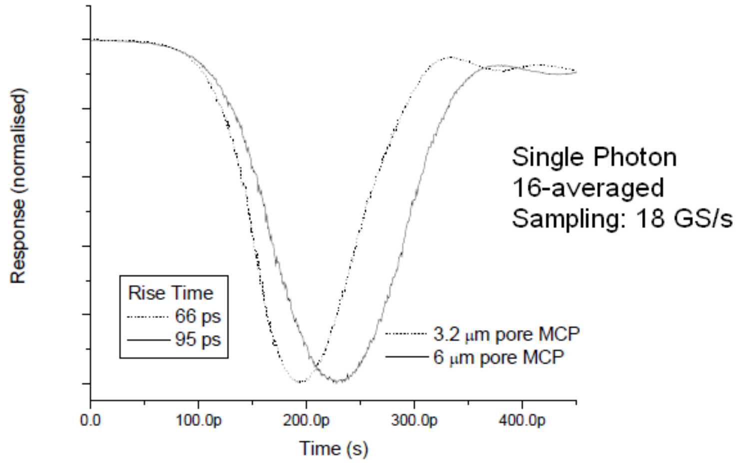
MCP signals



Segmented anodes, Burle-Photonis



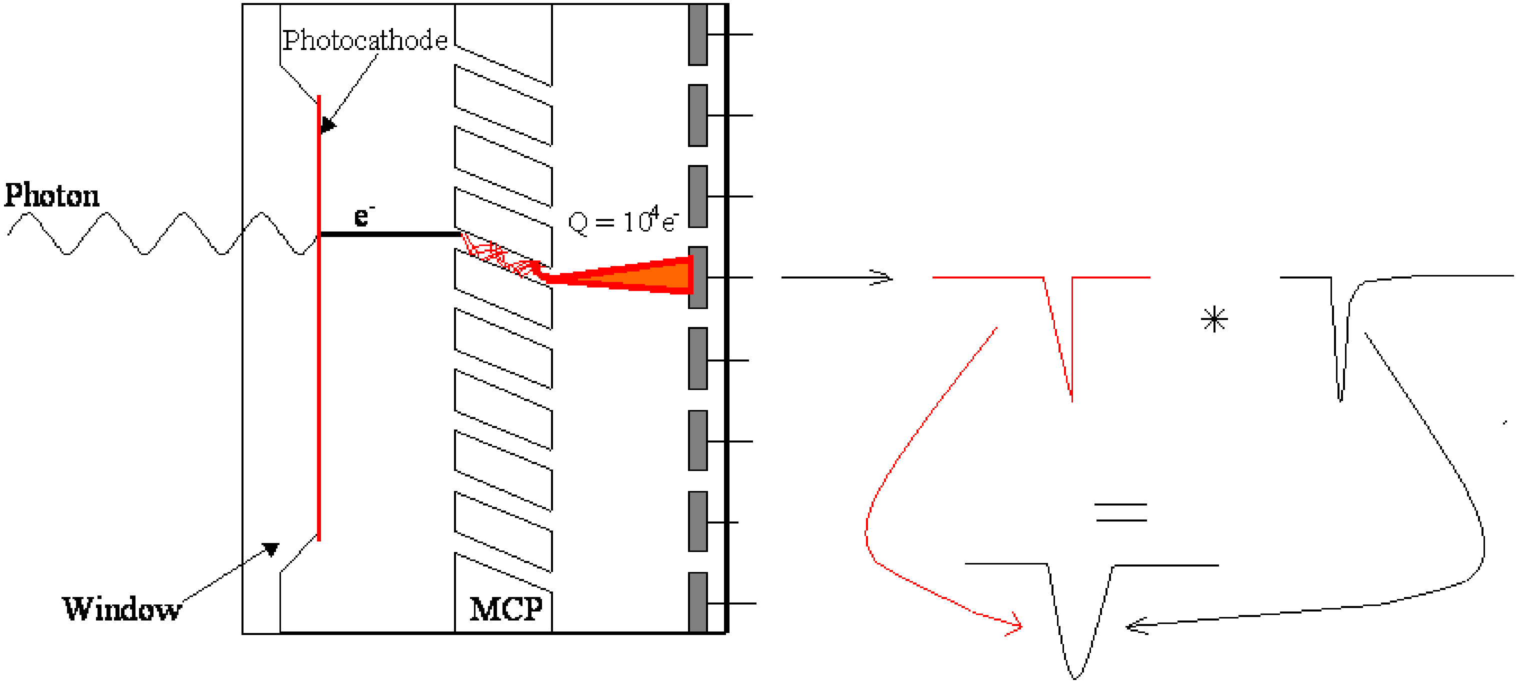
Glass + ALD MCPs (from Matt Wetstein, ANL)



Single Photon
16-averaged
Sampling: 18 GS/s

Time response curves for two models of PMT110 with different MCP pore diameters.

MCPs signal development: pulse



MCP signal rising edge: qE = ma $tr = l\sqrt{2m/qV}$

l = 1mm, E=100V/mm, tr=250ps

Slown down by: RC= 50 Ω . 5pF = 250ps

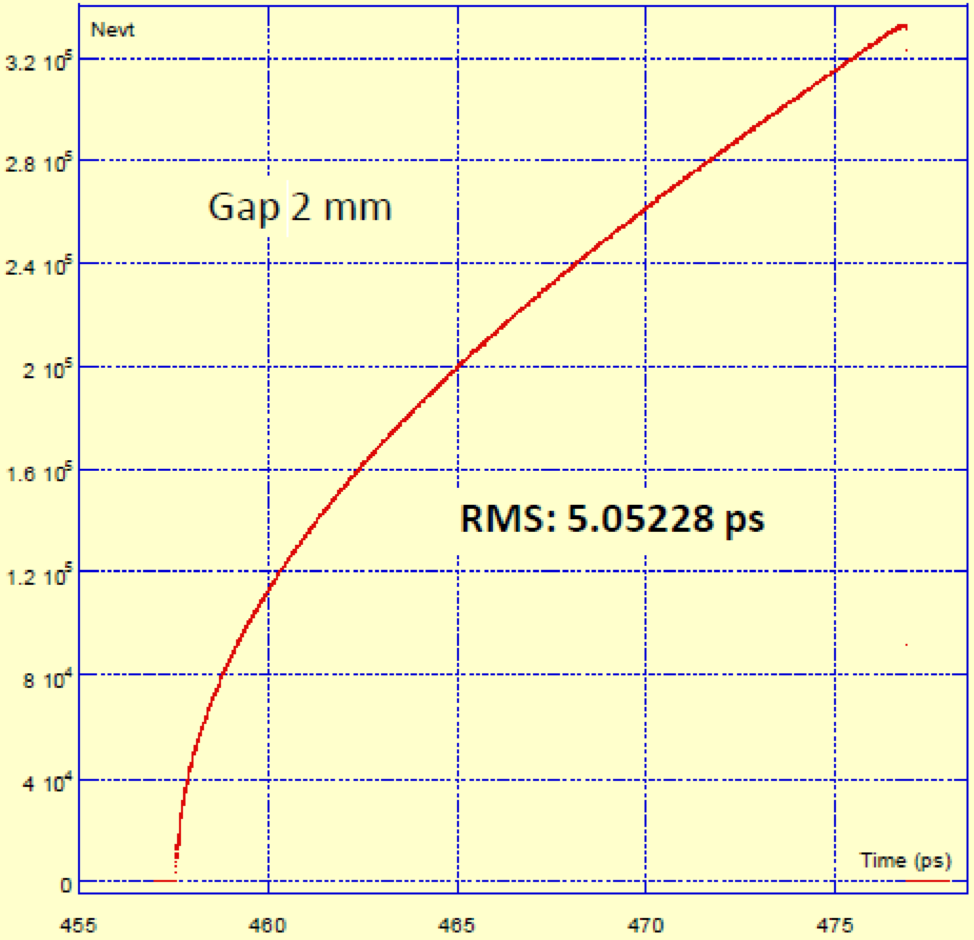
Fast rise-time: thin 2d gap, low LC parasitics

MCP Device Simulations: Photo-cathode gap

Monte-Carlo: 10^6 single photoelectrons events

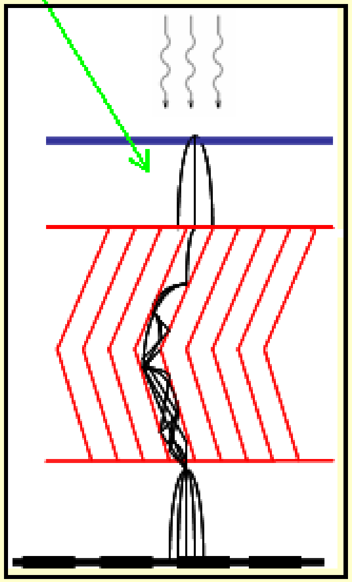
Simulation of the first gap: photocathode - pores input

Angular distribution: asin{rand[-1,+1]}



Gap 2 mm

RMS: 5.05228 ps



5ps contribution to TTS

(20-30ps total measured)

Lionel de Sa

Full device simulations:
Valentin Ivanov
Zeke Insepov

MCP signal development: “shaping”

MCP signal rising edge: qE = ma

l = 1mm, E=200V/mm, tr=250ps

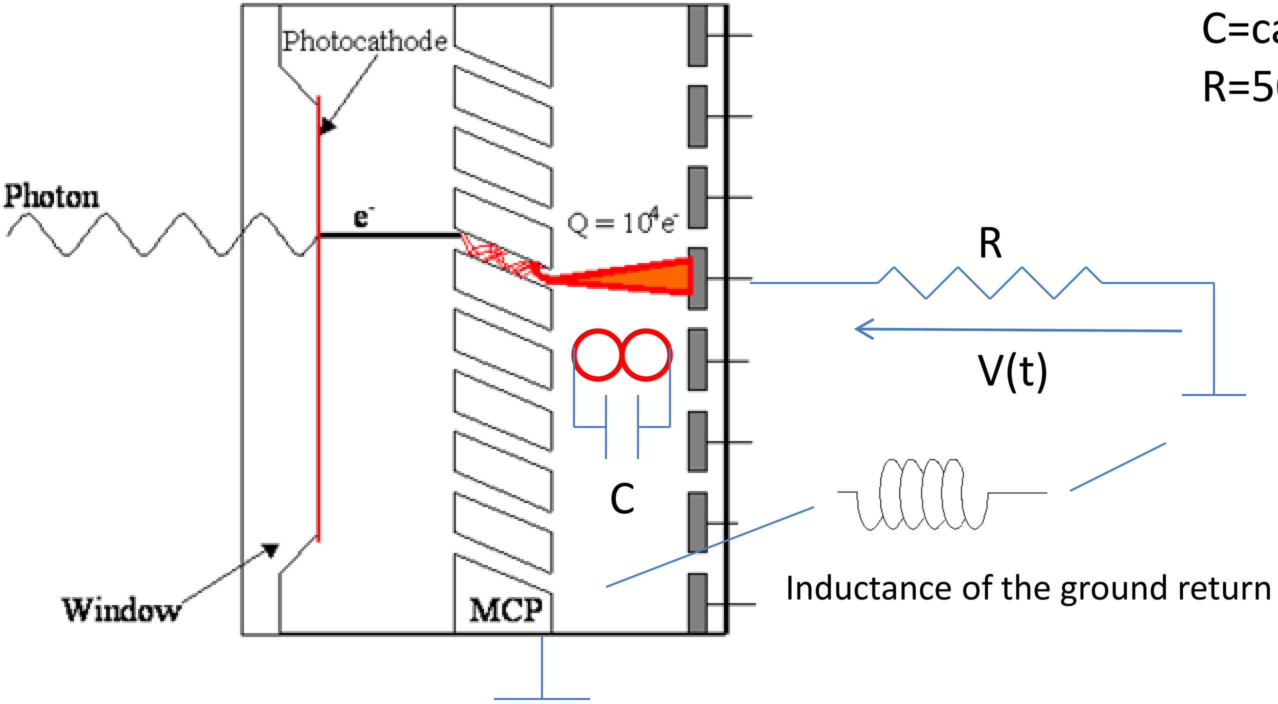
$$tr = l\sqrt{2m/qV}$$

Effect of parasitics:

C=capacitance of the detector

R=50 Ω

$$i_1(t) = i_0 t/(t+RC)$$

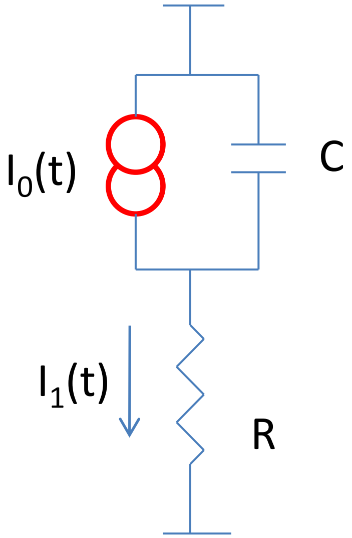


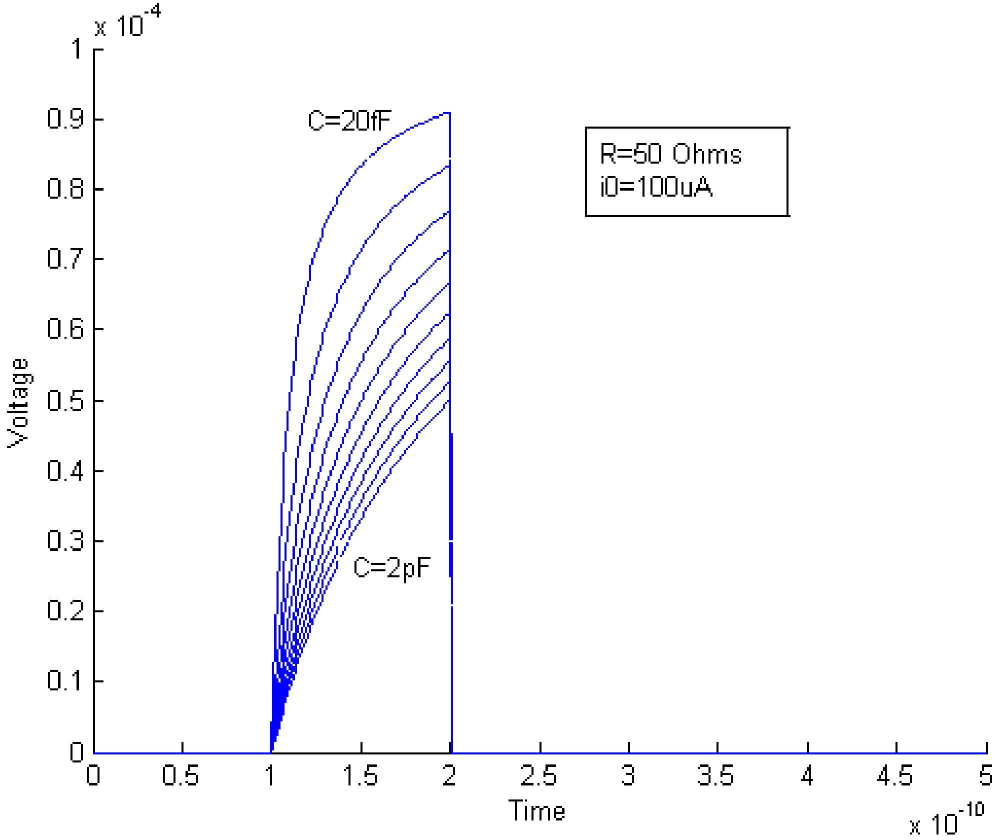
Fast rise-time: thin 2d gap, low LC parasitics

MCP Signal development

Effect of first order passive :

$$i_1(t) = i_0 t / (t + RC)$$





Rise time is RC dependent at first order

Single PE Signals

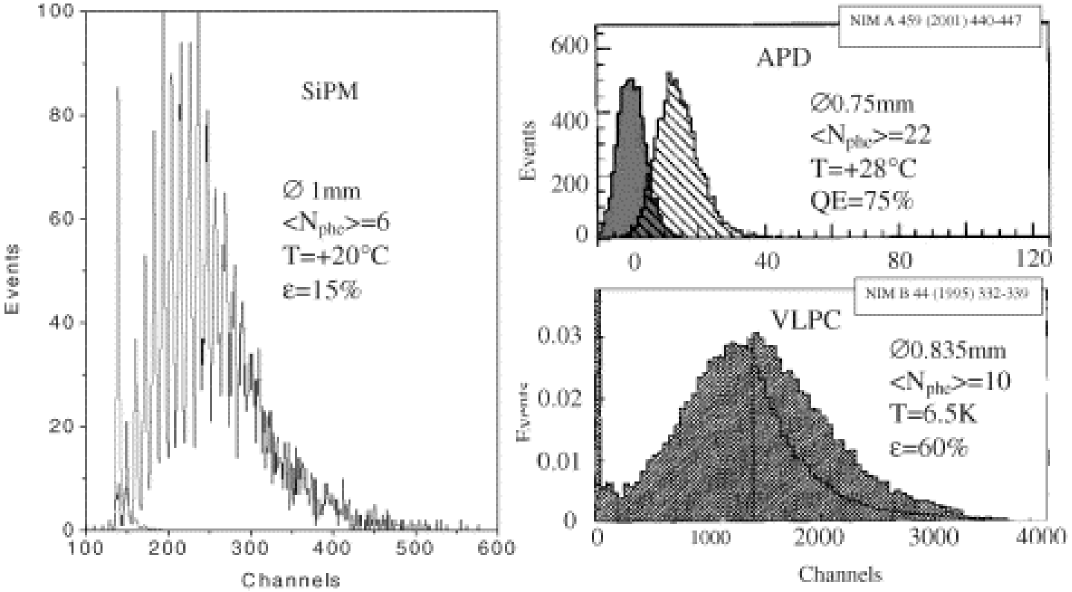
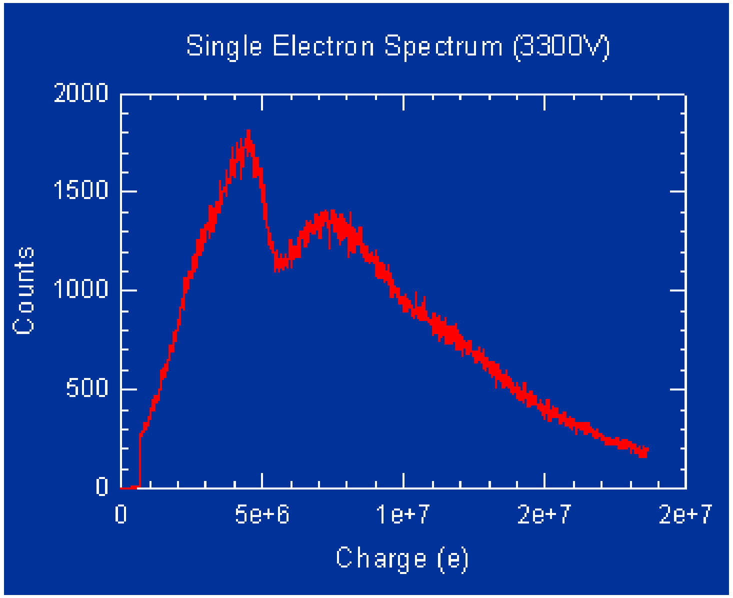


Fig. 3. SiPM application for sci fiber MIP detection (at room temperature): comparison with APD [6] (room temperature) and VLPC [7] (6.5°K).



From Dolgoshein et al.

From Paul Hink (Burle-Photonis)

MCP: Gain fluctuations in the pores: “noise” as loss of energy information

Detailed analysis from Alla Shymanska (*Auckland University of Technology,* New Zealand) See below

Outline

- Micro-Channel Plate devices
- MCP signals
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- Measurements
- Conclusion

Noise

Usually, the internal background count, or dark noise, in the current generation of MCPs is uniformly distributed across the plate with a value of 0.2 cts/sec/sq-cm. This is rather high compared to rates seen in the most commonly used proportional counters. However, it is more indicative of the sophistication of scintillator rejection techniques and the ignorance of MCP noise than any intrinsic behavior. Also, contamination by potassium and rubidium cause the background to be higher in MCPs. Better manufacturing will therefore lead to reductions in the dark noise.

Gain fluctuations (
pic SiPM
Heejong
Matt’s pulses

Noise

Usually, the internal background count, or dark noise, in the current generation of MCPs is uniformly distributed across the plate with a value of 0.2 cts/sec/sq-cm. This is rather high compared to rates seen in the most commonly used proportional counters. However, it is more indicative of the sophistication of scintillator rejection techniques and the ignorance of MCP noise than any intrinsic behavior. Also, contamination by potassium and rubidium cause the background to be higher in MCPs. Better manufacturing will therefore lead to reductions in the dark noise.

Impulse Noise

Property of the glass:

Understood as contamination from Potassium and Rubidium

Siegmund, O.H.W.; Vallerga, J.; Wargelin, B.
Nuclear Science, IEEE Transactions on
Volume 35, Issue 1, Feb 1988 Page(s): 524 - 528

Gain fluctuations

Statistical nature of the amplification process: SEE, number of bounces

Valentin Ivanov
Zeke Insepov

Alla Shymanska

Mathematical and Computer Simulations of Stochastic Processes of Electron Multiplication.

School of Computing and Mathematical Sciences,
Auckland University of Technology, Private Bag 92006, Auckland 1142, New Zealand

Abstract

This paper is devoted to a theoretical investigation of stochastic processes of an electron multiplication. The developed method is based on Monte Carlo simulations and theorems about series and parallel amplification stages proposed here. Splitting a stochastic process into a number of different stages, enables a contribution of each stage to the entire process to be easily investigated. In such approach, Monte Carlo simulations are used only once for one simple stage. The use of the theorems provides a high calculation accuracy with minimal cost of computations. The method is especially efficient for optimization problems which require computer simulations. In this paper the method is used to investigate the effect of variations in channel diameters on noise characteristics of micro-channel electron multipliers.

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Measured baseline fluctuations and dark counts with Burle-Photonis MCP-PMT's

Jean-Francois Genat and Edward May

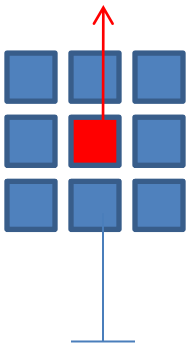
Dec 2009 –Jan 2010

Experimental conditions

10 and 25 μm 2” x 2” Burle-Photonis MCP tested

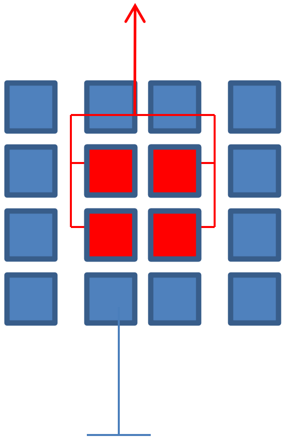
- 25 μm MCP HV: 1.7-2.0 kV

Signals taken on one anode pad, all other pads grounded:



- 10 μm MCP HV: 2.2-2.5 kV

Signals taken on one anode pad, all other pads grounded:

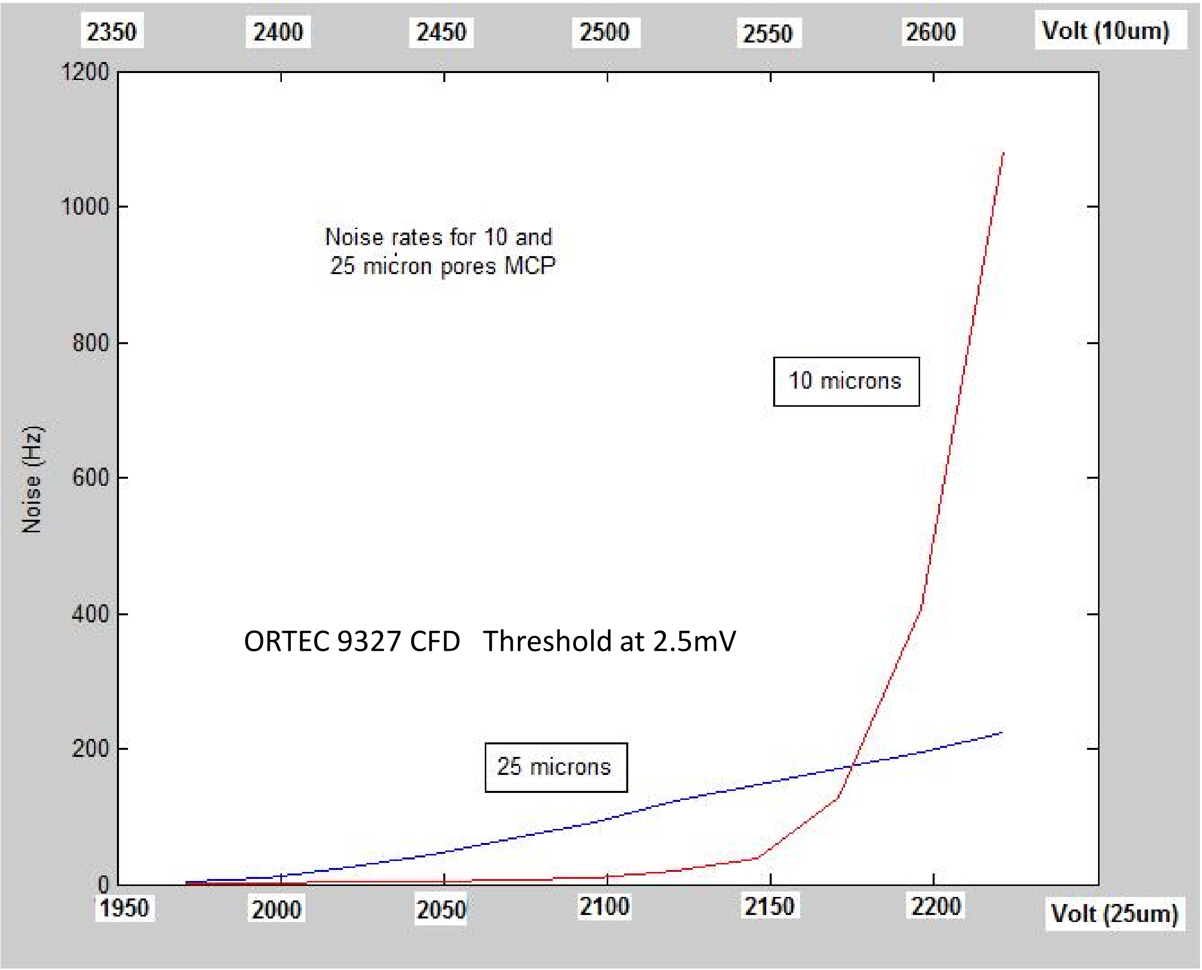


Discriminator ORTEC 9327, threshold set at 2.5mV

408nm laser light set at 100 Photo-Electrons
TDS 6154C 18GHz abw from Tek

100ps measured rise time degradation due to wiring.

Impulse dark noise vs HV

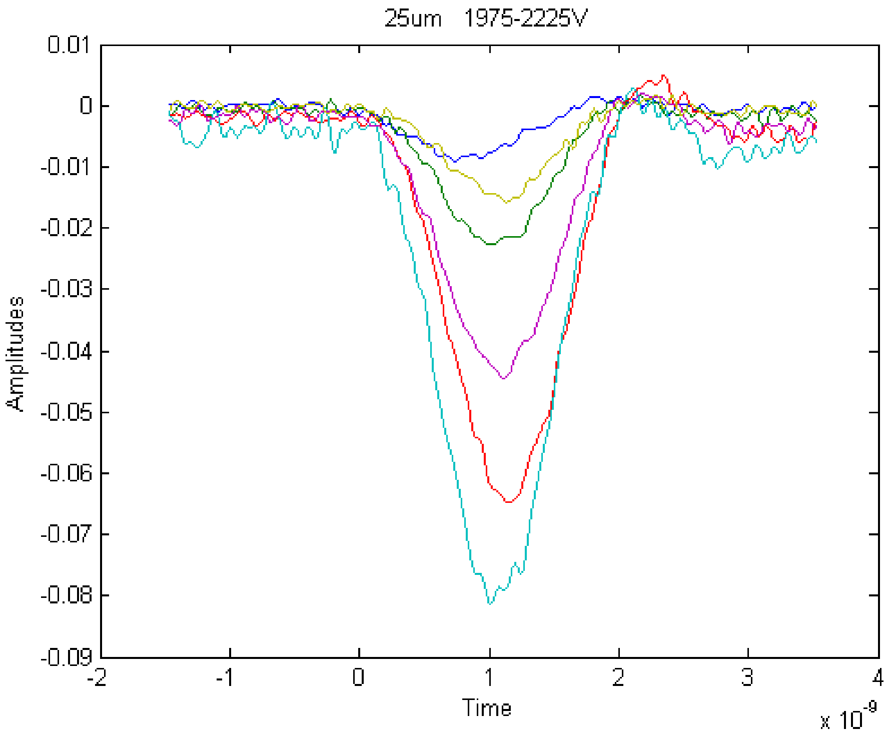


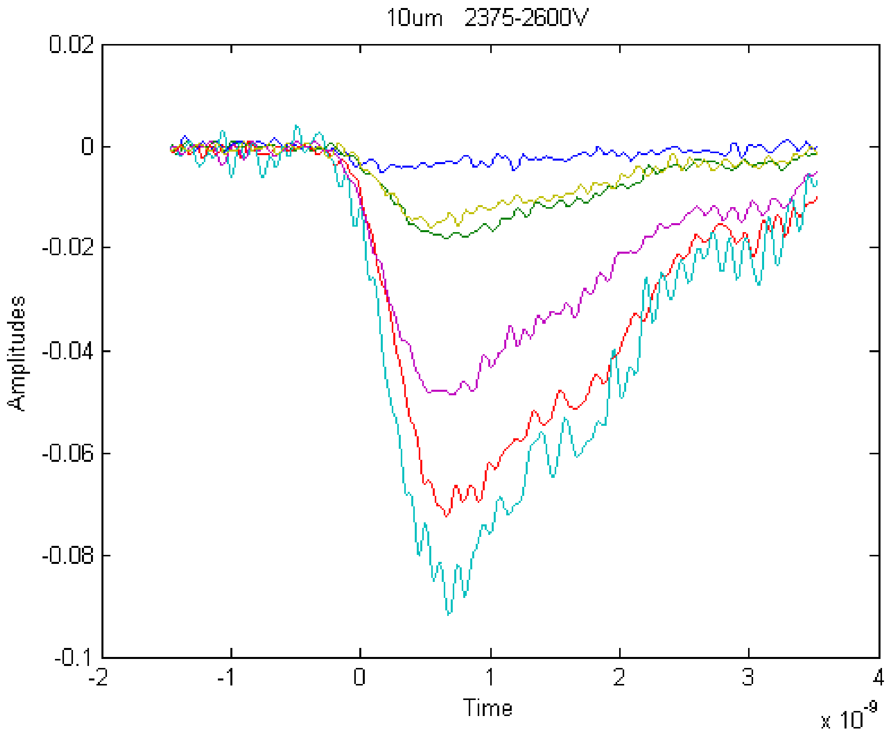
Conclusion: At full efficiency (25µm 2000V, 10µm 2400V), dark counts rates are:

25Hz (25µm)
20Hz (10µm)

Signals

408nm laser
100 Photo-Electrons

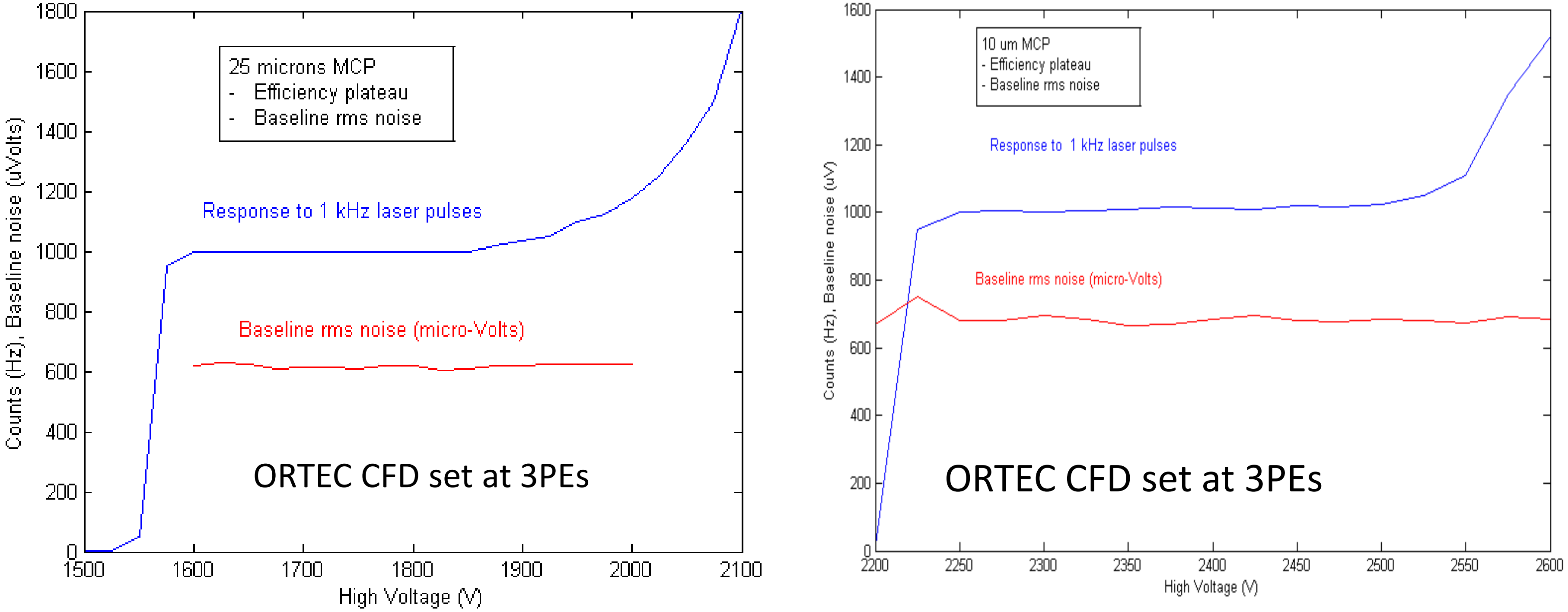




Conclusions: Gain is 40mV/100 = 0.4mV/PE (25μm) at 2100 V
5mV/100 = 50 μV/PE (10μm) at 2500V

10μm somewhat faster rise time, longer trailing edge, presumably due to the four anode pads connected together.

MCPs Efficiency and Baseline noise



Efficiency plateau and baseline noise (left: 25 μm, right 10 μm)
Plateaux are 250V for both MCPs

10 μm MCP showed double and triple after-pulses (not included in the count rates)

Conclusions

MCP PMTs show signals, baseline fluctuations and dark counts similar to regular Photomultiplier tubes

With:

Faster signals (device is thinner, consequently better timing resolution)

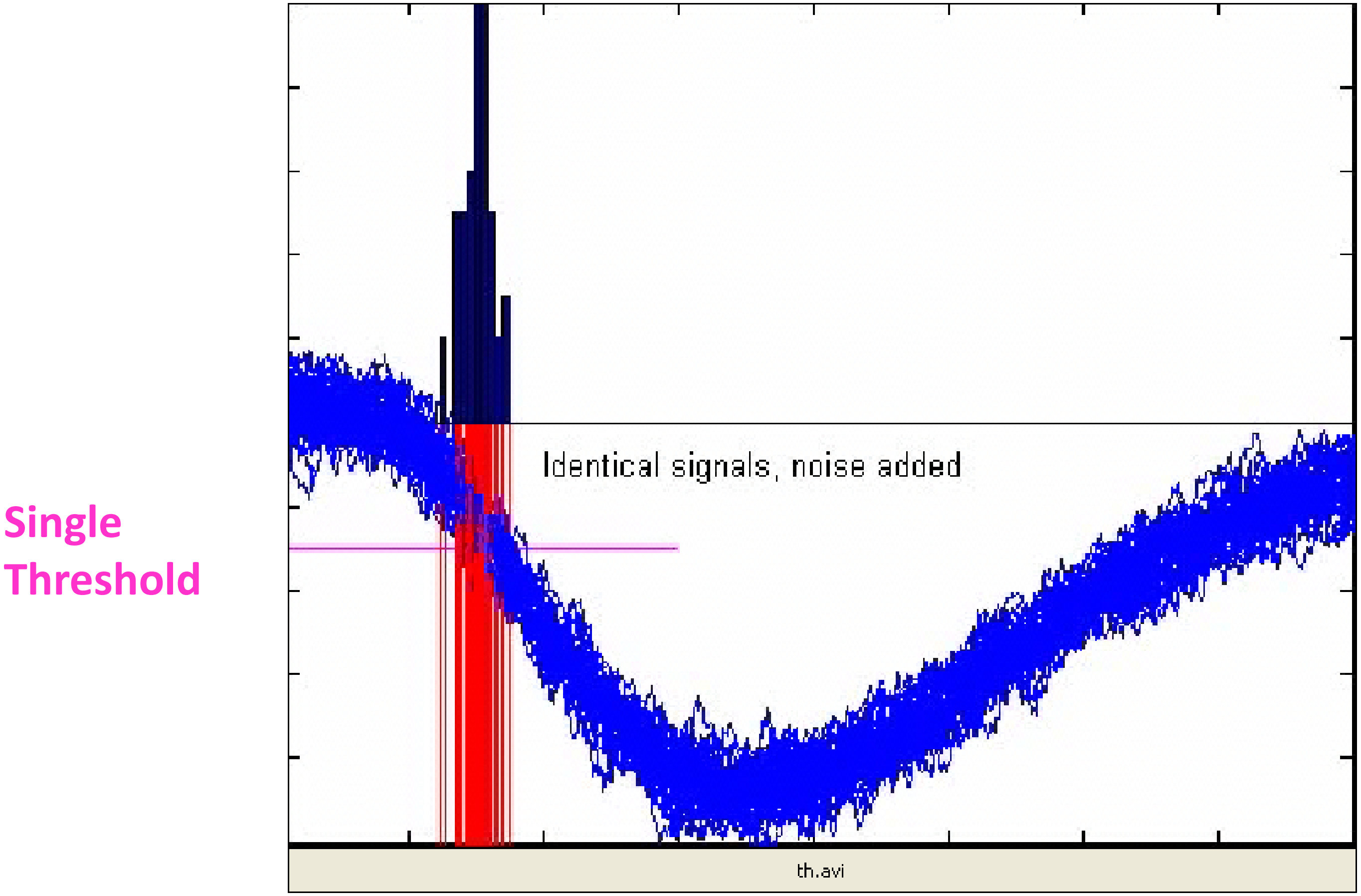
rise-time 250-500ps rise time compared to 500ps-1ns

Less noise compared to “good” PM Tubes:

dark counts 10-100 compared to 100-1000 Hz/cm2

The rise-time does not depend upon amplitude

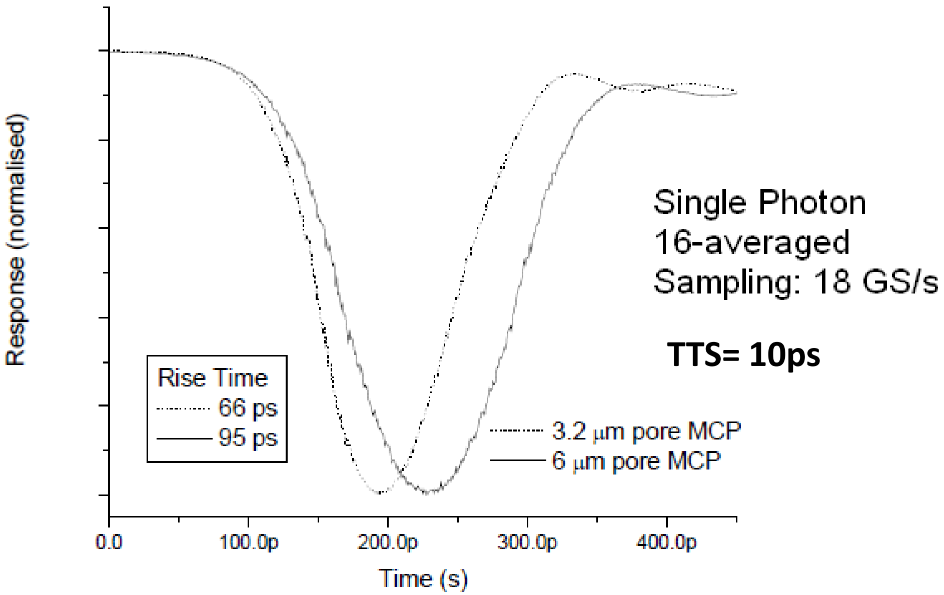
Timing resolution [5]



$$\sigma_t = \sigma_x / \frac{dx(t)}{dt}$$

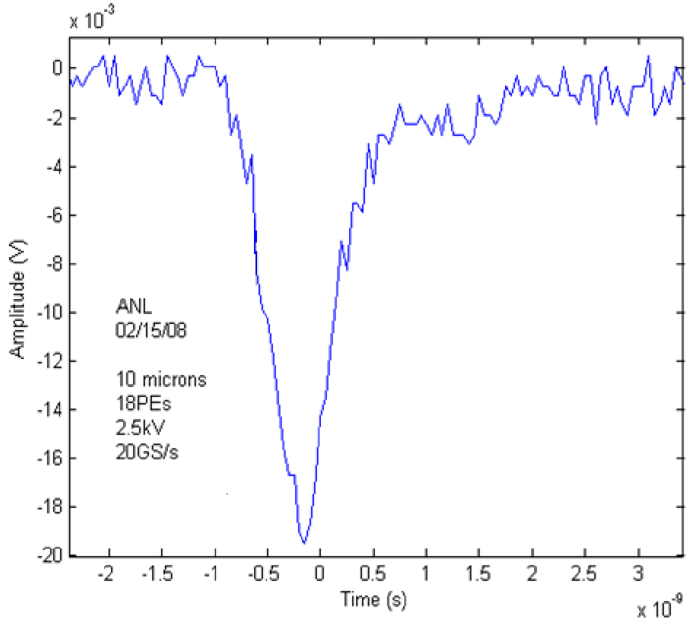
Time spread proportional to 1/rise-time and noise

Micro-Channel Plate signals



TTS= 10ps

Time response curves for two models of PMT110 with different MCP pore diameters.



2” x 2” imaging MCP (BURLE/PHOTONIS)

From Photek

Data taken at Argonne

11 mm diameter Micro-Channel Plate signal
Signal full bandwidth: 10 GHz

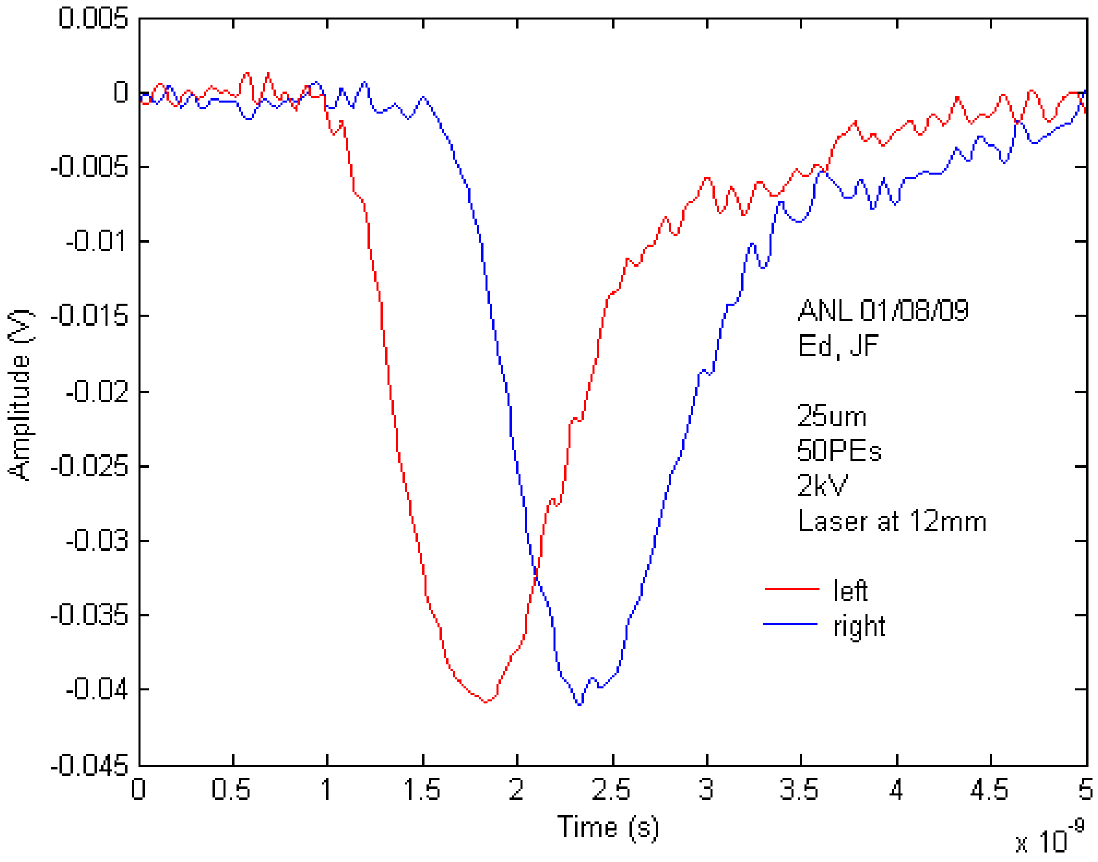
Typical Timing resolution:
Single Photoelectron Time Transit Spread: 10ps

2” x 2” Micro-Channel Plate signal
Signal full bandwidth: 2 GHz

30ps

Delay Line readout Position resolution

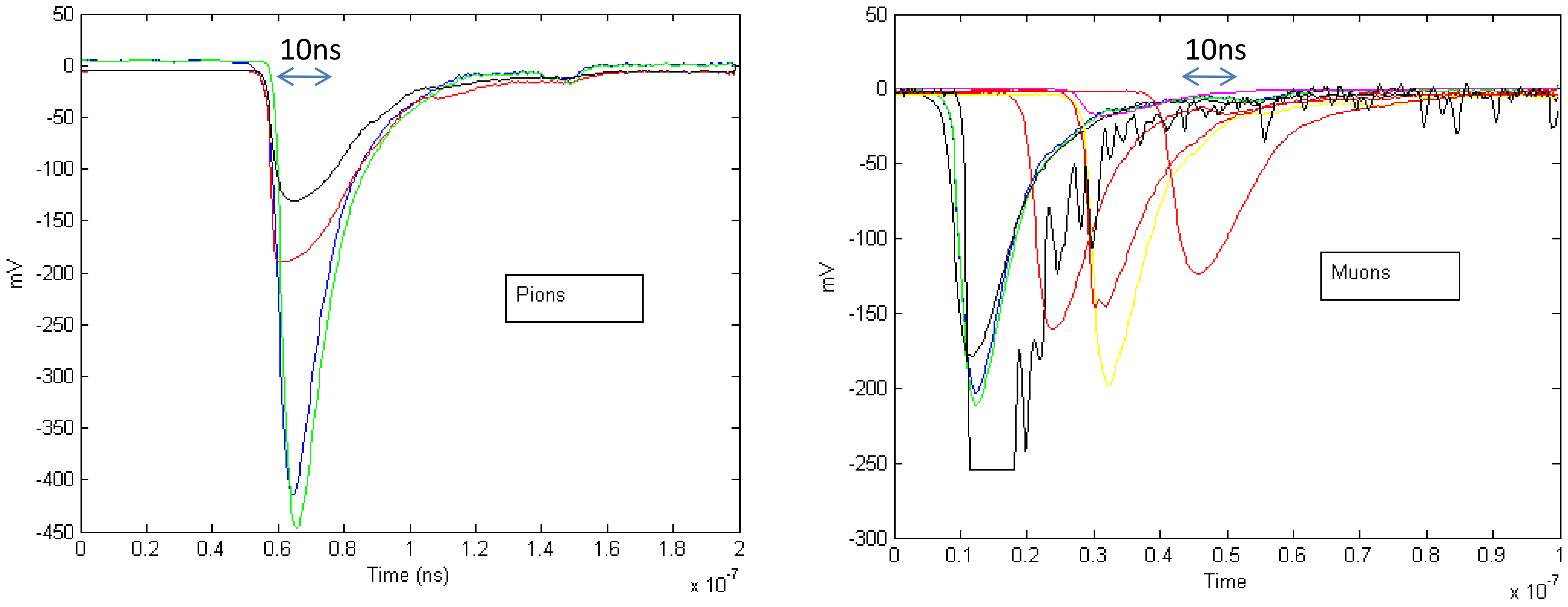
50 PEs



Oscilloscope
TDS6154C
Tektronix

25 μm pore MCP signal at the output of a ceramic transmission line
Laser 408nm, 50Ω, no amplification

Particle ID from Waveform analysis



Response to Pions   *to Muons*

Data from the Hadron Tile Calorimeter at LHC-ATLAS

Pion signals have shorter lifetime: shorter signals and faster rise-time

Outline

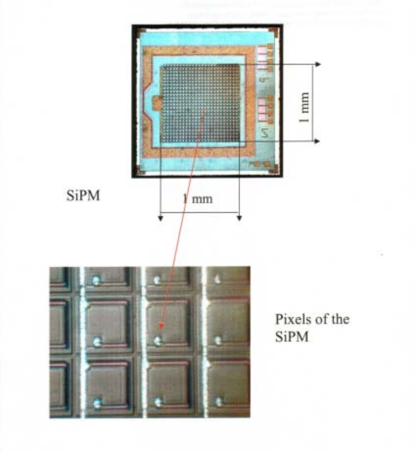
- Applications of Pico-second Timing
- Micro-Channel Plate devices
- Pico-second electronics and Waveform analysis
- Sampling Electronics
- Pico-second timing SCA in 130nm CMOS technology
- Perspective

Timing-imaging Devices

Multi-anodes PMTs
Dynodes

Silicon-PMTs [10]
Quenched Geiger in Silicon

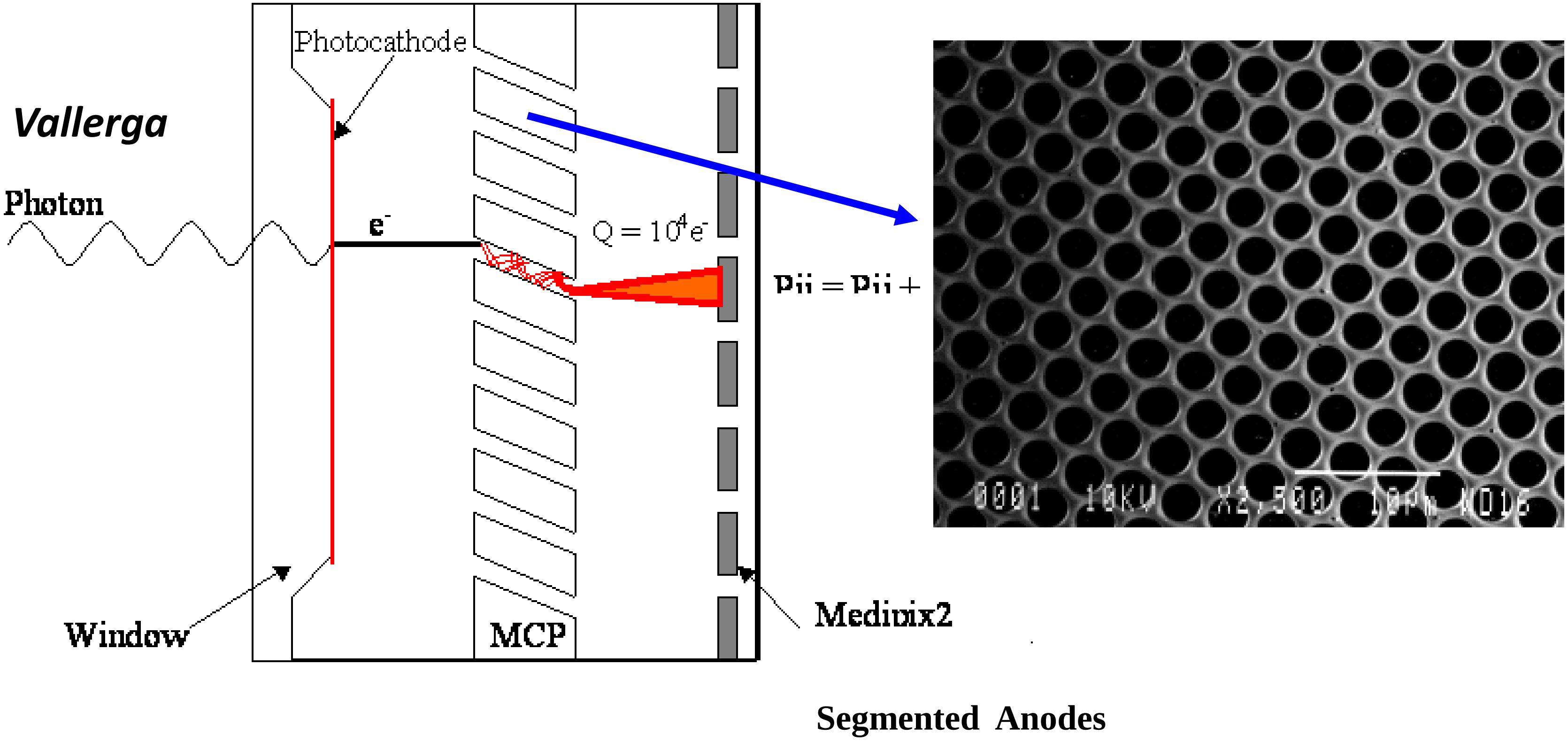
Micro-Channel Plates [1]
Micro-Pores



Quantum Eff.	30%	90%	30%
Collection Eff.	90%	70%	70%
Rise-time	0.5-1ns	250ps	50-500ps
Timing resolution (1PE)	150ps	100ps	20-30ps
Pixel size	$2x2mm^2$	$50x50\mu m^2$	$1.5x1.5mm^2$
Dark counts	1-10Hz	1-10MHz/pixel	$1Hz\text{-}1\ kHz/cm^2$
Dead time	5ns	100-500ns	$1\mu s$
Magnetic field	no	yes	15kG
Radiation hardness		1kRad=noisex10	good (a-Si, Al_2O_3)

Timing (and Imaging) Devices
Micro-Channel Plate Detectors [1-3]

J. Vallerga



Timing Resolution: Single Photo-electronTime Transit Spread: $\sigma_t^2=\sigma_{1stgap}^2+\sigma_{pore}^2+\sigma_{2ndgap}^2$

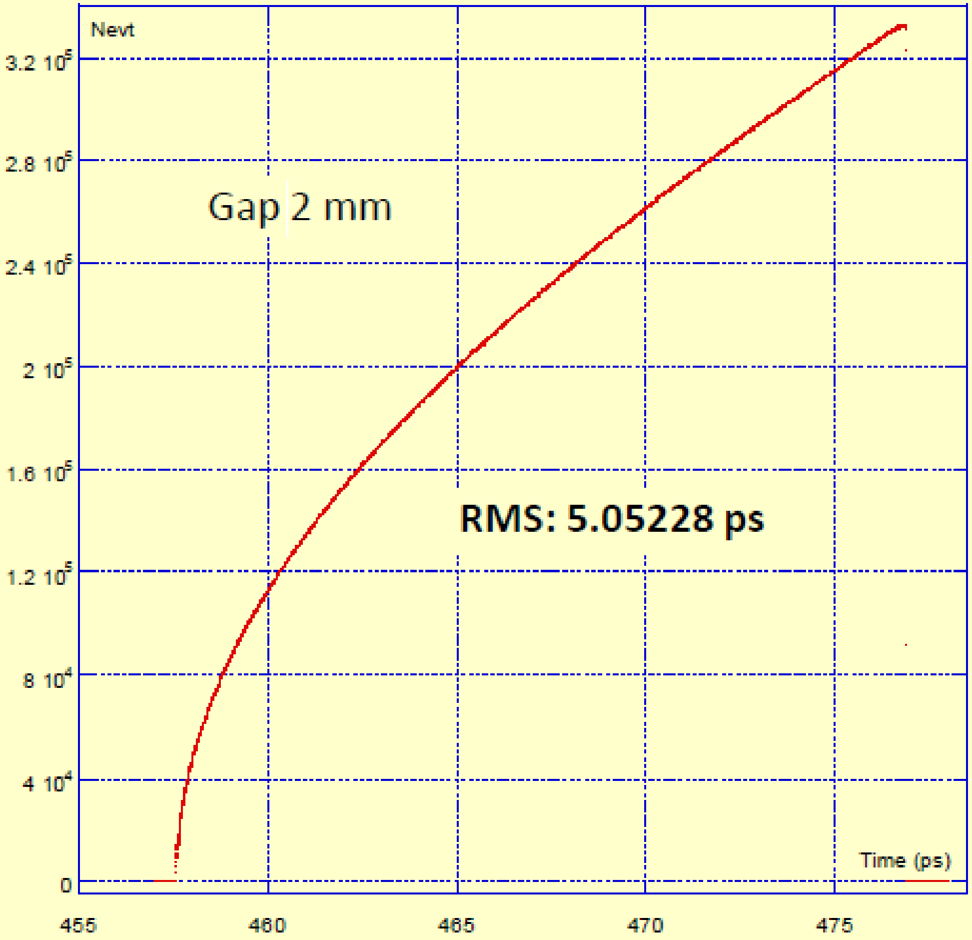
The thinner the device, the better the Timing Resolution

MCP Device Simulations: first gap

Monte-Carlo: 10^6 single photoelectrons events

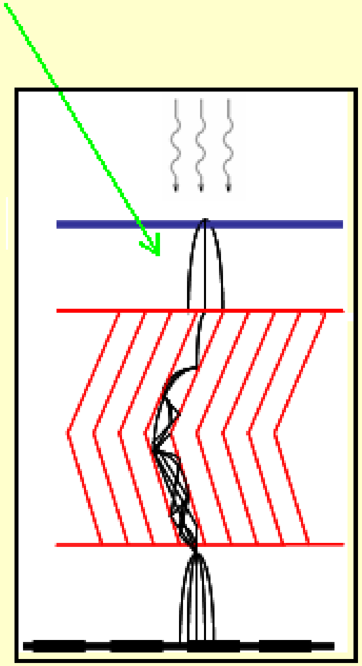
Simulation of the first gap: photocathode - pores input

Angular distribution: asin{rand[-1,+1]}



Gap 2 mm

RMS: 5.05228 ps



5ps contribution to TTS

(20-30ps total measured)

Lionel de Sa

Full device simulations:
Valentin Ivanov
Zeke Insepov

Two-micron space resolution using analog charge division technique

High precision analog measurements.

But integration time= 200ns !

R. Bellazzini et al. / Nuclear Instruments and Methods in Physics Research A 591 (2008) 125–128

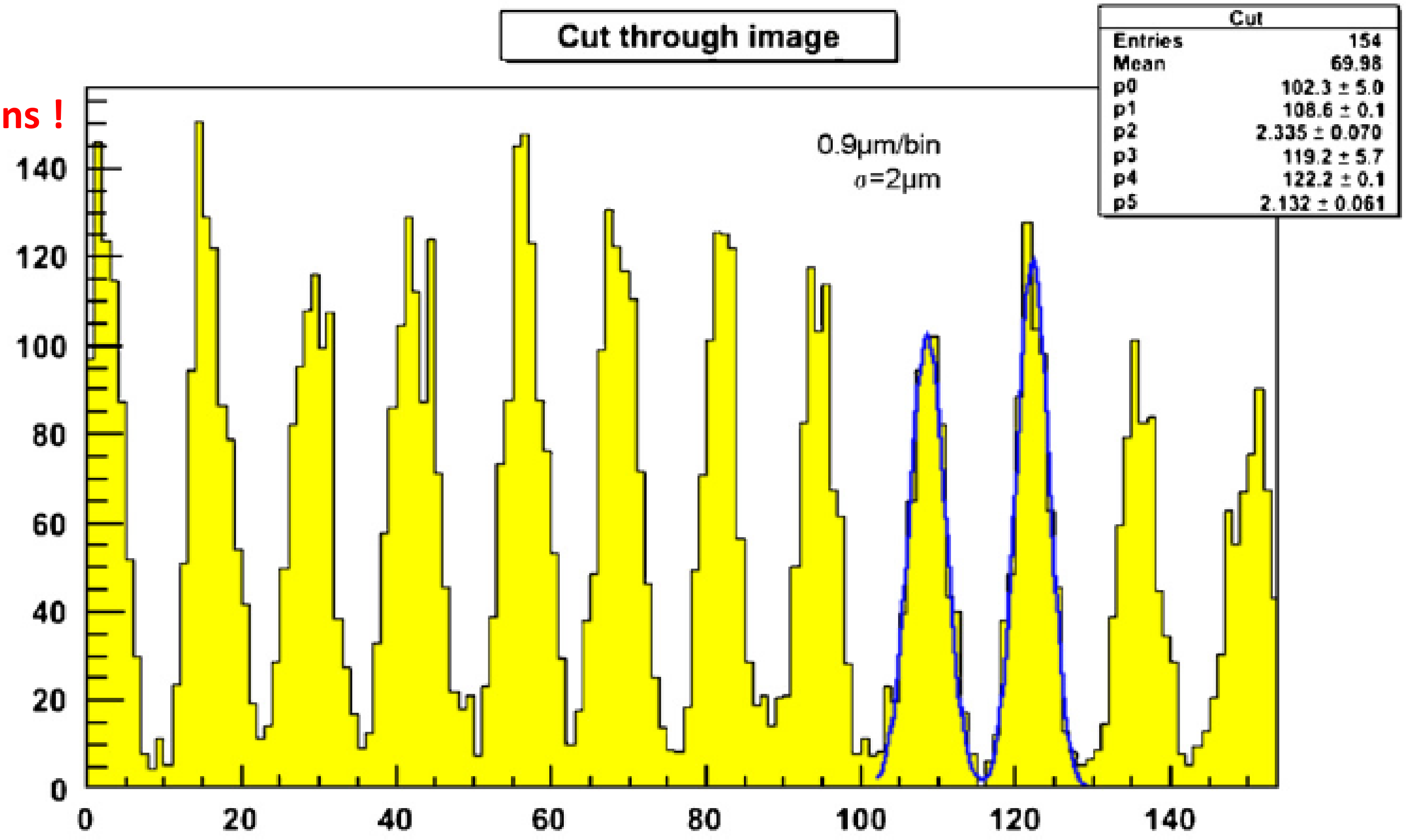
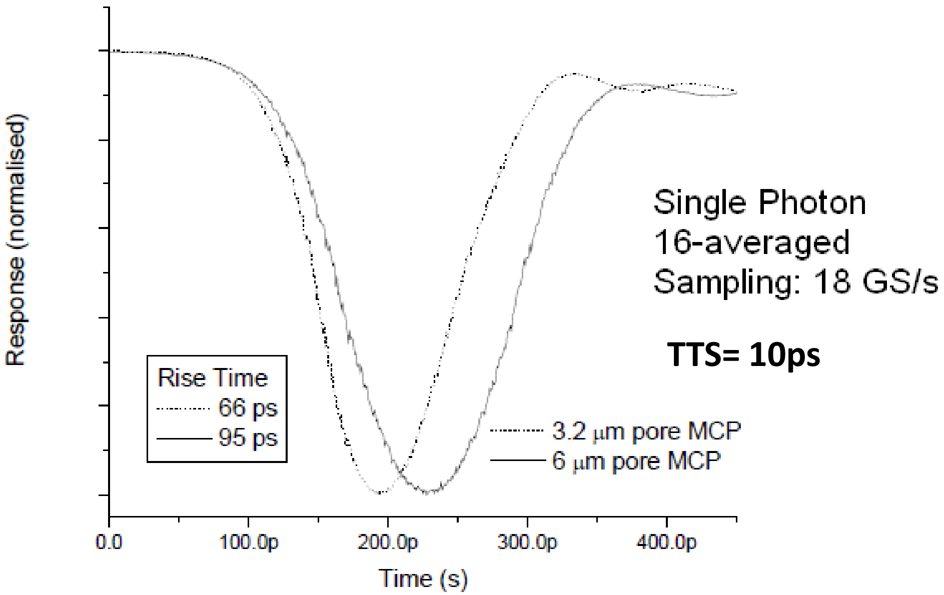


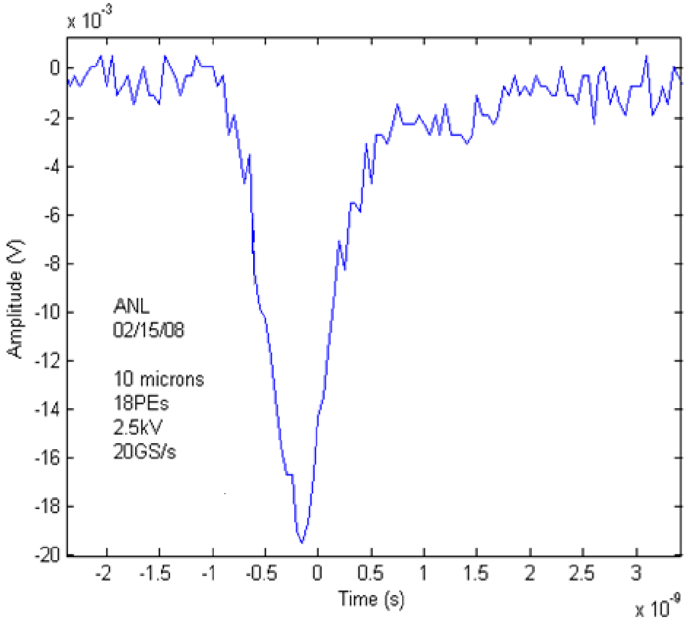
Fig. 4. A profile along a line cut across the MCP pores of Fig. 3. The spatial resolution of the readout is ~2 μm rms, capable of resolving every single MCP pore.

Micro-Channel Plate signals



TTS= 10ps

Time response curves for two models of PMT110 with different MCP pore diameters.



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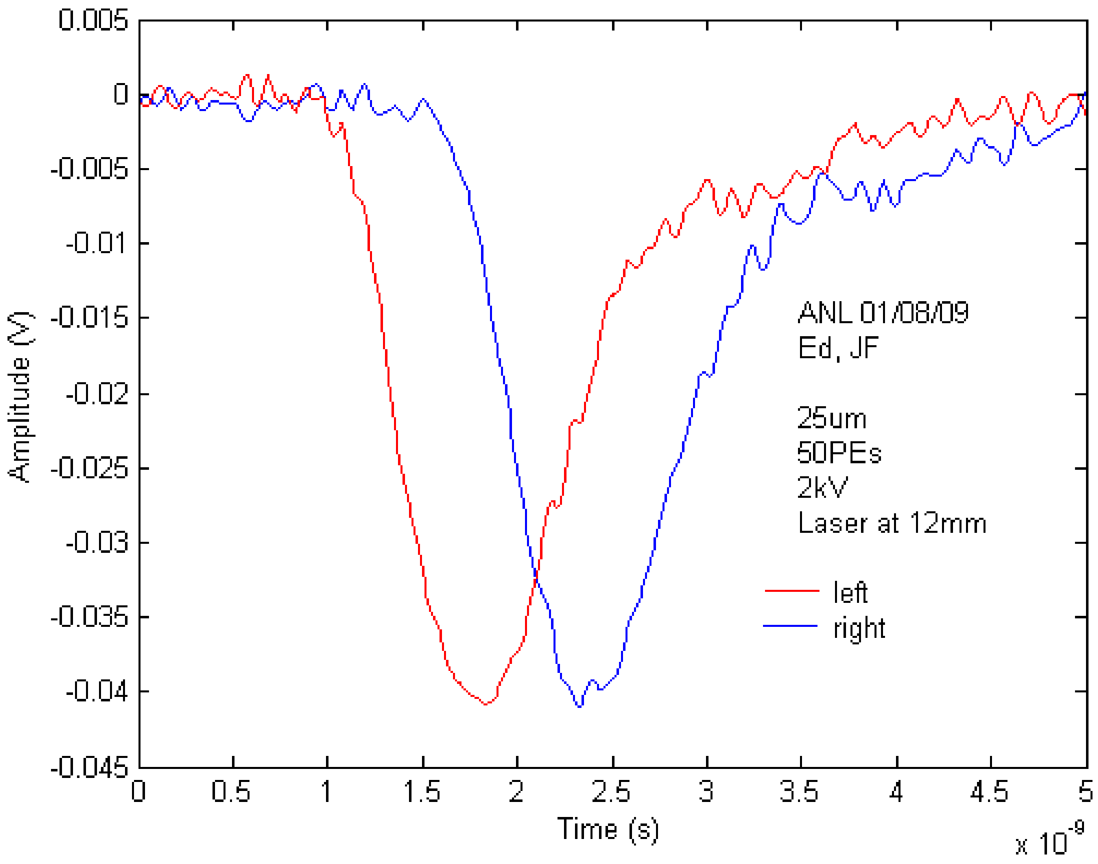
2” x 2” Micro-Channel Plate signal
Signal full bandwidth: 2 GHz

30ps

Delay Line readout   Position resolution

50 PEs



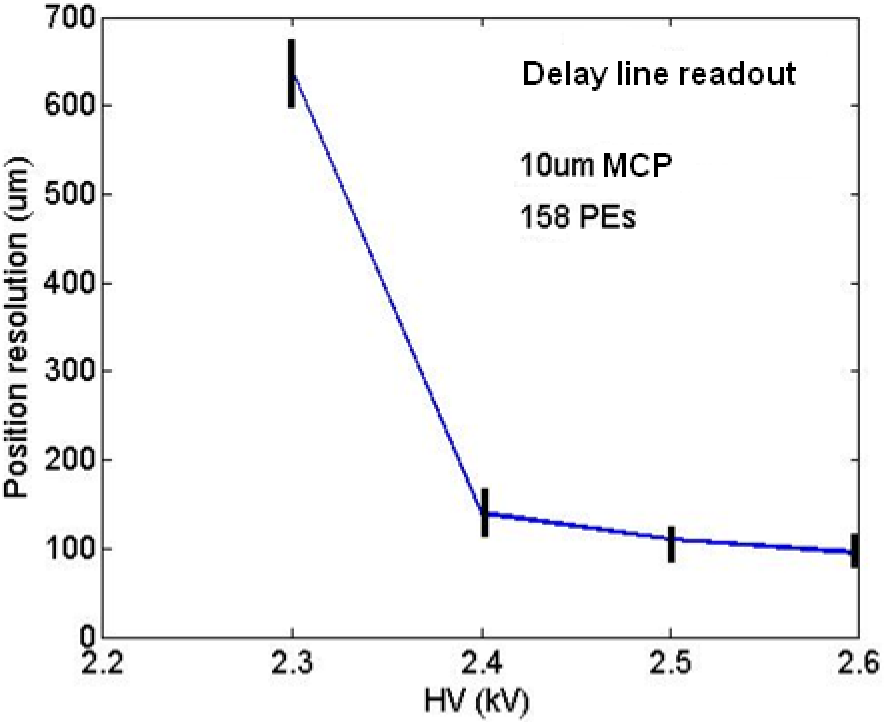
Oscilloscope
TDS6154C
Tektronix

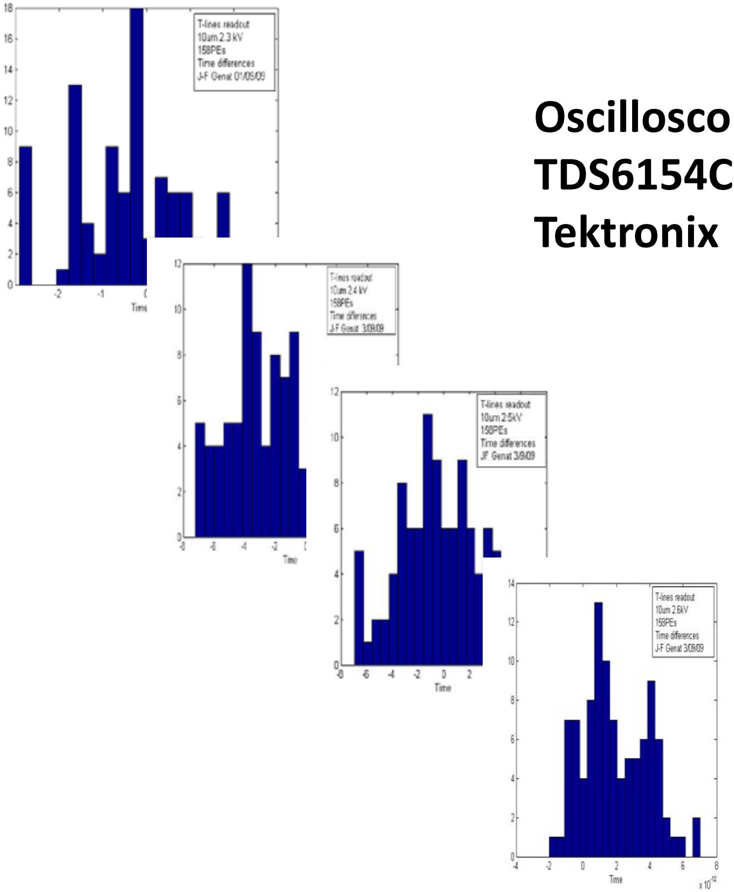
25 µm pore MCP signal at the output of a ceramic transmission line
Laser 408nm, 50Ω, no amplification

Delay Line readout   Position resolution

158 PEs

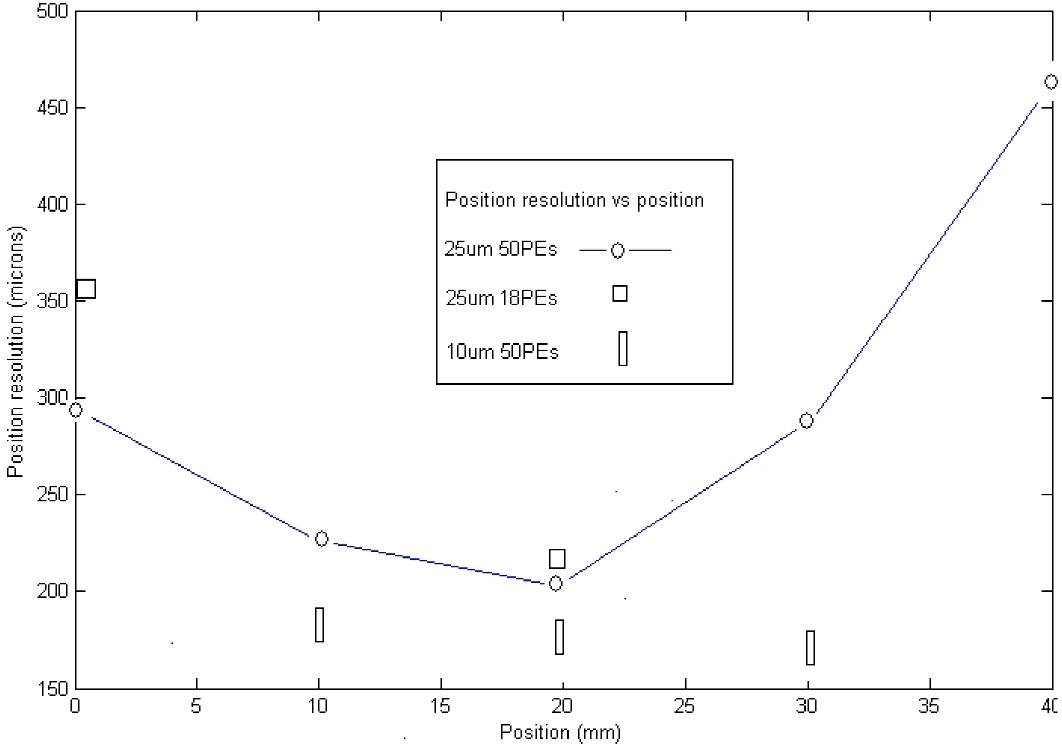
HV	**2.3 kV**	**2.4 kV**	**2.5 kV**	**2.6 kV**
Std time diff	**12.8ps**	**2.8ps**	**2.2 ps**	**1.95 ps**
Std position	**640μm**	**140μm**	**110μm**	**97μm**

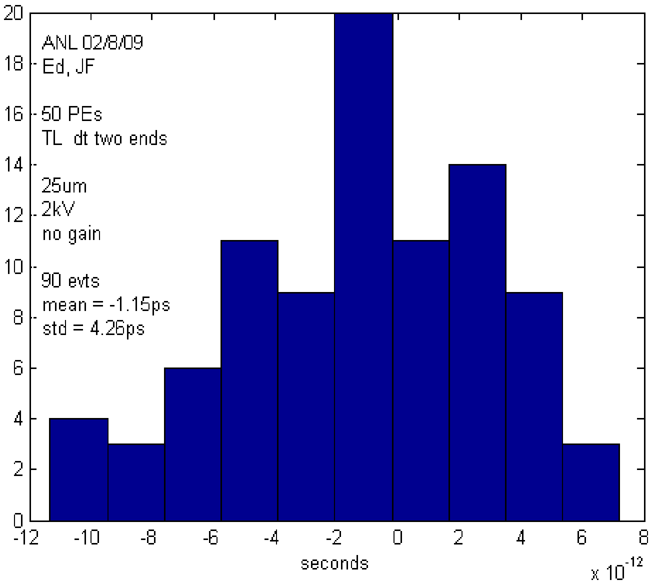




Oscilloscope
TDS6154C
Tektronix

Delay Line readout   Position resolution

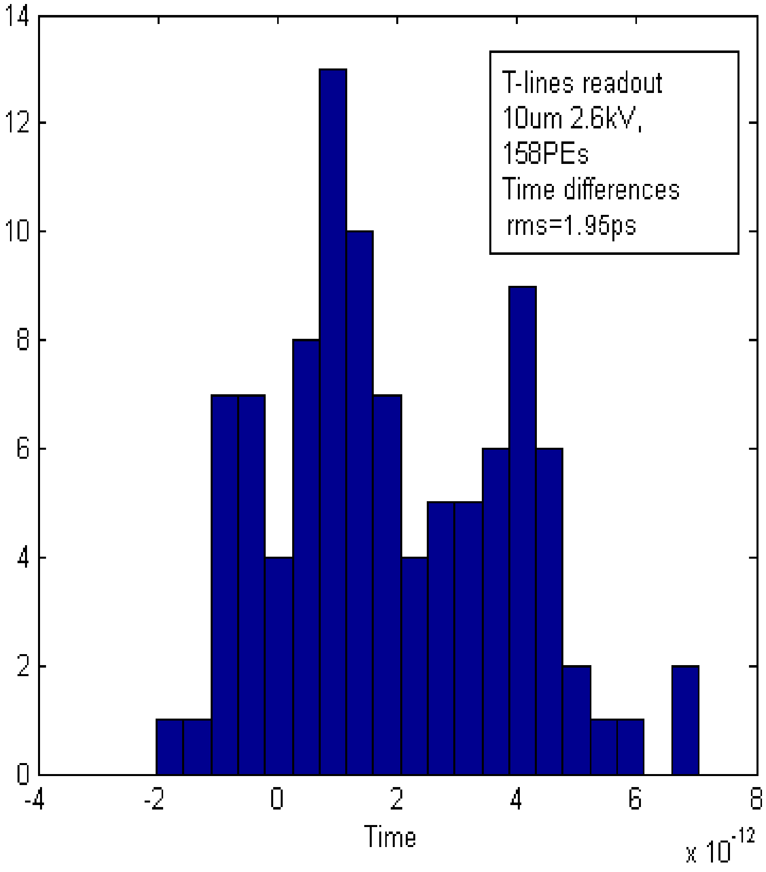




With Edward May and Eugene Yurtsev (Argonne)

Delay Line readout   Position resolution

Best result at 158PEs



Position resolution (velocity=8.25ps/mm) : **50PEs 4.26ps 213µm**

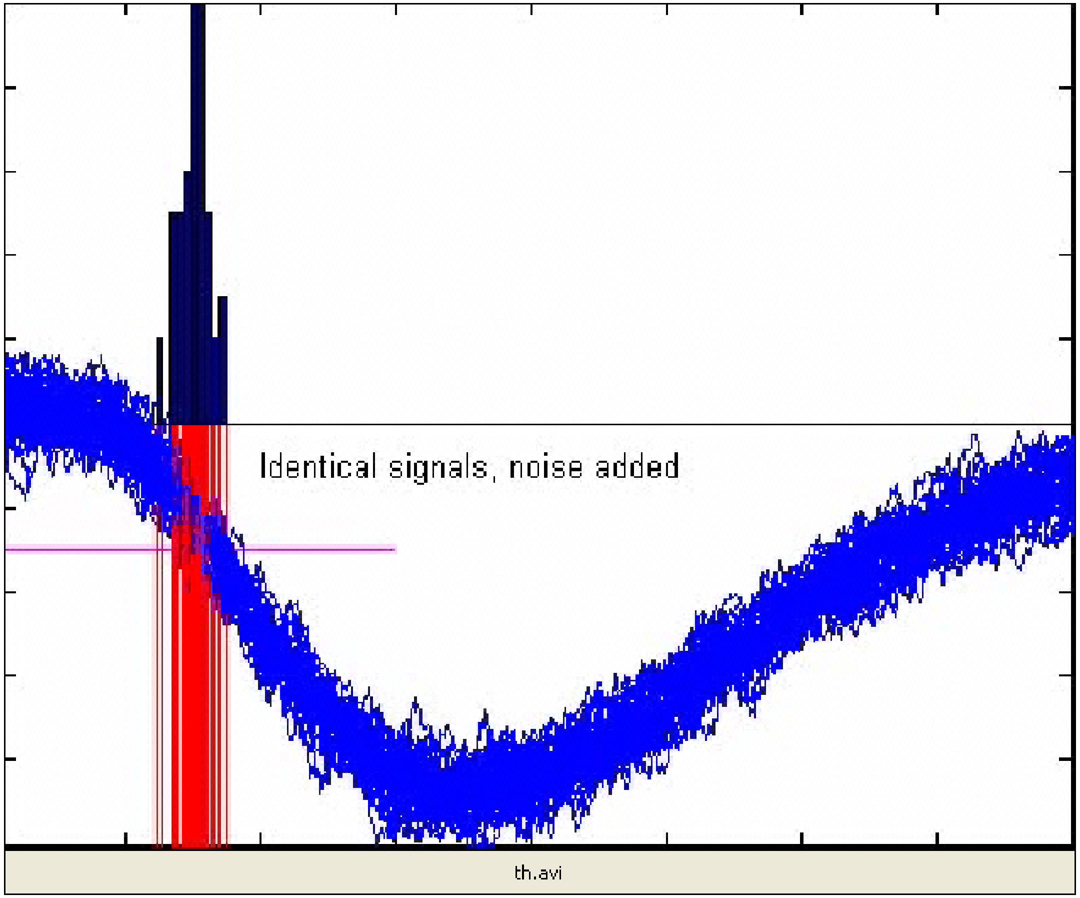
158PEs 1.95ps 97µm

Outline

- Applications of Pico-second Timing
- Micro-Channel Plate devices
- Pico-second electronics and Waveform analysis
- Sampling Electronics
- Pico-second timing SCA in 130nm CMOS technology
- Perspective

Timing resolution [5]

Single Threshold



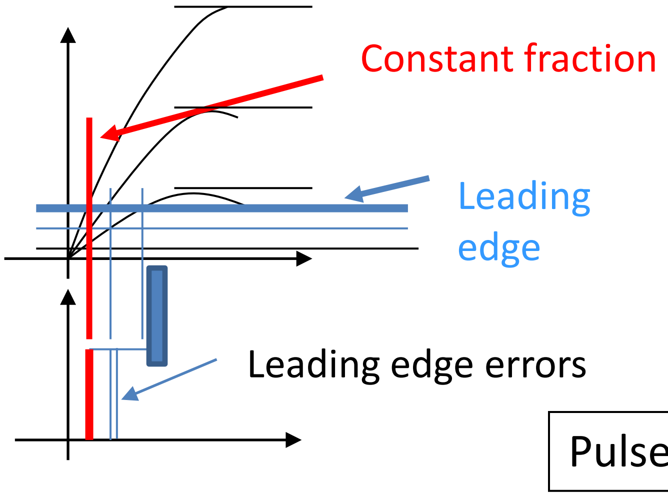
$$\sigma_t = \sigma_x / \frac{dx(t)}{dt}$$

Time spread proportional to 1/rise-time and noise

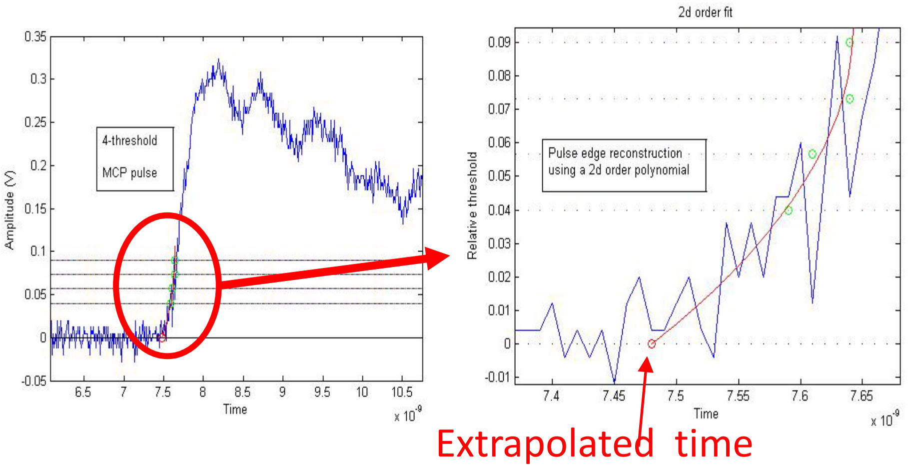
Timing techniques

ANALOG

Constant-fraction

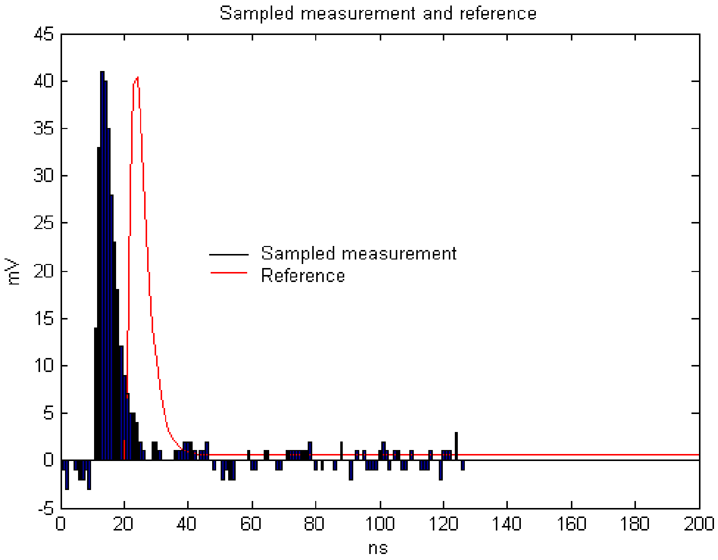


Multi-threshold



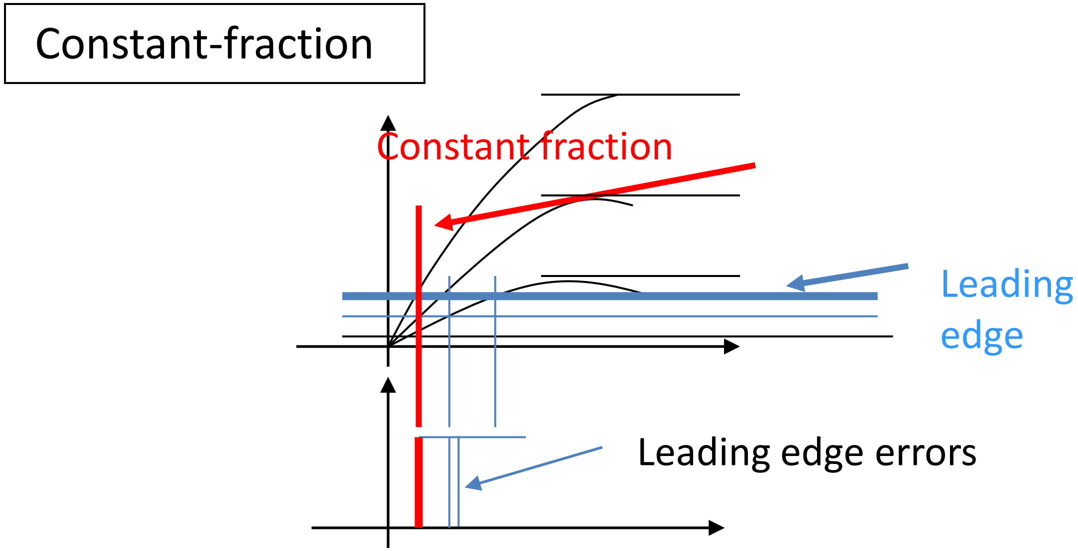
Pulse sampling and Waveform analysis

DIGITAL



Sample, digitize,
Fit to the known waveform

Constant fraction [6]



Measure pulse amplitude: threshold at a given fraction a delayed version of the pulse

3-parameter (at least !) technique

- **Absolute Threshold**
- **Fraction threshold**
- **Delay**

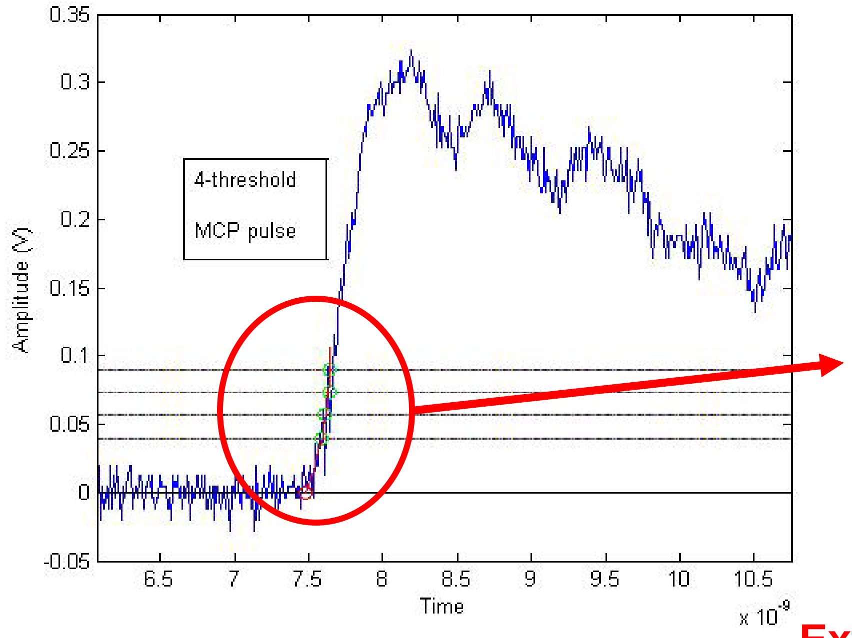
Analog delay difficult to integrate (cable in most implementations)

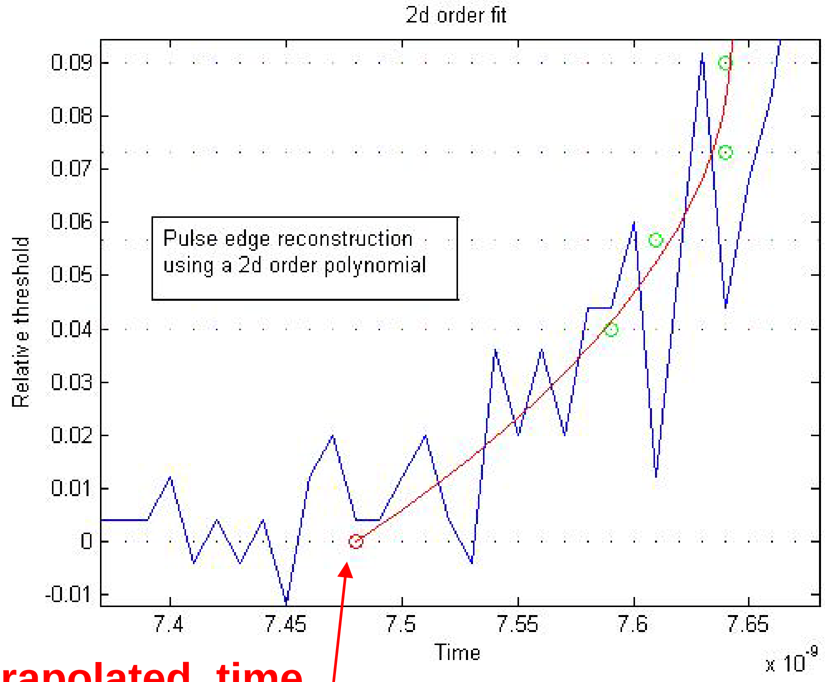
Multi-threshold

Multi-threshold: sample several times over thresholds

Best results:

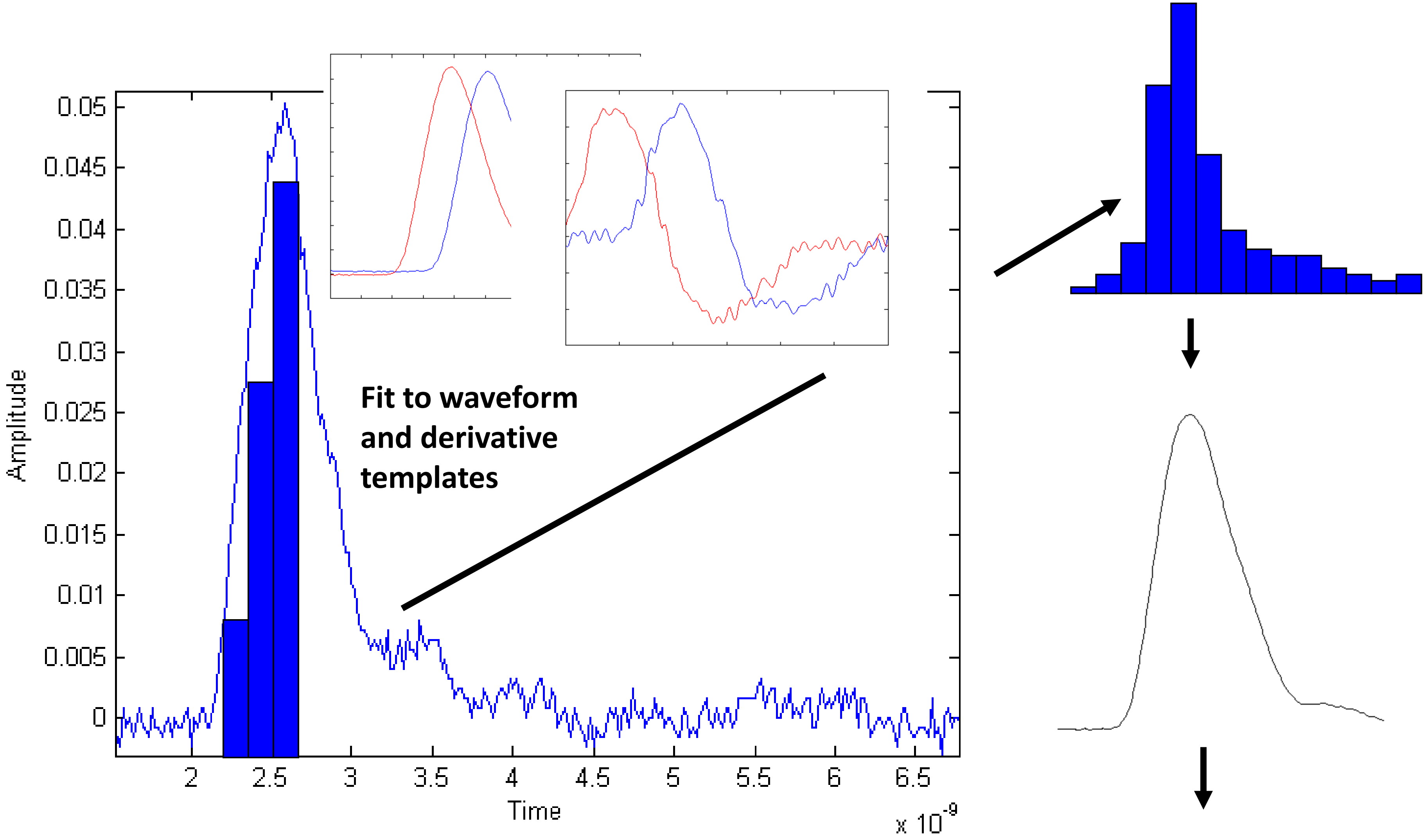
- **Number of thresholds 4-8**
- **Thresholds values equally spaced**
- **Order of the fit: 2d order optimum**





Extrapolated time

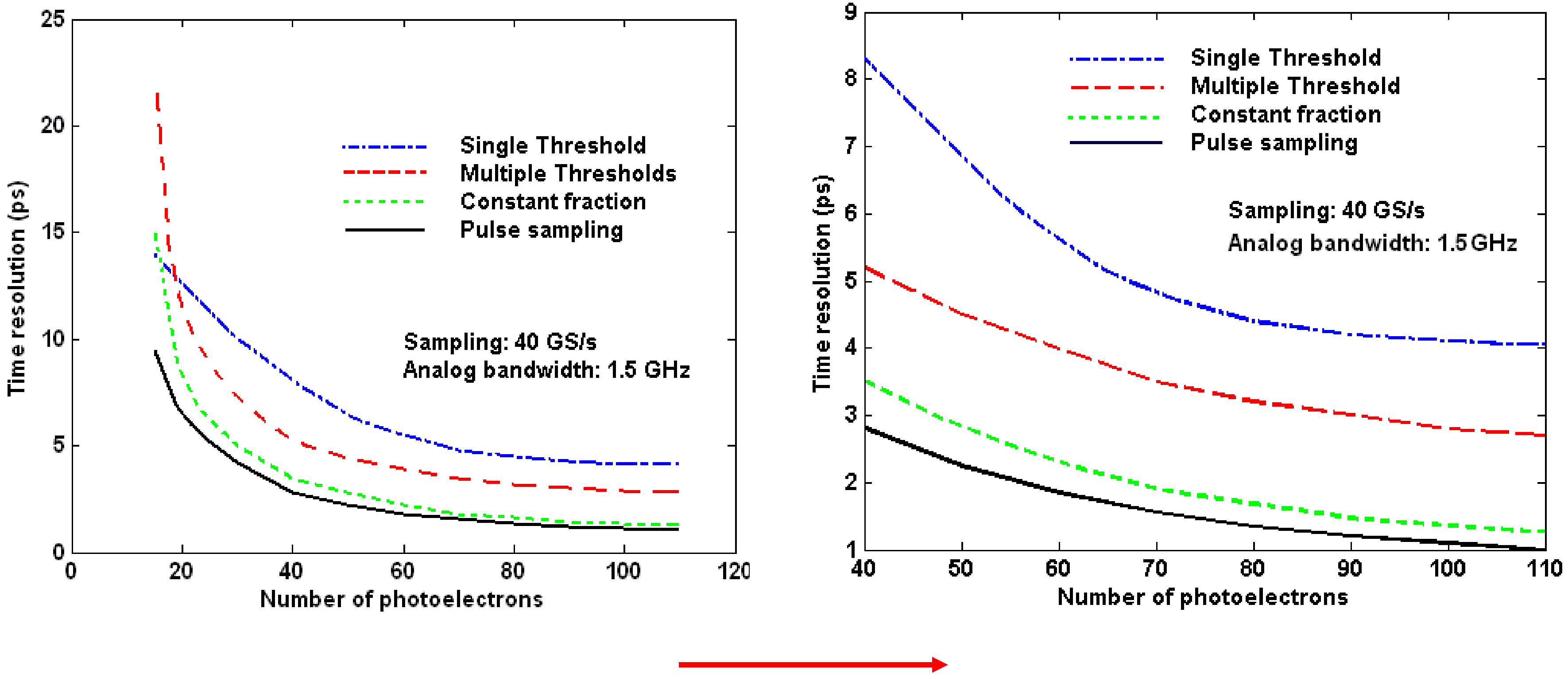
Digital Waveform Analysis



Fit to waveform and derivative templates

Psec Timing and Charge

Methods compared (simulation) [11]



zoom

Time resolution vs Number of photo-electrons

Picosecond Digital Electronics for Micro-Channel Plate Detectors

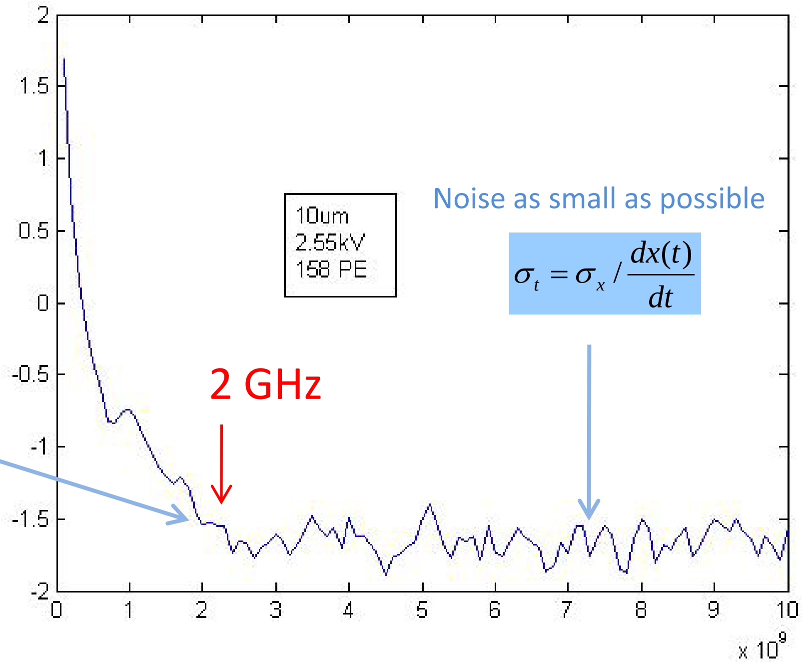
Store the full detector information as with a digital oscilloscope:

- Detector + electronics noise >> quantization noise (LSB/ $\sqrt{12}$)
- Sampling frequency > 2 x full Analog Bandwidth (Shannon-Nyquist)

Fourier spectrum of a 2"x 2" MCP signal

$$\sigma_t = \sigma_x / \frac{dx(t)}{dt}$$

Slope as steep as possible



2 GHz

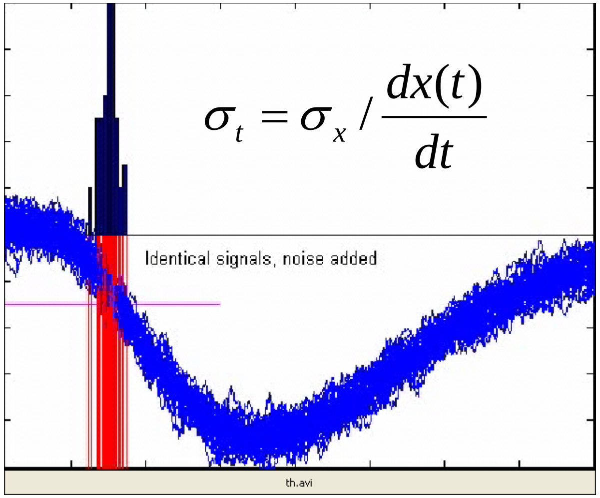
Noise as small as possible

$$\sigma_t = \sigma_x / \frac{dx(t)}{dt}$$

Ideal approach:

Digitize on the fly, if the two above conditions can be fulfilled.
If not, loss of precision due to A/D conversion and/or loss of timing information

Picosecond Digital Electronics for Micro-Channel Plate Detectors



$$\sigma_t = \sigma_x / \frac{dx(t)}{dt}$$

A/D state of the art:

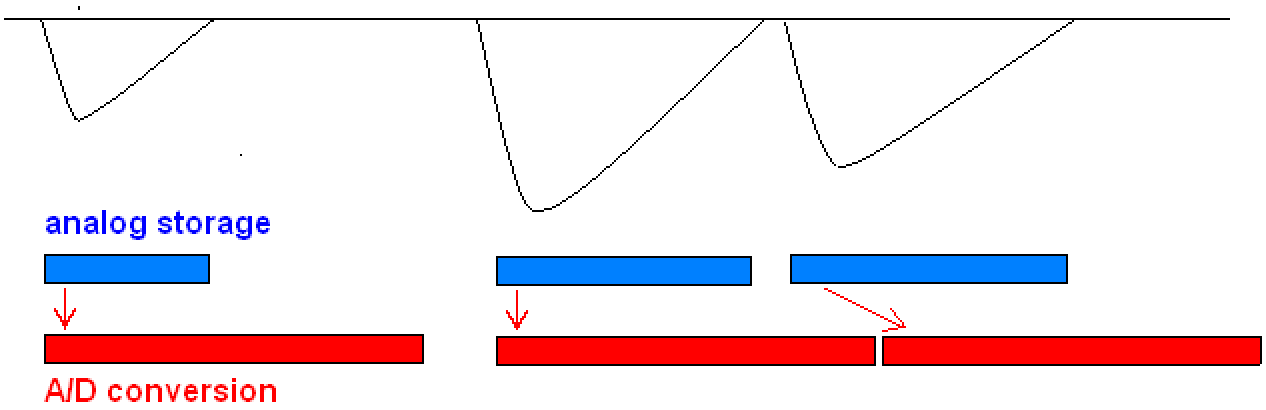
8-bit 1GS/s
10-bit 300 MS/s
16-bit 160 MS/s

Need at least 5 GS/s sampling rate, 10-12bit
There is no !

Fast analog storage
and slower digitization, if rate allows, or dead-time acceptable

Apply the best timing algorithm suited to the detector, get the charge for free … !

Fast analog storage [7-9]



Example:

Analog	ADC
5 GS/s analog storage,	8-ch 12-bit 80 MS/s (AD9222-80)
	Ok up to 2% occupancy

- Internal Analog buffer or
- Use other channels on-chip with a fast input multiplexer

Sampled Micro-Channel Plate signals

Assume: a typical noise at 1mV (detector+system)
LSB set to 1mV for a 1V dynamic range (quantization noise 300μV),
50-200ps rise-time

Fast timing: →

10 bit, 2.5-10 GHz full analog bandwidth > 5-20 GS/s sampling rate

Readout electronics

Deep sub-micron CMOS ASICs:

- ☺ faster: larger analog bandwidth, sampling rate
- ☺ improved radiation hardness
- ☺ cheap, 1-10$/ch
- 🚫 less dynamic range

Outline

- Applications of Pico-second Timing
- Micro-Channel Plate devices
- Pico-second electronics and Waveform analysis
- Sampling Electronics
- Pico-second timing SCA in 130nm CMOS technology
- Perspective

Fast Sampling Electronics

- Integration in custom ASIC for large scale detectors ~ 10^{4-6} channels,
- Self or external trigger,
- Low power,
- Full digital (serial) interface,
- High reliability and availability,
- Low cost.

Sampling Chips

	Sampling GS/s	Bandwidth GHz	Dyn. range bits	Depth	PLL	ADC bits	Trigger	Techno
G. Varner (Hawaii) [9]	6	1.0	10	1024	no	12	experience	.25μm
S. Ritt (PSI) [8]	6	.8	11.5	256	3.9ps	no	no	.25μm
D. Breton/E. Delagnes (Orsay/Saclay) [7]	2.5	.5	13.4	250	20ps	no	no	.35μm

ASIC Deep Sub-Micron (< .13μm) CMOS processes allow today:

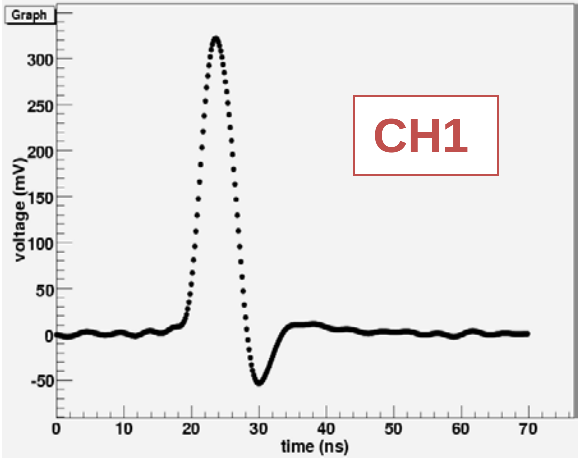
Sampling: 10-20 GHz
Bandwidth: > 1.5 GHz
Dyn. Range: 10bit

Sampling Chips Survey

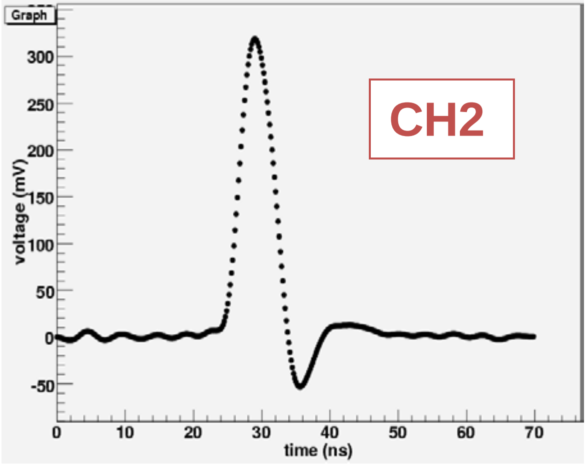
	Hawaii	Varner		Saclay/Orsay	Delagnes/	Breton		PSI	S.Ritt	This proposal
	Blab1	Lab1-2	Lab 3	Hamac	Matacq	Sam	Planned	DRS3	DRS4	
Sampling	100 MHz-6 GHz		20 MHz-3.7GHz	40 MHz	0.7-2.5 GHz	0.7-2.5 GHz	10 GHz	10 MHz-5 GHz	5 GHz	10-20 GHz
Bandwidth (3db)	300 MHz		900 MHz	50 MHz	200-300 MHz	300 MHz	650 MHz	450 MHz	950MHz	> 1.5 GHz
Channels	1	8	9	8	1	2		12 6 2 1	8 4 2 1	4 16
Triggered mode	Yes		Common stop		Yes			Common stop	Common stop	Channel trigger
Resolution	10 bit			13.3 bit	13.4 bit	11.6 bit		11.6 bit	11.5 bit	8-10-bit
Samples	128 rows of 512	256	256	144	2520	256	2048	1024-12288	1024-8192	256
Clock			33 MHz	40 MHz	100 MHz				fsamp/2048	20-40 MHz
Max latency	560 us	2.2ms	50us							
Input Buffers	Yes			Yes	Yes	Yes	No	No	No	No
Differential inputs	No	No	No	Yes	Yes	Yes		Yes	Yes	Yes
Input impedance	50 Ohms	50 Ohms	50 Ohms Ext	10 MOhm/3pF	50 Ohms				11pF	50 Ohms
Readout clock	500 MHz			5 MHz	5 MHz	16 MHz		33 MHz	33MHz	500 MHz
Locked delays	Ext DAC	Ext DAC	Ext DAC			Yes		Ext PLL	Int PLL	Int PLL
On-chip ADC	12-b +500MHz TDC			No		No		No	No	Yes
R/W simultaneous	Yes			Yes		No		No	Yes	No
Power/ch	15mW/1.6W			36 mW	250-500 mW	150 mW		2-8mW	7.2mW at 2GS/s	
Dynamic range	1mV/1V			0.26mV/2.75V	175 uV-2V	0.65mV-2 V		0.35mV/1.1V	.35mV/1V	1V
Xtalk	Inter-rows 0.1%		10%			0.30%		< 0.5%		
Sampling jitter			4.5ps			25ps			6ps	?
Power supplies	-tbd/+2.5	-tbd/2.5V	-tbd/2.5V	-1.7/3.3V				2.5V	2.5V	1.2V
Process	TSMC .25	TSMC .25	TSMC .25	HP/DMILL .8	AMS .8	AMS .35	AMS .18	UMC .25	UMC .25	IBM .13
Chip area	5.25 mm2	10 mm2	2.5mm2	19.8mm2	30mm2			25mm2		1mm2/ch
Temp coeff	0.2%/°C		0.2%/°C					5e-5/°C	25ppm/°C	
Cost/channel	500$/40 10$/2k								10-15$	

Existing ASICs: Labrador 3 [9]

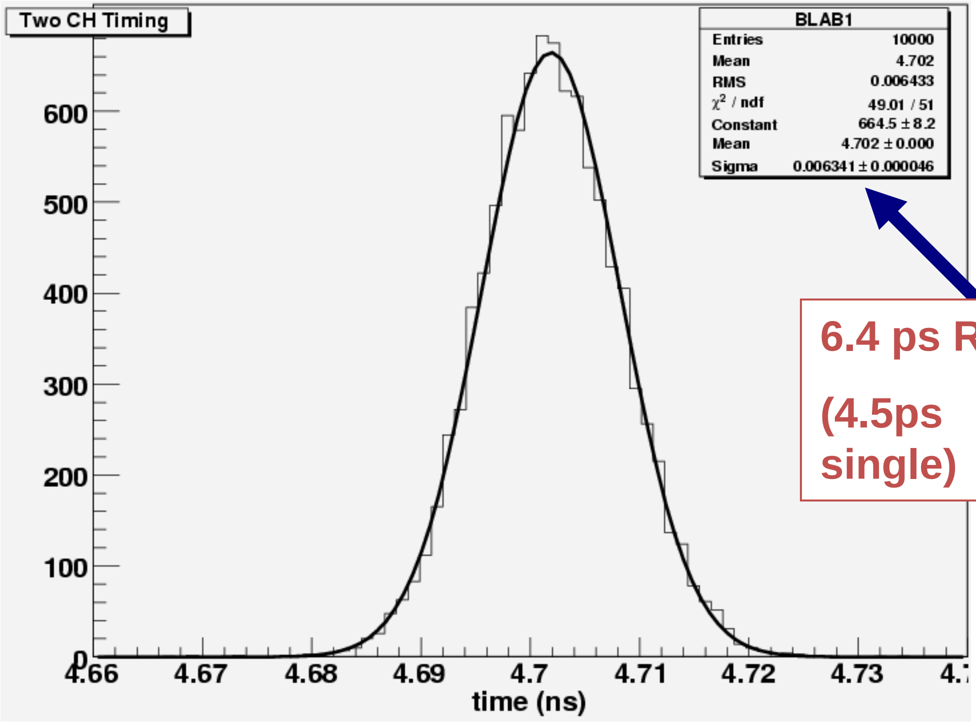
Gary Varner
U-Hawaii



CH1



CH2



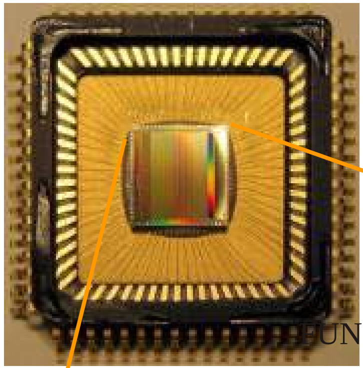
6.4 ps RMS

(4.5ps single)

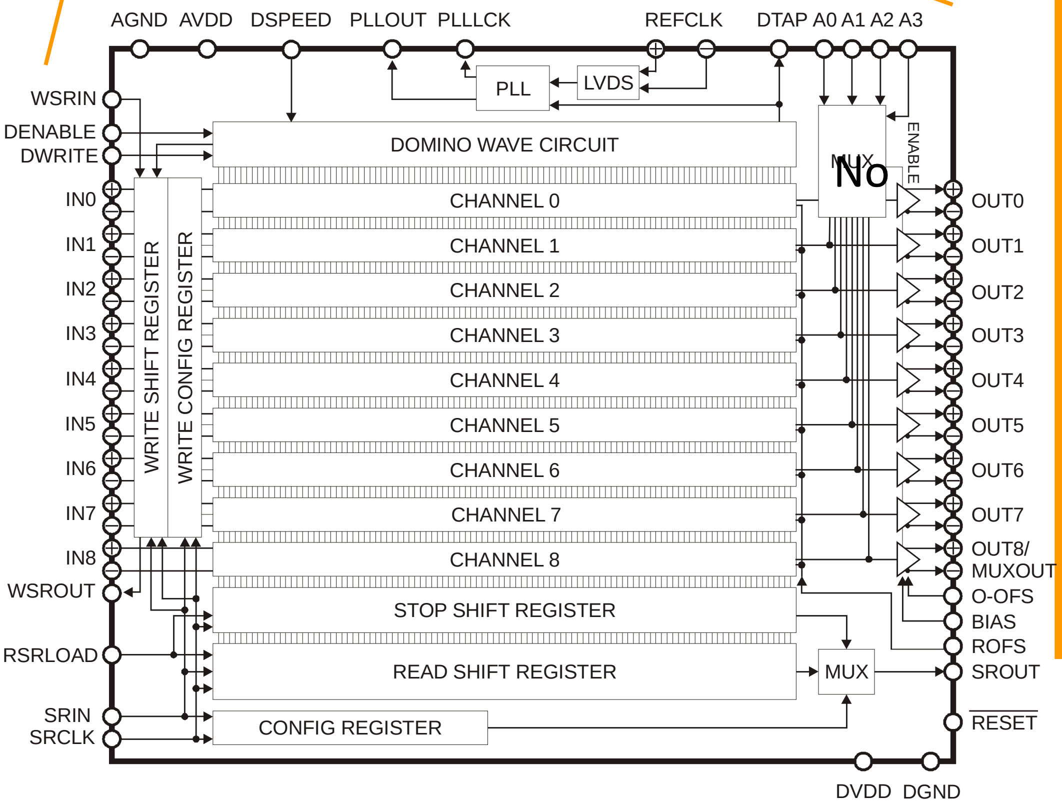
250nm CMOS

Waveform Digitizing Chip DRS4 [8]

Stefan Ritt
Paul Scherrer Institute
Switzerland



FUNCTIONAL BLOCK DIAGRAM

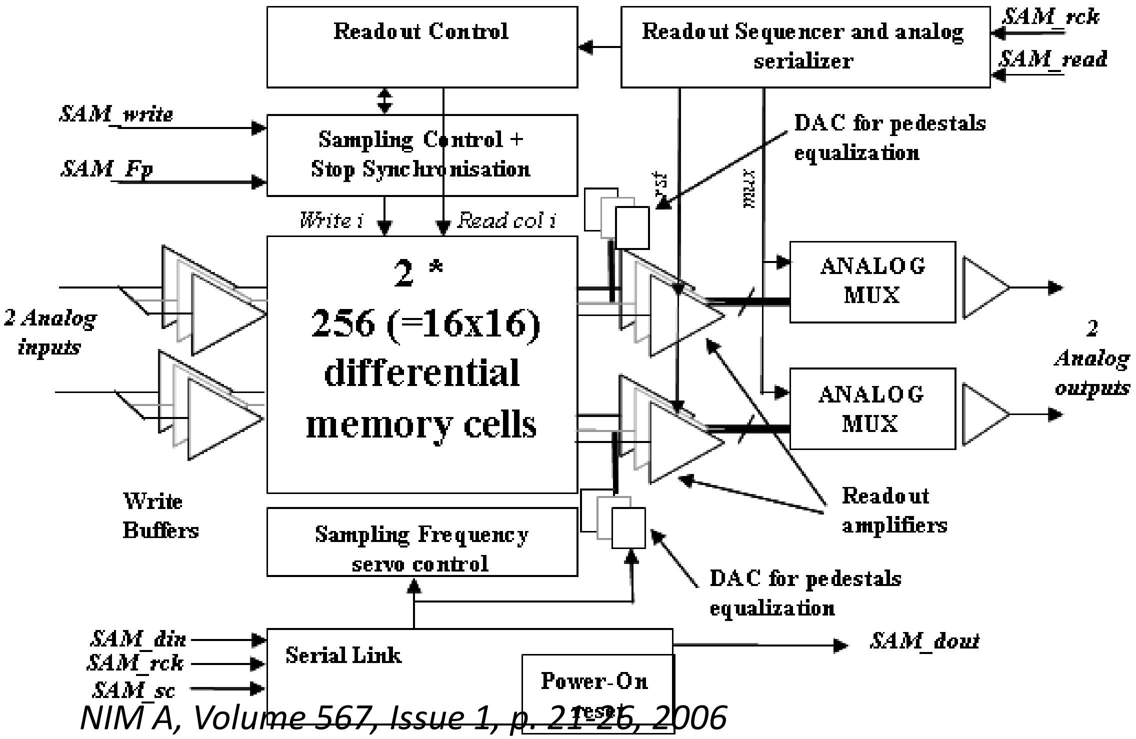


- UMC 0.25 µm rad. hard
- 9 chn. each 1024 bins, cascadable up to 8192
- Sampling speed 0.2 … 5 GS/s
- Bandwidth 950 MHz
- 17.5 mW/chn @ 2.5V
- On-chip PLL stabilization
- Readout speed using ext. ADC: 30 ns * $n_{samples}$
- SNR: 69 dB calibrated
- Aperture jitter: 4 ps at 5 GS/s calibrated

250nm CMOS

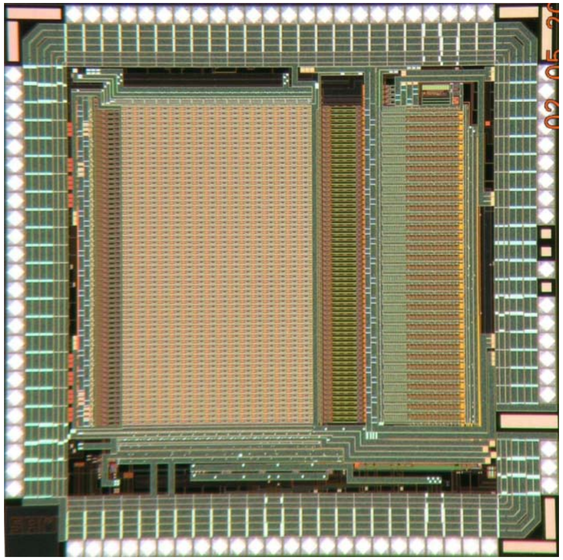
The SAM (Swift Analog Memory) ASIC [7]

D. Breton/E. Delagnes
Orsay/Saclay



NIM A, Volume 567, Issue 1, p. 21-26, 2006

- **2 differential channels**
- **256 cells/channel**
- **BW > 450 MHz**
- **Sampling Freq 400MHz->3.2GHz**
- **High Readout Speed > 16 MHz**
- **Smart Read pointer**
- **Few external signals**
- **Many modes configurable by a serial link.**
- **Auto-configuration @ power on**
- **AMS 0.35 µm => low cost for medium size prod**



6000 ASICs manufactured, tested and delivered in Q2 2007

Outline

- Applications of Pico-second Timing
- Micro-Channel Plate devices
- Pico-second electronics and Waveform analysis
- Sampling Electronics
- Pico-second timing SCA in 130nm CMOS technology
- Perspective

130nm CMOS Sampling ASIC

This chip is developed by U-Chicago and U-Hawaii

It includes

- 4 channels of full sampling (256 cells)
- 1 channel of sampling cell to observe the sampling window

Test structures:

- Sampling cell,
- ADC Comparator,
- Ring Oscillator

Sampling ASIC

- Prototype chip in 130nm CMOS technology (IBM 8RF-DM)

- **4-channel sampling, >10-15GSa/s**
- **1-2 GHz analog bandwidth, 50 Ohms**
- **40-80 MHz clock**
- **256 cells (<100ps/cell, 12.5-25ns range)**
- **Free running delays (no PLL)**
- **Sampling window 500ps-2ns**
- **Dynamic range .7V**
- **Crosstalk <1%**
- **On-chip parallel 12-bit ADC (2 μs min conversion time)**
- **Free running delays (No PLL)**
- **Linearity < 1% on the full dynamic range**
- **Read clock up to 50 MHz (one cell/period, 22 μs total readout time)**
- **One reference channel (sampling window)**
- **1.2V power supply**
- **Power < 40 mW/channel**
- **Process IBM 8RF-DM (130nm CMOS)**

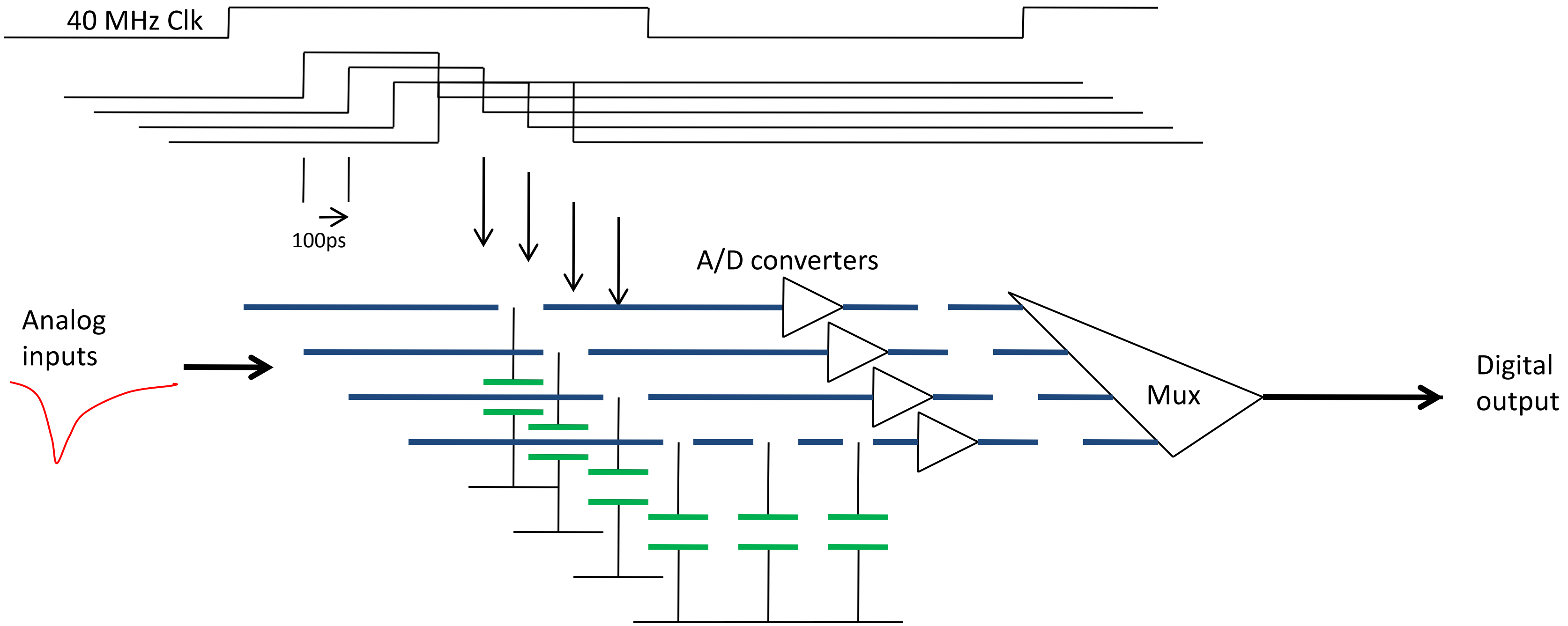
- **4 x 4 mm^2**

Chicago-Hawai'i

Sent July 2009, received Oct 21st

Sequence of operations

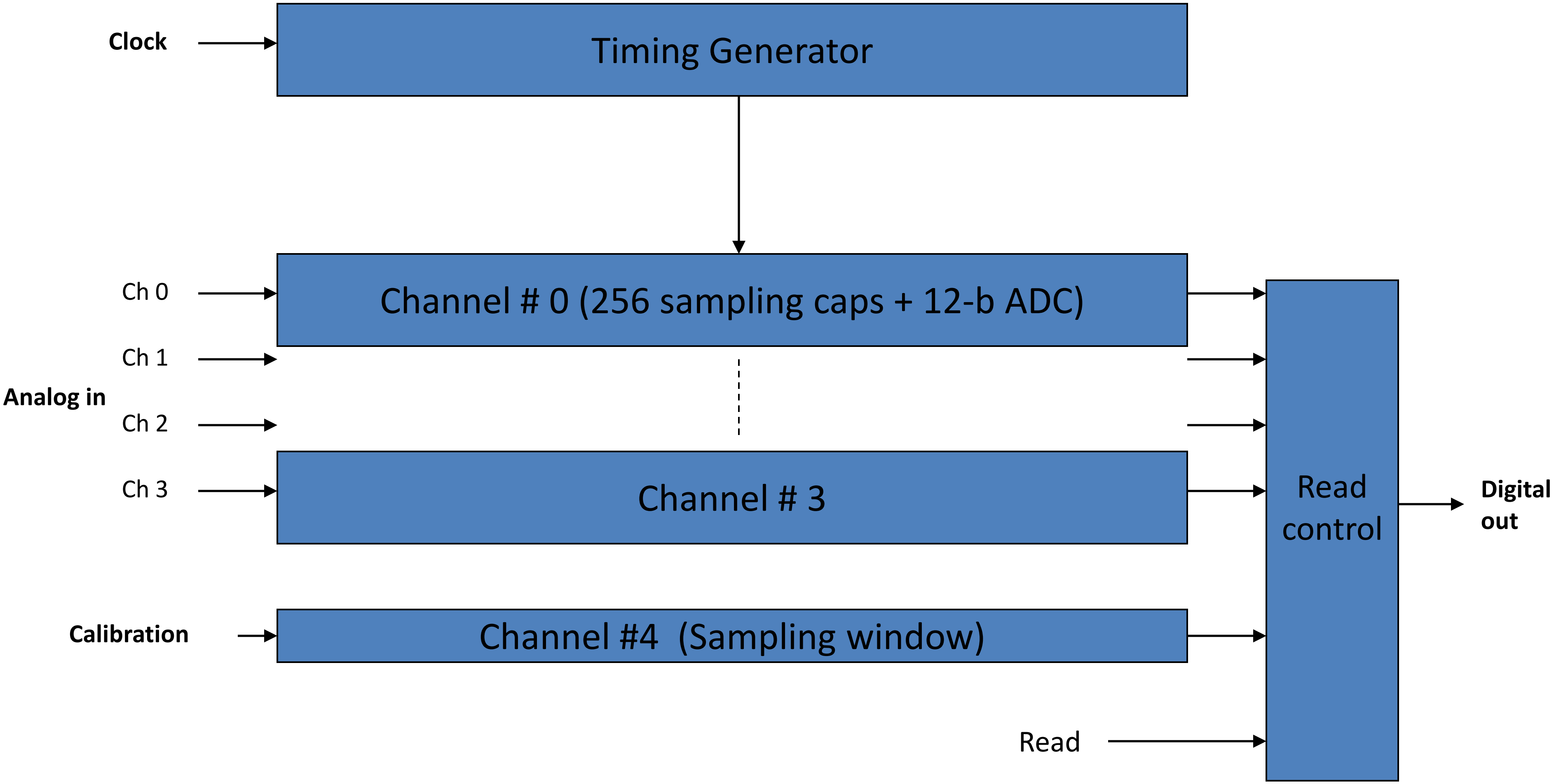
-1 Write: The timing generator runs continuously, outputs clock phases 100ps spaced. Each phase closes a write switch during one sampling window.



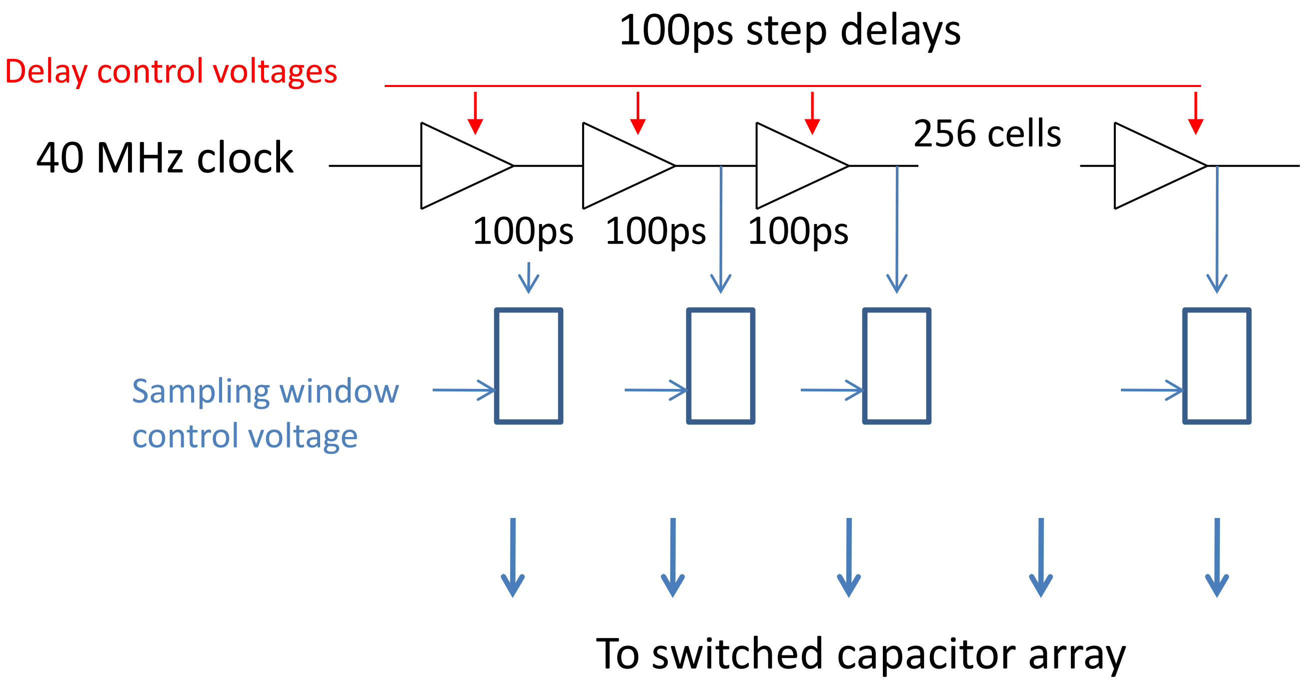
-2 A/D conversion after a trigger that opens all the write switches
and starts all A/D conversions in parallel
Data available after 2 μs (2GHz counters)

-3 Read occurs after conversion (data can still be taken as in Phase 1)

Block diagram



10 GS/s Timing Generator



100ps step delays

Delay control voltages

40 MHz clock

256 cells

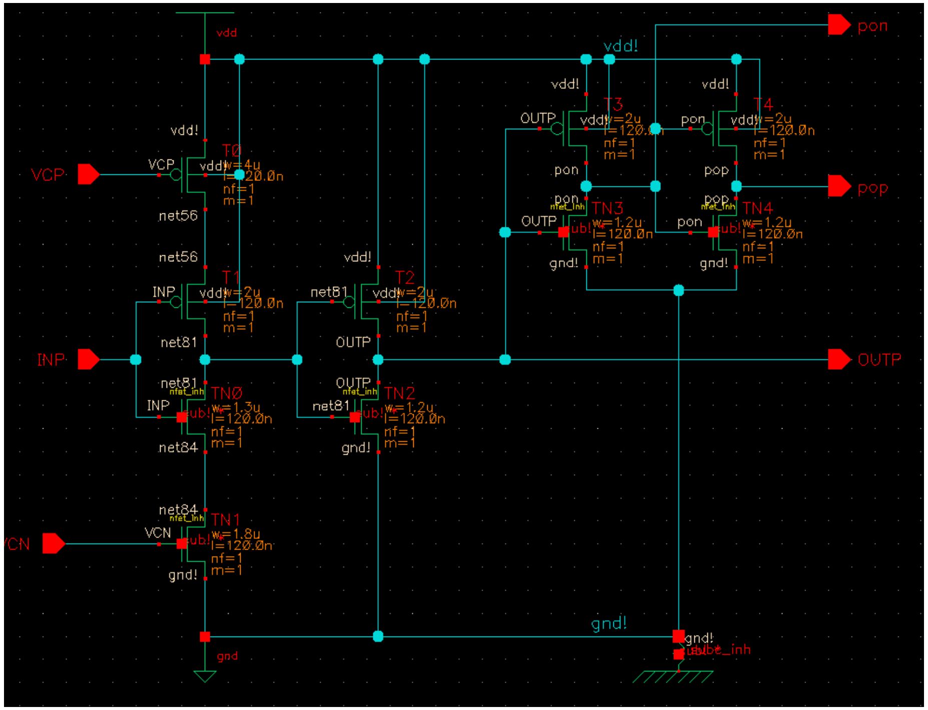
100ps 100ps 100ps

Sampling window control voltage

To switched capacitor array

Timing Generator
Voltage Controlled Delay Cell

- 256 voltage controlled delay cells of 100-200ps
- 20-40 MHz clock propagated

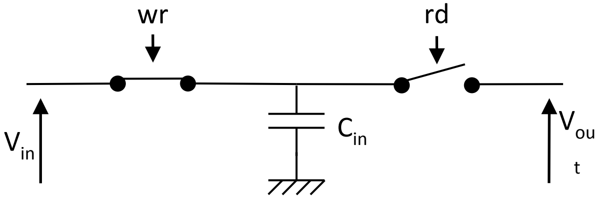


Voltage Controlled Delay Cell

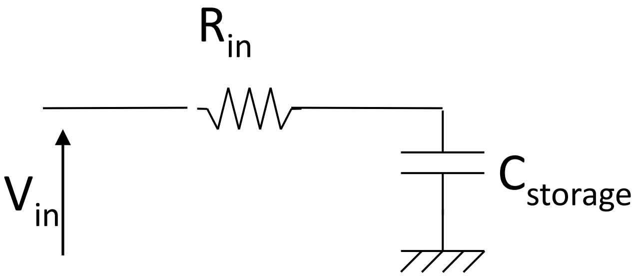
Test structure:

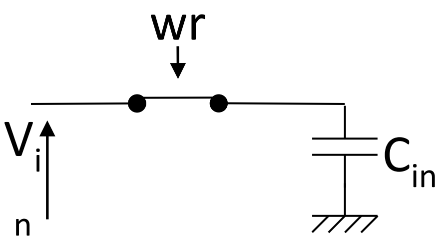
Ring Oscillator: Two delay cells + inverter

Sampling Cell



Principle





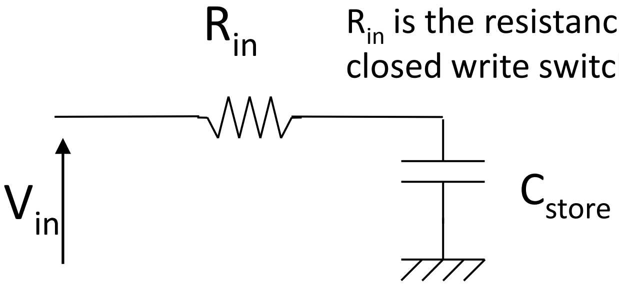
“Write” state 3 dB analog bandwidth is $1/(2\pi R_{in} C_{storage})$

“Sampling window” Number of switches closed x sampling period

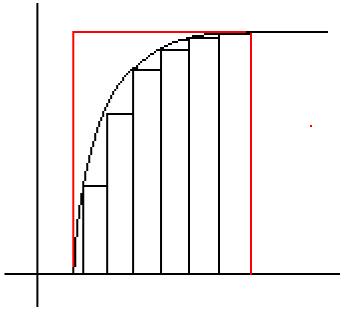
Thermal kT/C switching noise = 250µV = one 12-bit ADC count

Analog bandwidth and Sampling window

On chip:



R_{in} is the resistance of the closed write switch



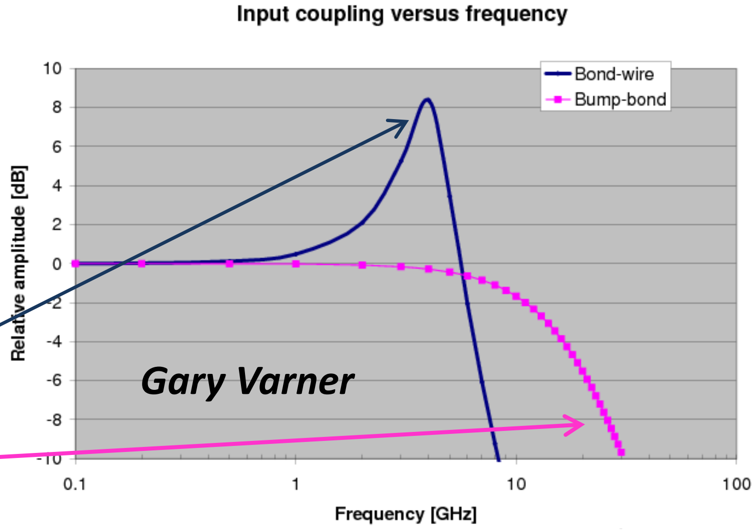
Sampling window

Sampling window = Number of switches closed at a time x sampling period

Sampling Window$_{10\text{-}3}$ = -log(10^{-3}) x rise-time / 2.2= 1/ 3 dB Analog Bandwidth

In practice, R_{in} and C_{store} are minimum, but limited by the stray capacitor of the switch, and the leakage current of the switch in the open state.

R_{in} =1.5kΩ, C_{store}= 70 fF
3dB Analog Bandwidth = 2 π $R_{in}C_{store}$= 1.5 GHz
Sampling window $_{10\text{-}3}$ > 625ps = 7 samples at 10 GS/s

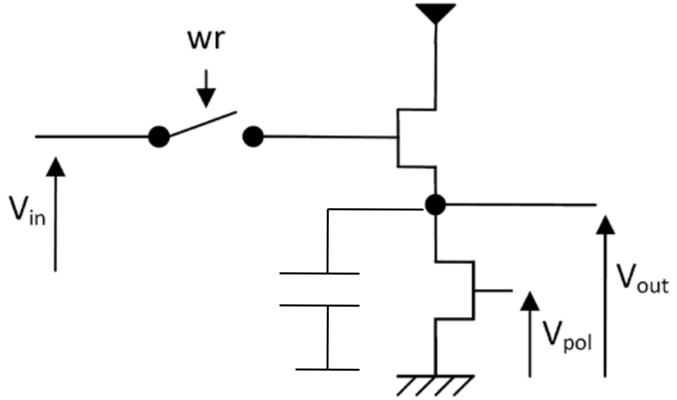


Off chip: Inductance of the wire bonds and pad capacitance: **Bump-bonding**

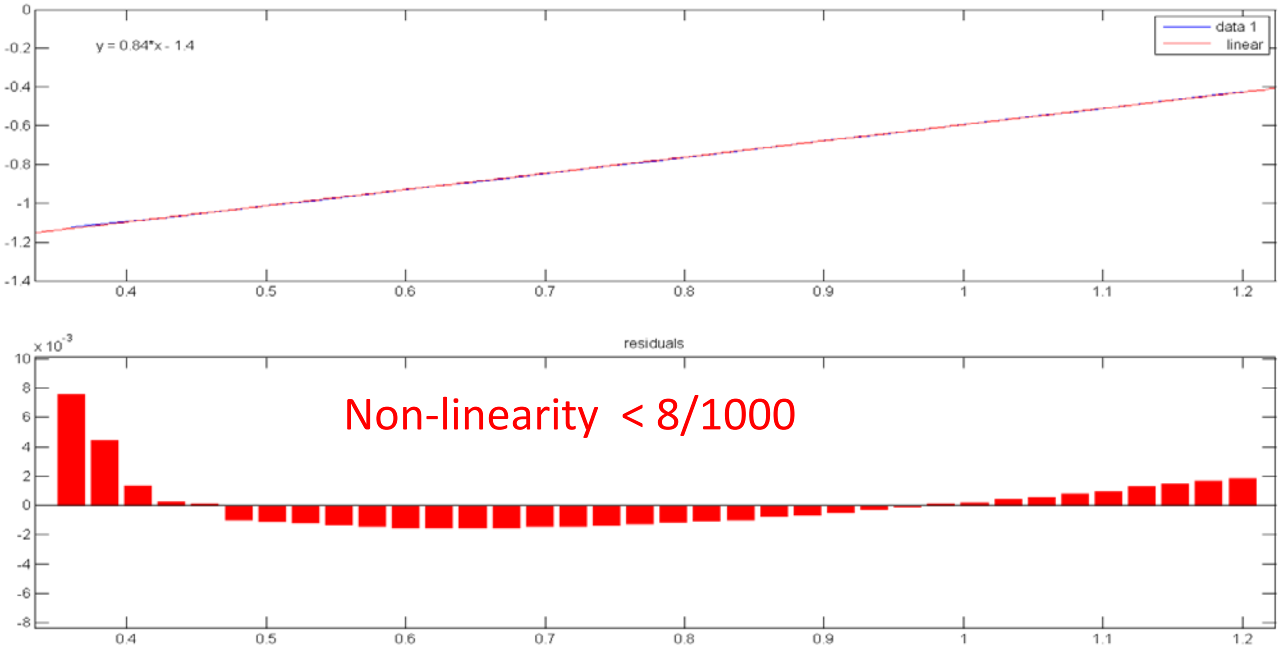
Sampling cell design

Need a voltage buffer to read the small storage capacitor (70fF)

The gate of the source follower transistor is part of the storage capacitor (40+30fF)

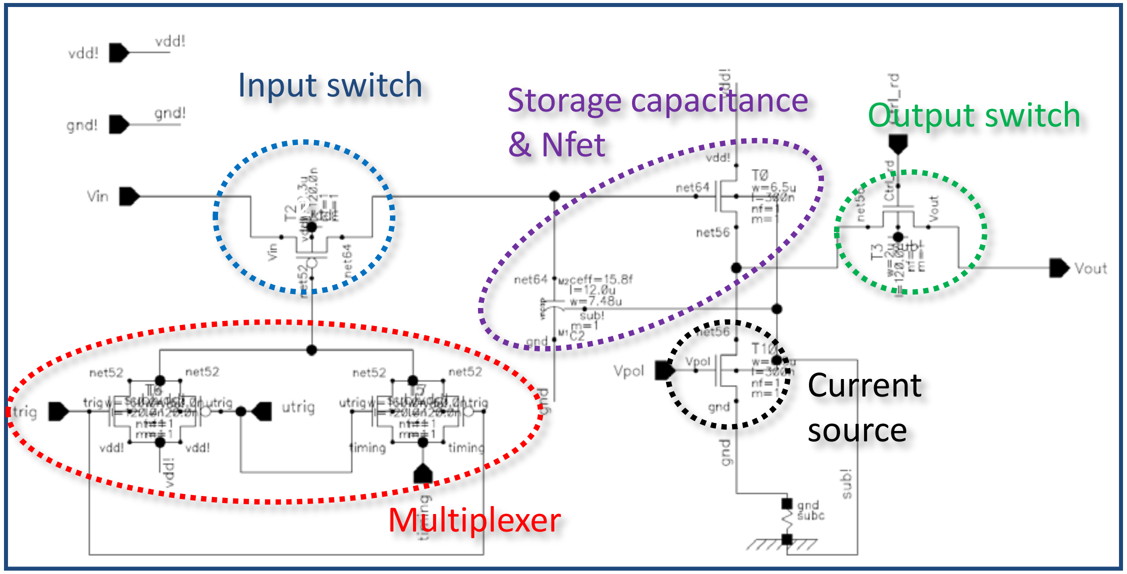


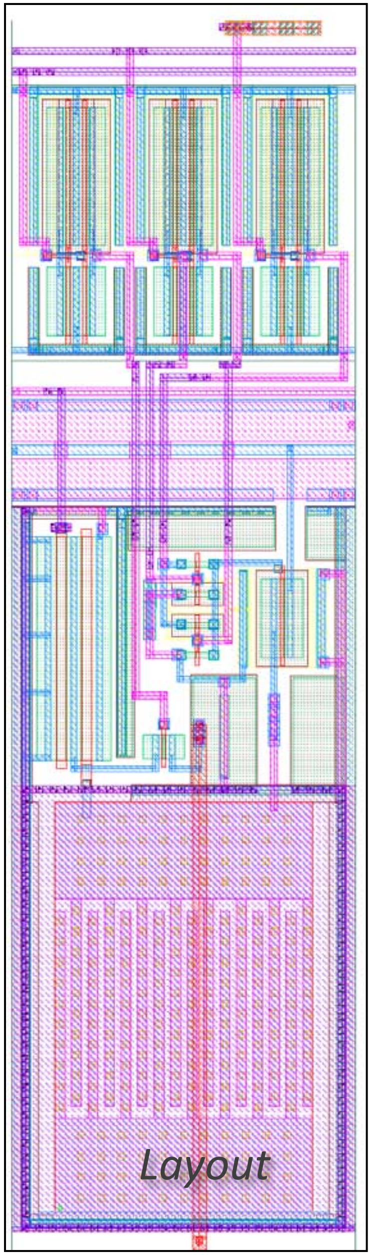
$$V_{out} = Vin - V_T - (V_{pol} - V_T)\sqrt{\frac{W}{L}\frac{L_{pol}}{W_{pol}}}$$



Non-linearity < 8/1000

Sampling Cell





Sampling Capacitance 70fF
Switch resistance: 1.5kΩ
Analog bandwidth 1.5GHz

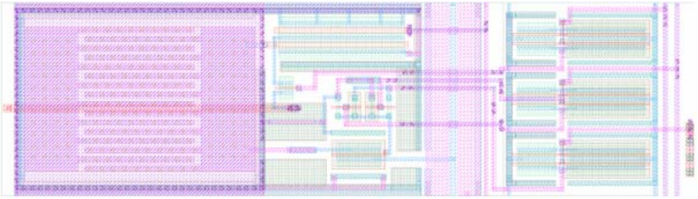
ADC

Wilkinson:

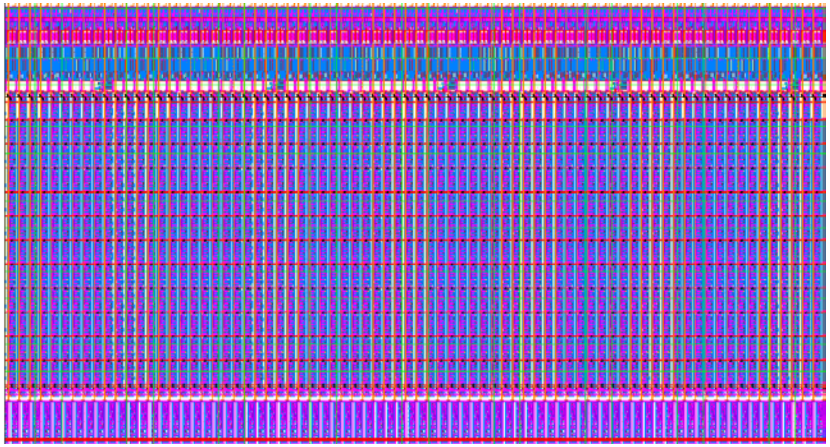
All cells digitized in one conversion cycle

- Ramp generator
- Comparators
- Counter
- Clocked by the ring oscillator at 1-2 GHz

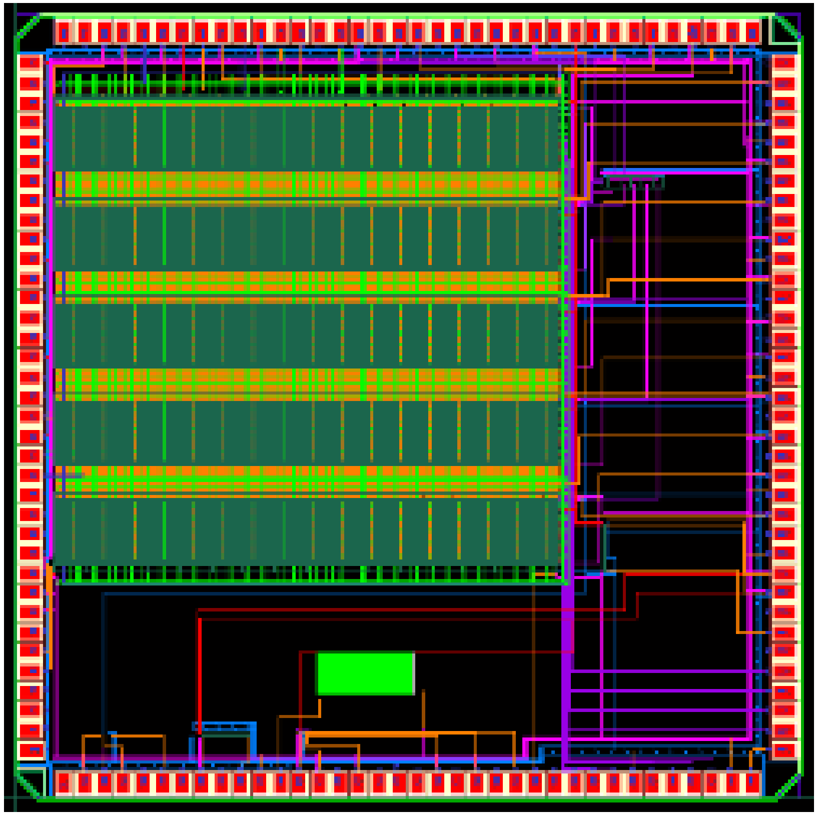
Layout



One sampling cell

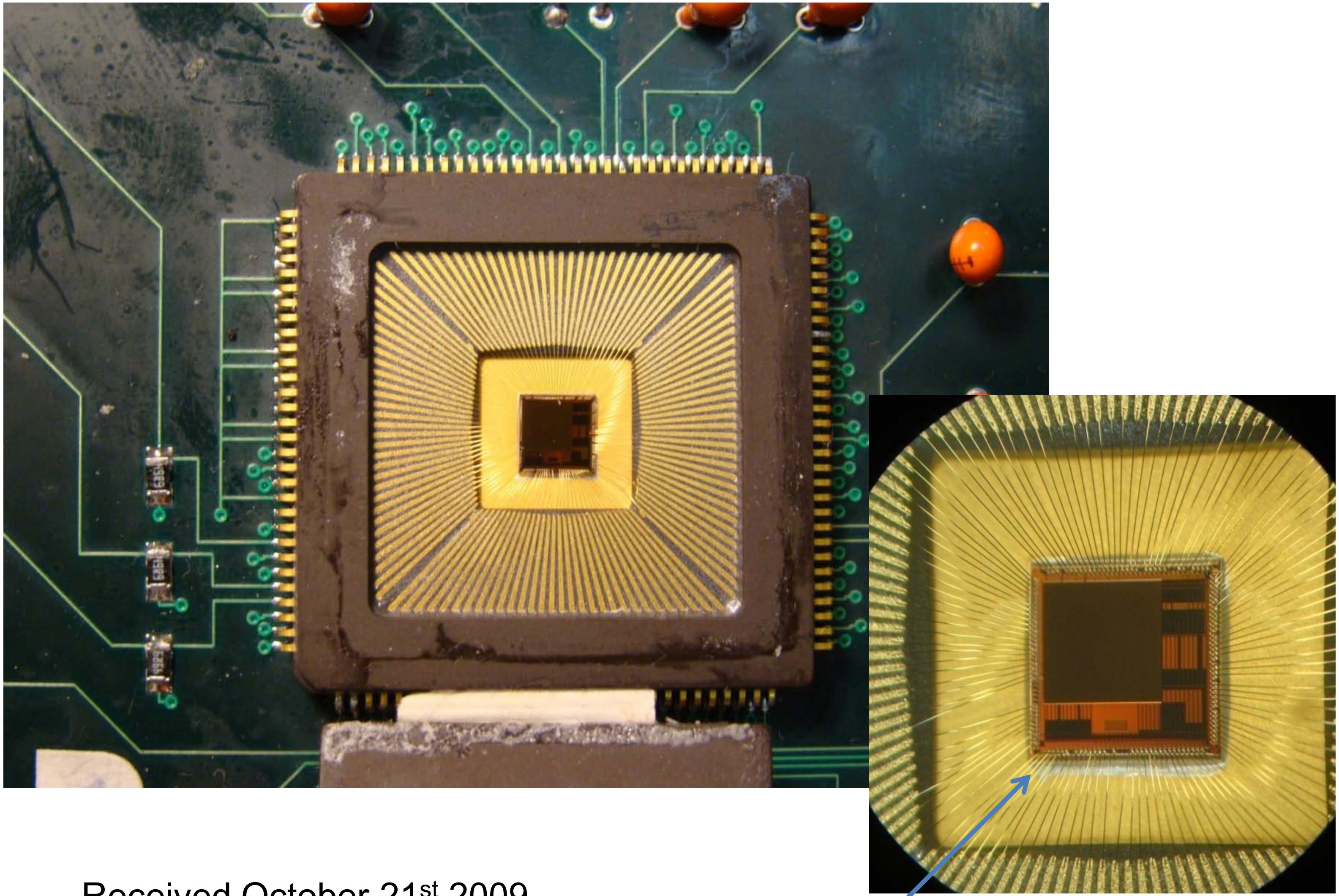


One channel



CMOS 130nm IBM 4 x 4 mm^2

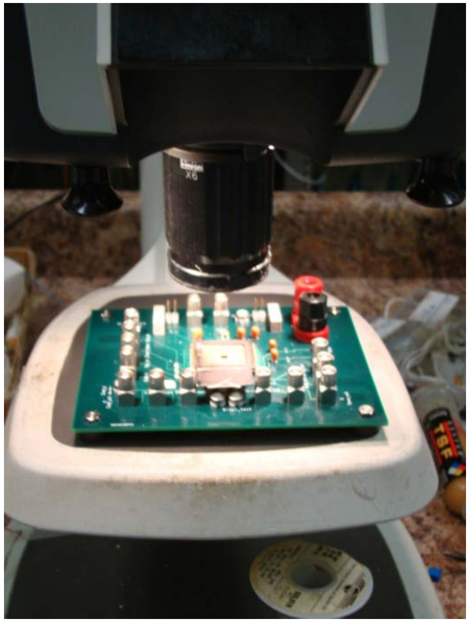
Pictures



Received October 21st 2009

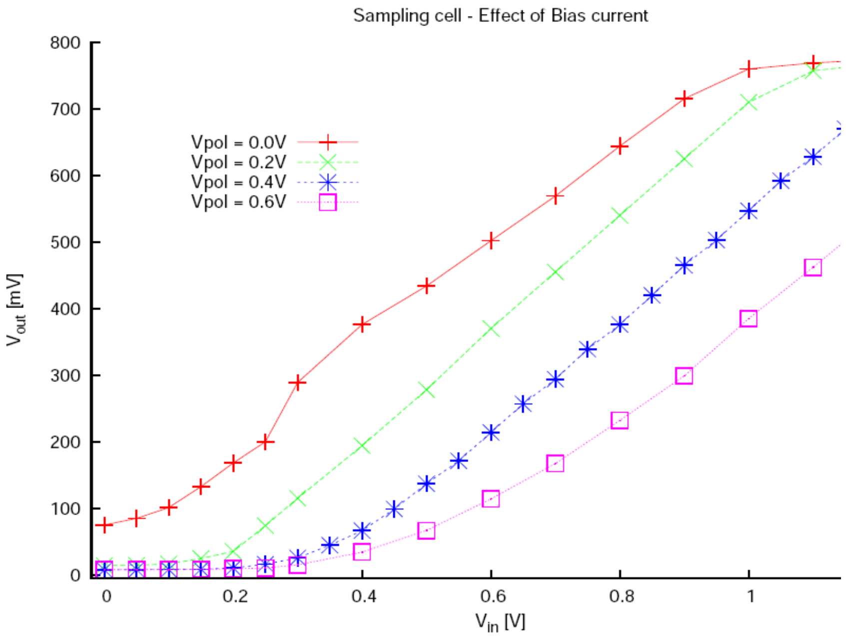
Die to be bump-bonded on PCB

Tests

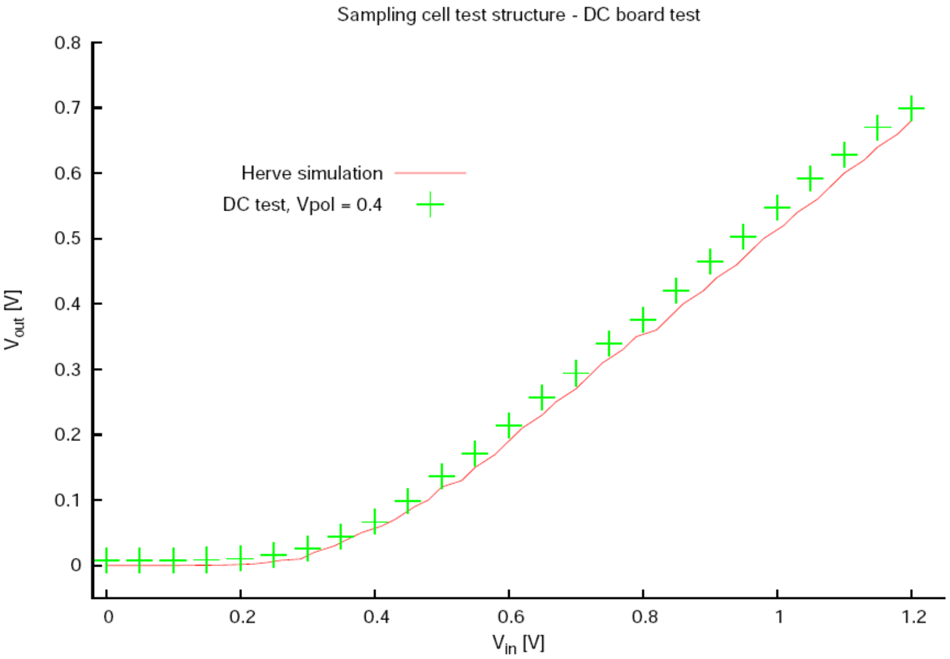


- First tests of packaged chips (presented here)
  - DC power vs biases,
  - Sampling cell response vs input
  - ADC's comparator
  - Leakages (voltage droop)
  - Digital Readout
- Fine tests to come… (chip is just being bump-bonded to PCB)
  - Analog bandwidth
  - Resolution, signal-to-noise
  - Sampling cell response vs sampling window
  - Crosstalkk
  - Max sampling rate
  - Full ADC
  - Linearities, dynamic range, readout speed

Tests: Sampling cell



Measurements



Simulation/Measurements

Ok, except a saturation for voltage inputs > 750 mV

Very close to simulation

Tests: Sampling cell Leakages

1 - input LOW, write switch CLOSED

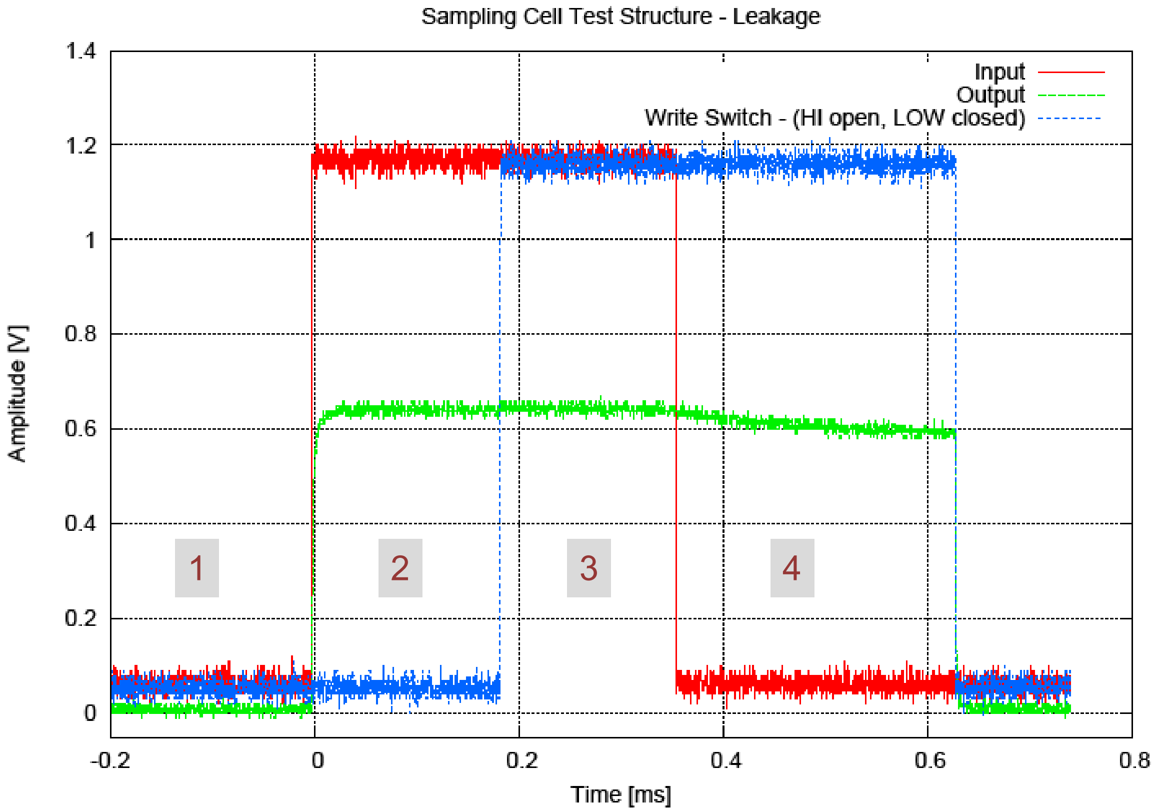
2 - input HI, switch CLOSED

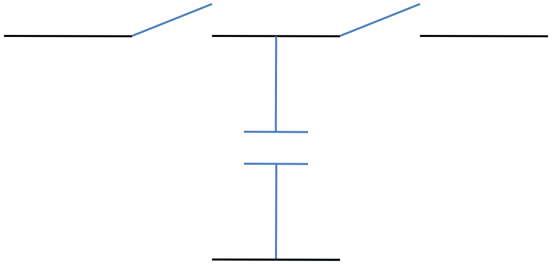
3 - input HI, switch OPEN

4 - input LOW, switch OPEN

Leakage current is 7 pA

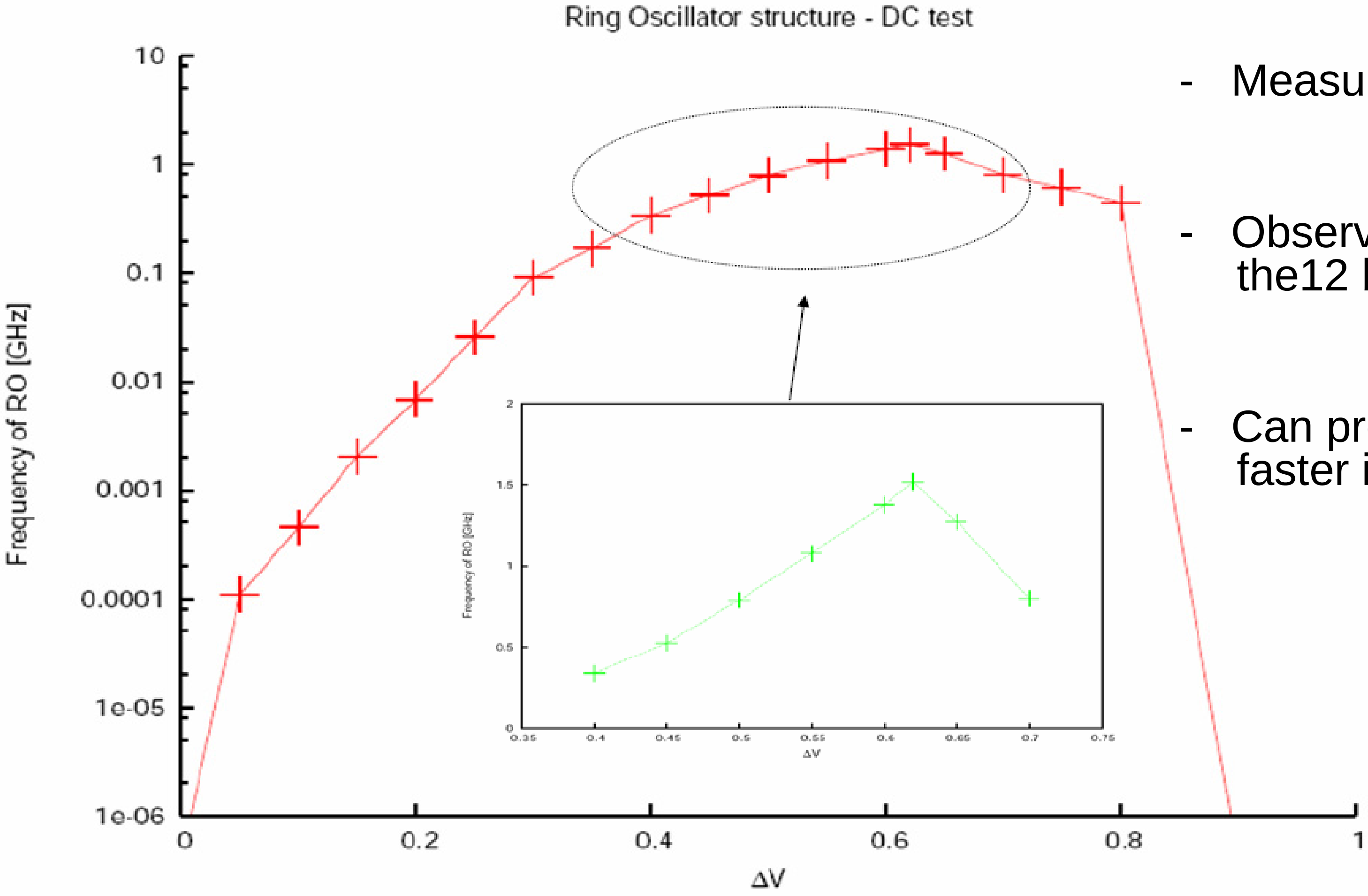
Much smaller than in simulation





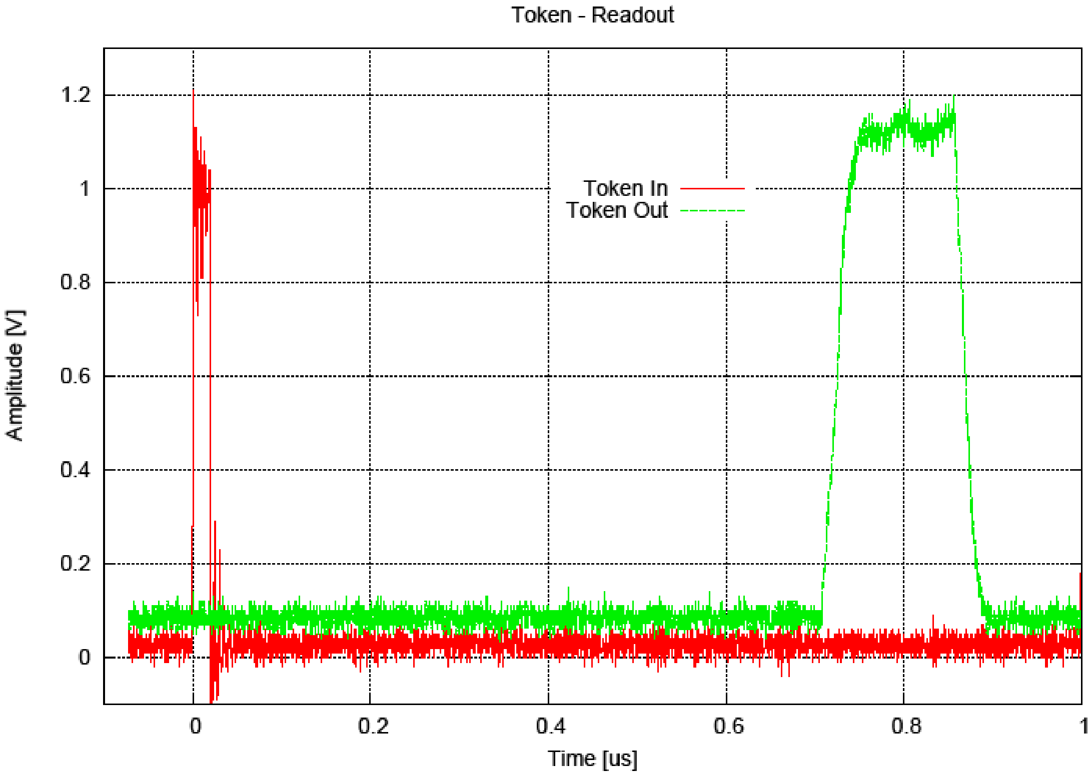
Write switch   Read switch

Tests: Ring Oscillator



- Measured up to 1.5 GHz
- Observation limited by the12 bit down-counter
- Can presumably run faster internally

Tests: Digital readout



Token passing readout to multiplex the 1024 data words onto the output bus

.

Tests Summary

Test structures measured as expected from simulations in terms of:

- Dynamic range:

  Sampling cell runs ok within 0-700mV as simulated
- Speed:

  Ring Oscillator up to 1.5 GHz
- Readout logic ok

One problem with I/O pads:

DC path to ground through protection diodes, but I/O's can be easily overdriven.

Full sampling channels have still to be measured

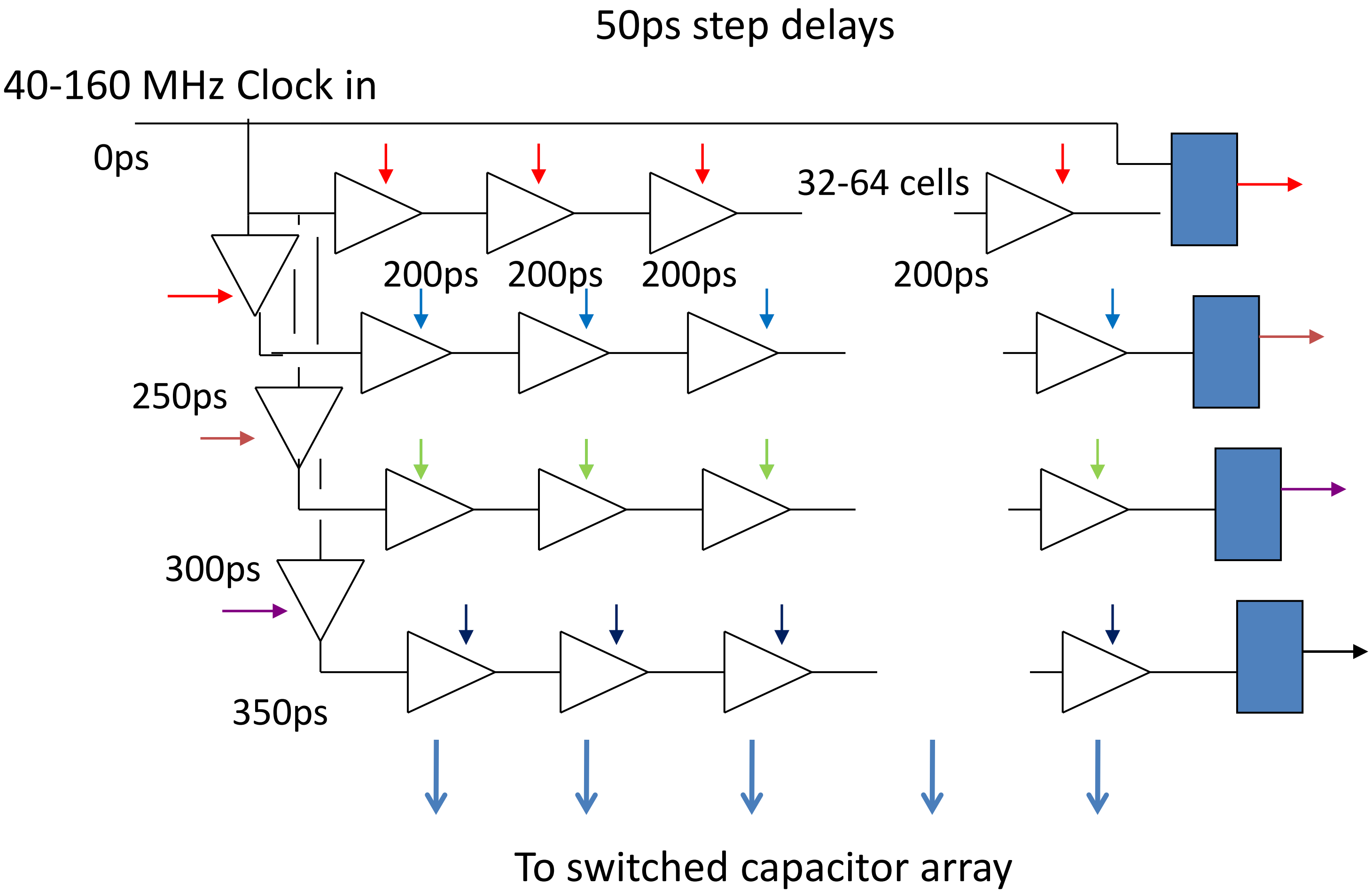
Next Design

- Measure and fully understand the first version
- Test with actual MCP signals for pico-second timing

- Include:
  - Input trigger discriminator
  - Phase lock (Temperature, voltage supply, process)
  - Increase the dynamic range to 1V
  - Improve the analog bandwidth to 2GHz
  - Increase the sampling rate up to 20 GS/s
  - Improve the readout frequency to 8 x 40 = 320 MHz

- 130nm CMOS runs at MOSIS: Feb 1st, May 10th

20 GHz Timing generator [12]



Outline

- Applications of Pico-second Timing
- Micro-Channel Plate devices
- Pico-second electronics and Waveform analysis
- Sampling Electronics
- Pico-second timing SCA in 130nm CMOS technology
- Perspective

Perspective

- The 4-channel 130nm CMOS ASIC:

  First tests ok, more test results to come shortly…

- **Next chip : Upgrade with channel discriminator, internal PLL, improve analog bandwidth, sample rate, multi-gain input stages (QIE-like)**

- Other ASIC design at the University of Chicago:

  An integrated Front-End for the Hadron Tile Calorimeter upgrade at ATLAS

  Include: 3-gain input stage, Integrator, 12-bit ADC

130nm CMOS OK for these designs so far.

Latest technologies (90nm) are faster , but require multi-gain to cope with the reduced voltage supply range:

Multi-gain switched capacitor arrays ?

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Thanks for your attention !