Large Area, High Speed Photo-detectors Readout

Jean-Francois Genat[+]

On behalf and with the help of

Herve Grabas[+], Samuel Meehan[+], Eric Oberla[+], Fukun Tang[+], Gary Varner [++], and Henry Frisch[+]

[+]University of Chicago

[++]University of Hawaii

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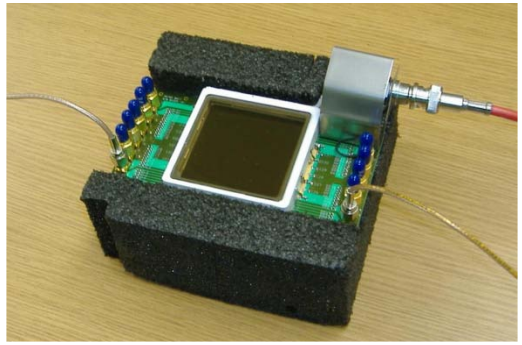
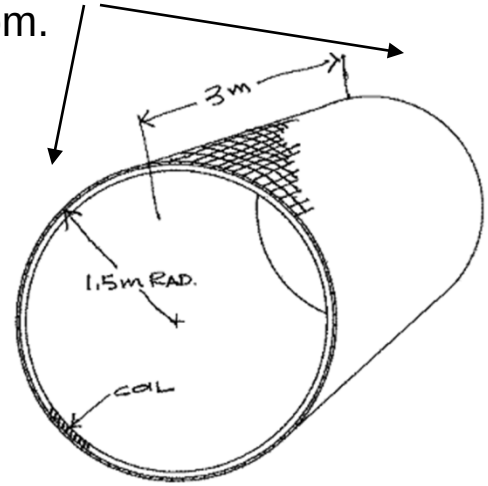
University of Hawaii at Manoa

Large Area Photo-detectors Readout

- Fast photo-detectors with delay lines readout can provide:
  - Pico-second timing
  - 2D Position



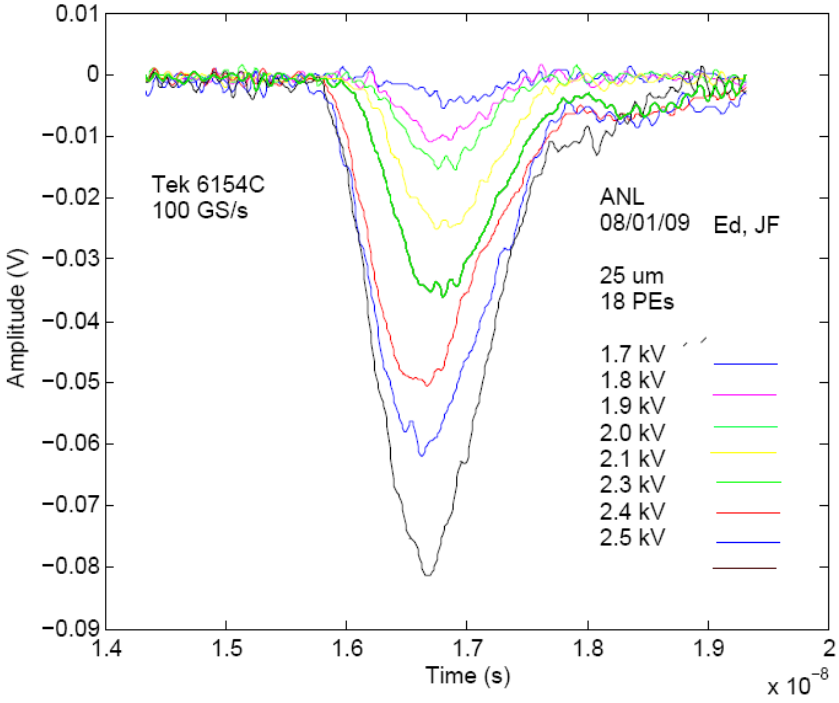
- Significant reduction of electronics channels needed for large area detectors and consequently less power, room.

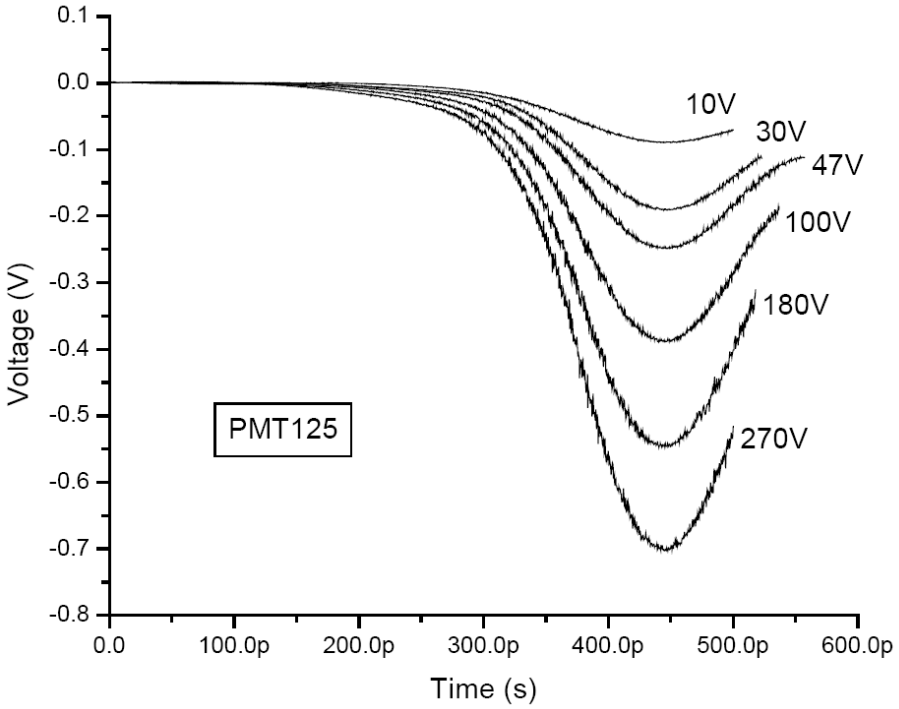


Accurate time (few ps) and position (~100μm) measurements using GHz bandwidth electronics

Micro-Channel Plates signals

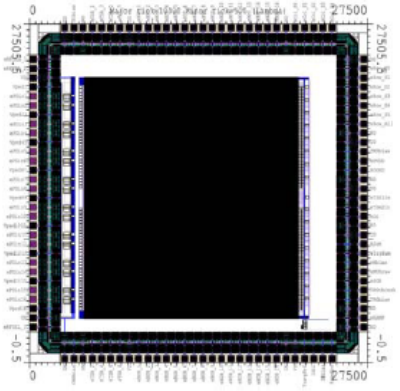
- left: 25 μm pores MCP tests at Argonne
  Bandwidth 1 GHz
- right: 6 μm pores MCP from Photek
  Bandwidth 3 GHz

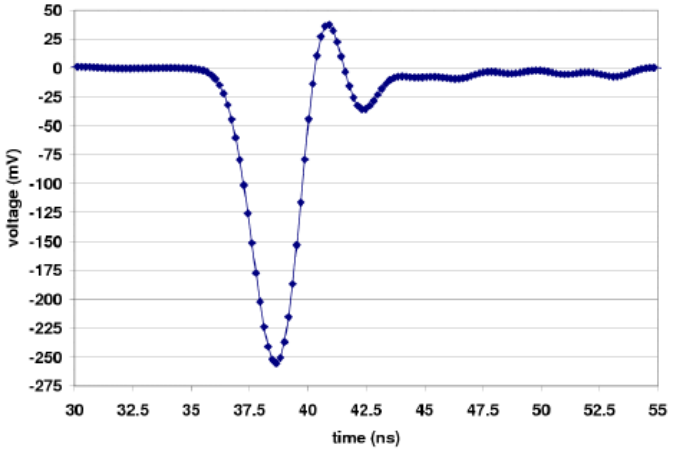


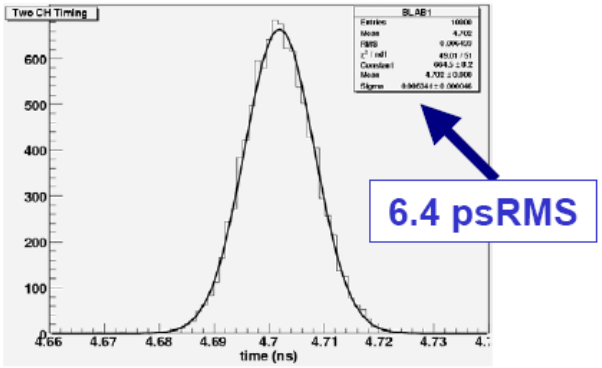


Picosecond timing

Fast sampling allows reconstructing the time of arrival to a few picoseconds knowing the waveform.

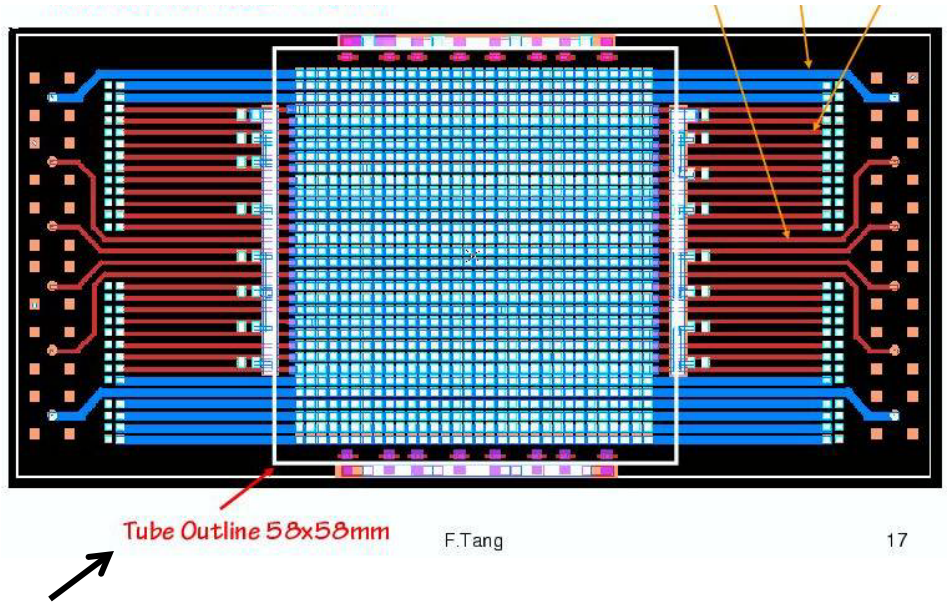






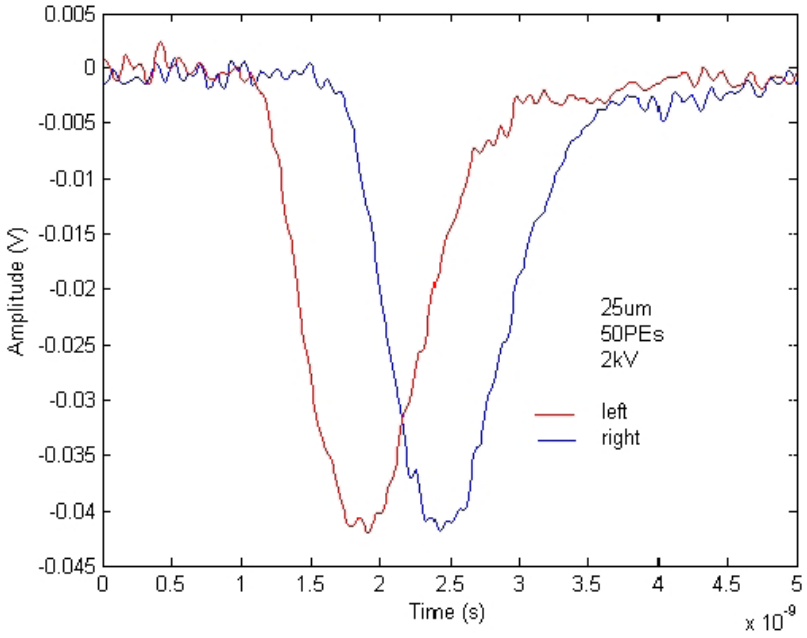
Gary S. Varner
University of Hawaii
ps Timing Workshop,
March 2008

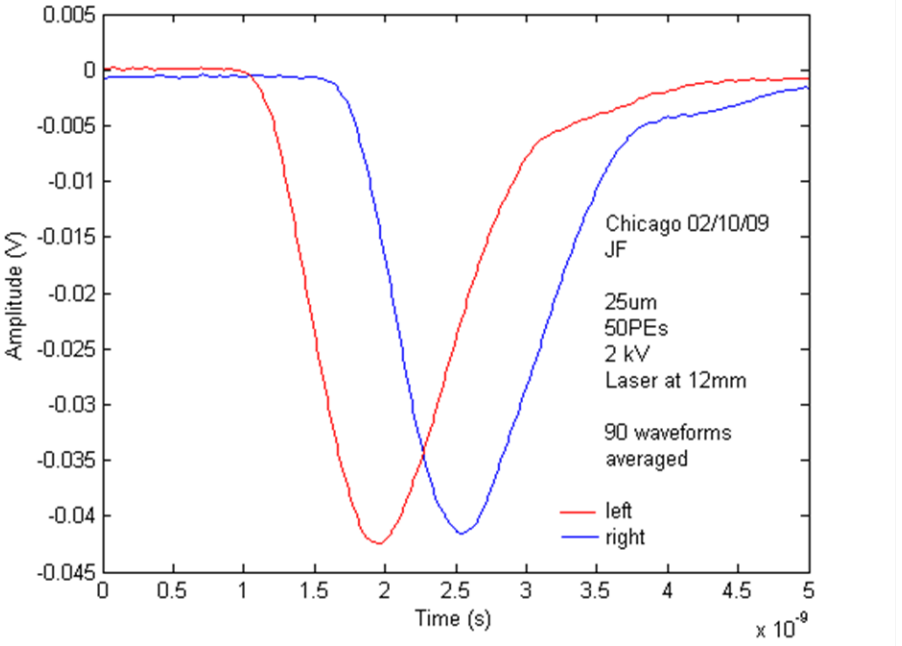
Transmission lines read at the ends



- Burle-Photonis Micro-channel plates,
- 50 Ohms matched transmission lines,
- Waveform sampling (presently fast digital oscilloscope)
- Waveform analysis (fit to waveform template)

Fast photo-detectors signals





Left: Micro-channel plate signals: two ends of a transmission line (12 cm length)
Right: Template obtained after averaging timed and scaled signals

Pulse Sampling

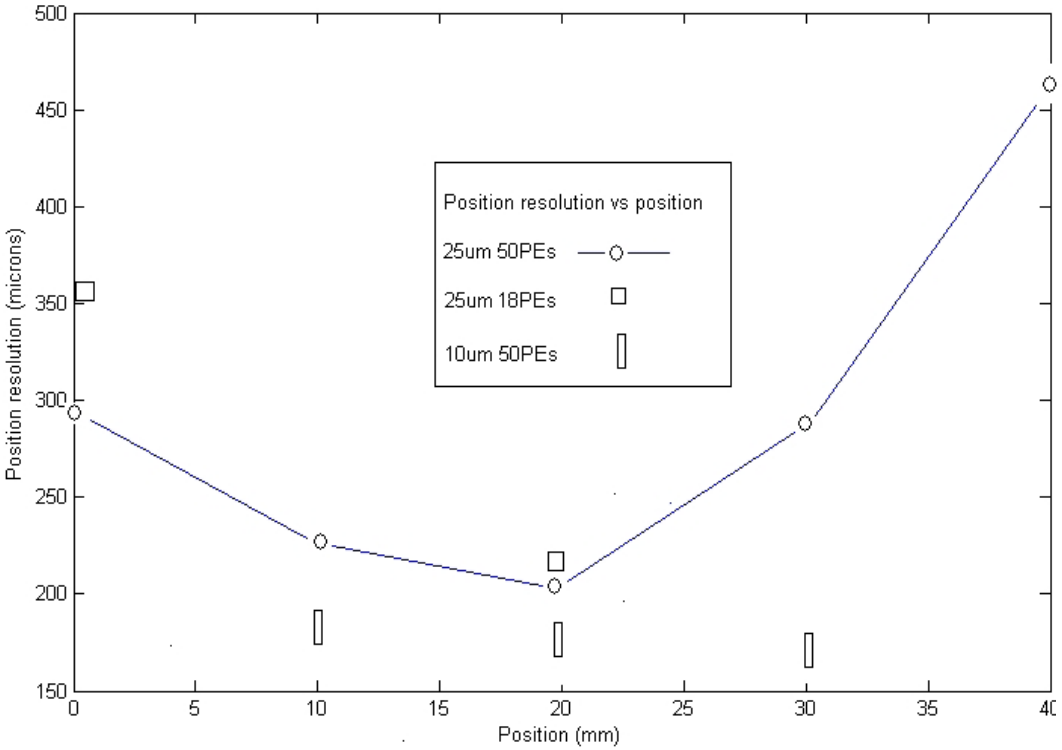
Pulse sampling allows:

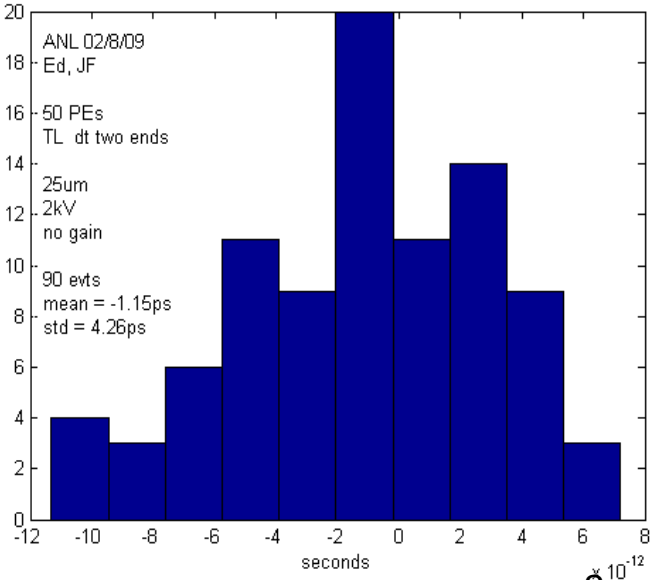
- Reconstructing charge and time accurately knowing the detector waveform using digital signal processing such as:
  - leading edge reconstruction (for timing),
  - optimum filtering (for charge).

Depending on the context and sampling rate

- Digitize on the fly for sampling rates below 1 GS/s
- Store (analog) and digitize upon trigger above 1 GS/s

Position resolution using fast timing

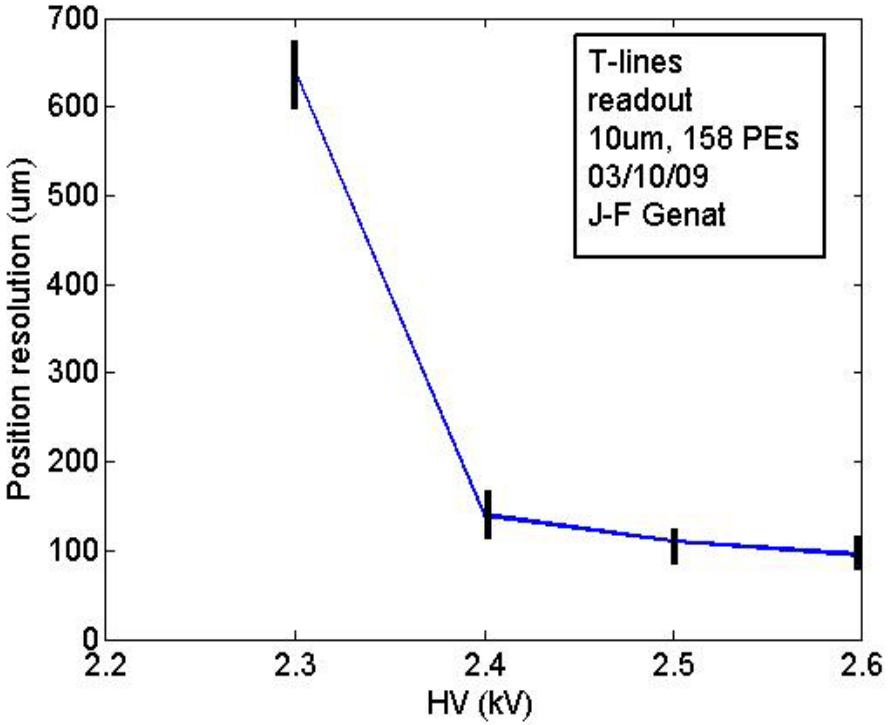


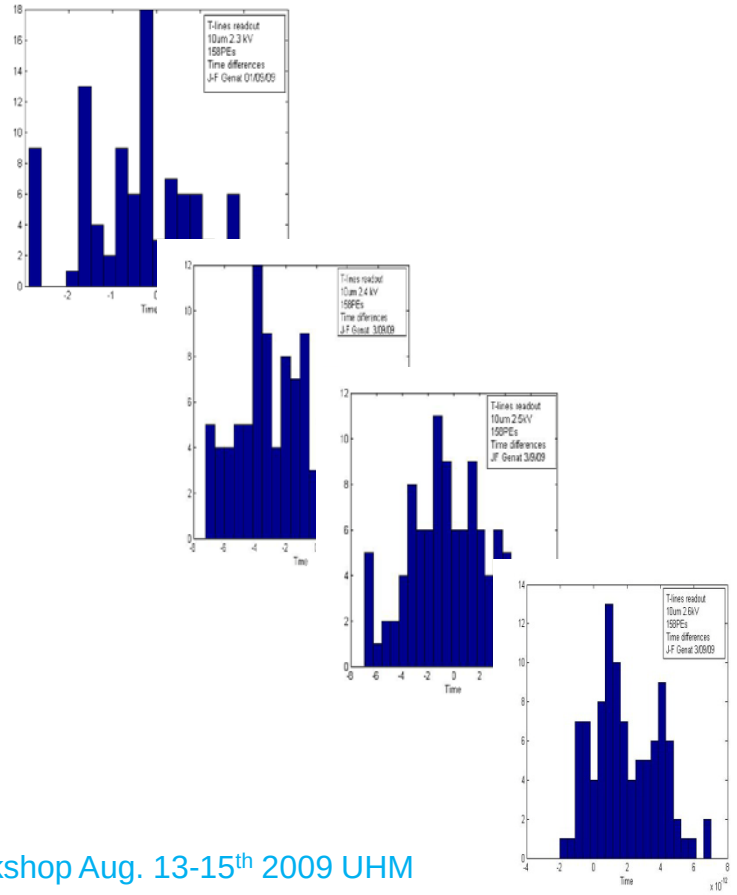


Position Resolution at 158PEs

158 PEs

HV = 2.3 kV	2.4 kV	2.5 kV	2.6 kV
Std 12.8ps	2.8ps	2.2 ps	1.95 ps
640μm	140μm	110μm	97μm





Fast Sampling Electronics Requirements

- Sampling rates of a few GS/s (analog memories)
- Integration in custom ASIC for large scale detectors ~ $10^{4\text{-}6}$ channels,
- Measure time, position and charge,
- Dynamic range,
- Full digital (serial) interface,
- Self or external trigger,
- Low power,
- High reliability and availability,
- Low cost.

Sampling Chips

State of the art:

	Sampling GHz	Bandwidth GHz	Dyn. range bits	Depth	PLL	ADC bits	Trigger
G. Varner (Hawaii)	6	1.0	10	1024	no	12	experience
S. Ritt (PSI)	6	.8	11.5	256	3.9ps	no	no
D. Breton (Orsay) + E. Delagnes (Saclay)	2.5	.3	13.4	250	20ps	no	no

Optimization for fast timing:

Sampling	10-15 GS/s
Bandwidth	> 1.5 GHz
Dyn. Range	8-10bit
Depth	256

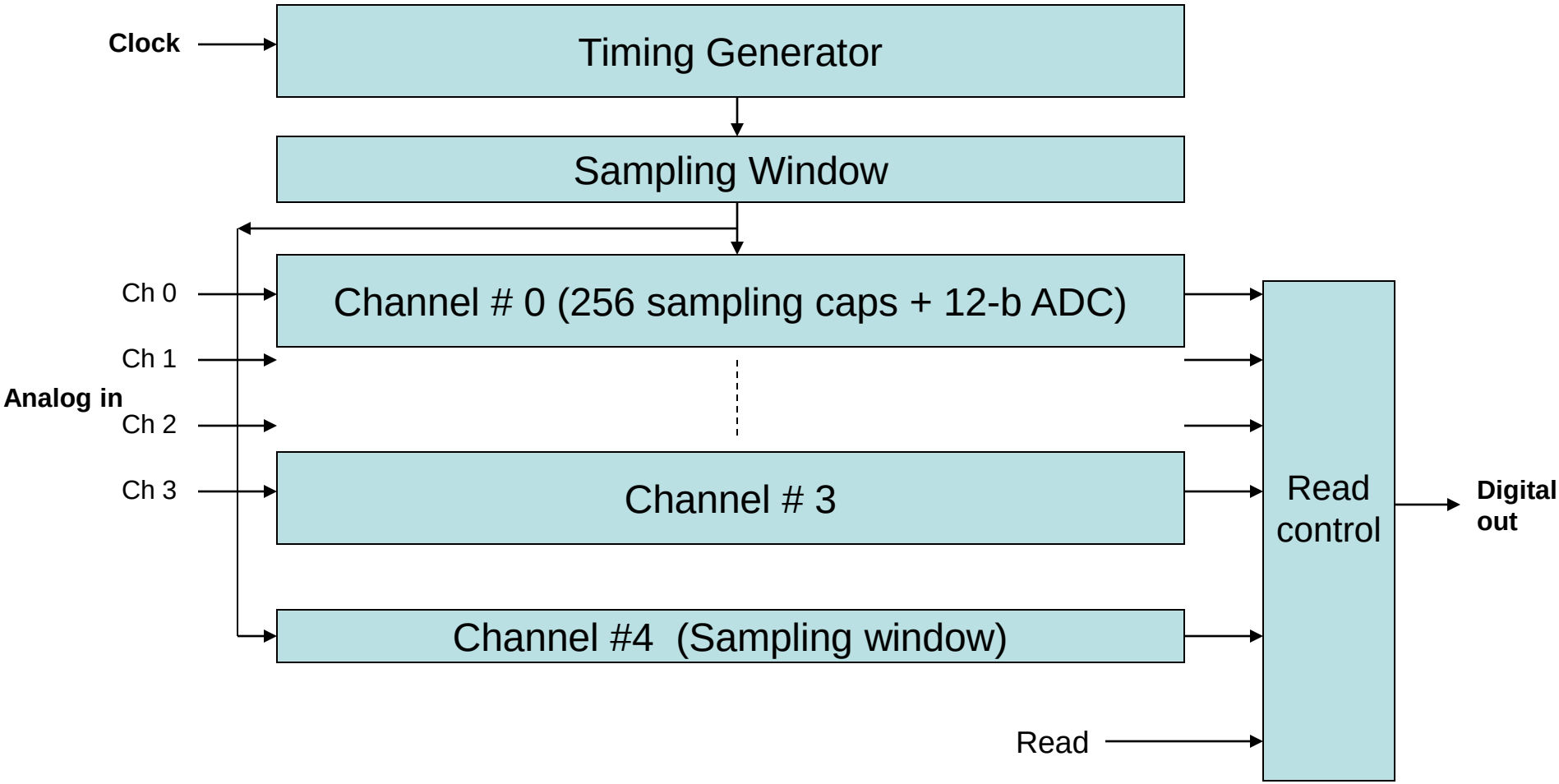
Sampling chips, this proposal

	Hawaii			Saclay/Orsay			PSI			This proposal
	Varner	Lab 3	Planned Blab2	Delagnes	Sam	Planned	S.Ritt	DRS3	DRS4	
				Breton						
Sampling rate		20 MHz-3.7 GHz	1-10 GHz		0.7-2.5 GHz	10 GHz		10 MHz-5 GHz	5 GHz	15 GHz
Bandwidth (3db)		900 MHz	850 MHz		300 MHz	650 MHz		450 MHz	950MHz	> 2 GHz
Channels		9	16		2			12/6/2/1	8/4/2/1	16-32
Triggered mode		Common stop	On sums		Common stop			Common stop	Common stop	Channel trigger
Resolution			10-bit		11.6 bit			11.6 bit	11.5 bit	8-10-bit
Samples		256	4/8 x 512		256	2048		1024-12288	1024-8192	256
Clock		33 MHz	33 MHz		65 MHz			20 MHz	fsamp/2048	60 MHz
Max latency		50us			5ms			0.6ms		
Input Buffers			TIA 5kOhms		Yes	No		No	No	No
Differential inputs		No	Pseudo		Yes			Yes	Yes	No
Input impedance		50 Ohms Ext	50/70 Ohms		> 10 Mohms				7-11pF	50 Ohms
Readout clock					16 MHz			33 MHz	33 MHz	30 MHz
Readout time		150μs	512μs					30ns * n sples	30 ns * n sples	25ns * n samples
Locked delays		Ext DAC	Ext PLL		Int DLL			Ext PLL	Int PLL	Int PLL
On-chip ADC		Yes	1 GHz Wilkinson		No			No	No	Yes
R/W simultaneous			Yes		No			No	Yes	No
Power/ch		50 mW	20mW/sple 2mW/rd		150 mW			2-8mW	2-20mW	
Dynamic range			1mV/1V		0.65mV-2 V			0.35mV/1.1V	.35mV/1V	1V
Xtalk		average <10%	< 0.1%		0.30%			< 0.5%	< 0.5%	
Sampling jitter					40ps			200ps (Ext PLL)		10ps
Power supplies		-tbd/2.5V	-tbd/2.5V					2.5V	2.5V	1.2V
Process		TSMC .25	TSMC .25		AMS .35	AMS .18		UMC .25	UMC .25	IBM .13
Chip area		2.5mm2	10 mm2		10mm2			25mm2	25mm2	1mm2/ch
Temp coeff		0.2%/◦C						5e-5/◦C	75uV/◦C /25ppm/◦C	
Cost/channel			500$/40 10$/2k		15.7$/12k				10-15$	

Prototype Sampling ASIC Minimum specifications.

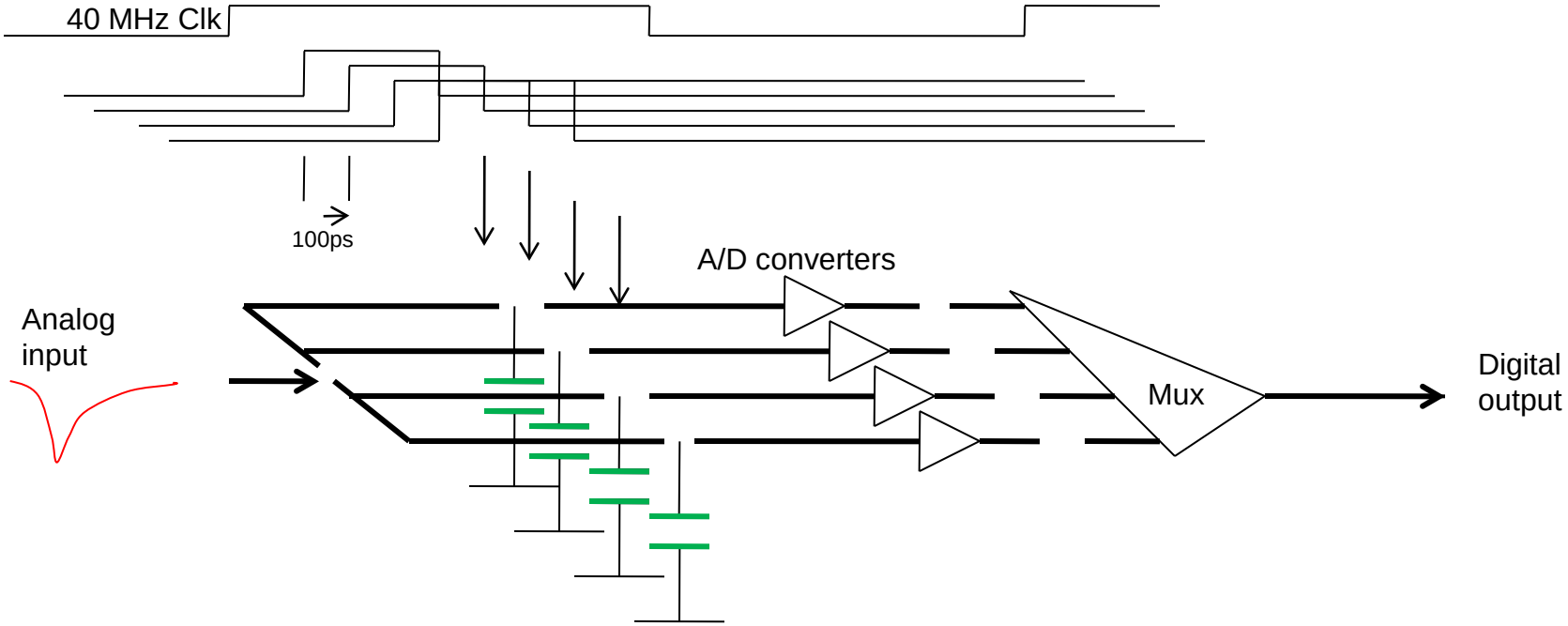
- Sampling rate 10 - 15 GS/s
- Analog Bandwidth 2 GHz
- Dynamic range 0.7 V
- Sampling window adjustable 500 ps - 2 ns
- Sampling jitter 10 ps
- Crosstalk 1%
- DC Input impedance 50 Ω internal
- Maximum read clock 40 MHz
- Conversion clock Adjustable 1-2 GHz internal ring oscillator. Minimum conversion time 2us.
- Readout time 4 x 256 x 25 ns=25.6 μs
- Power 40 mW / channel
- Power supply 1.2 V
- Process IBM 8RF-DM (130nm CMOS)

Block diagram



Modes

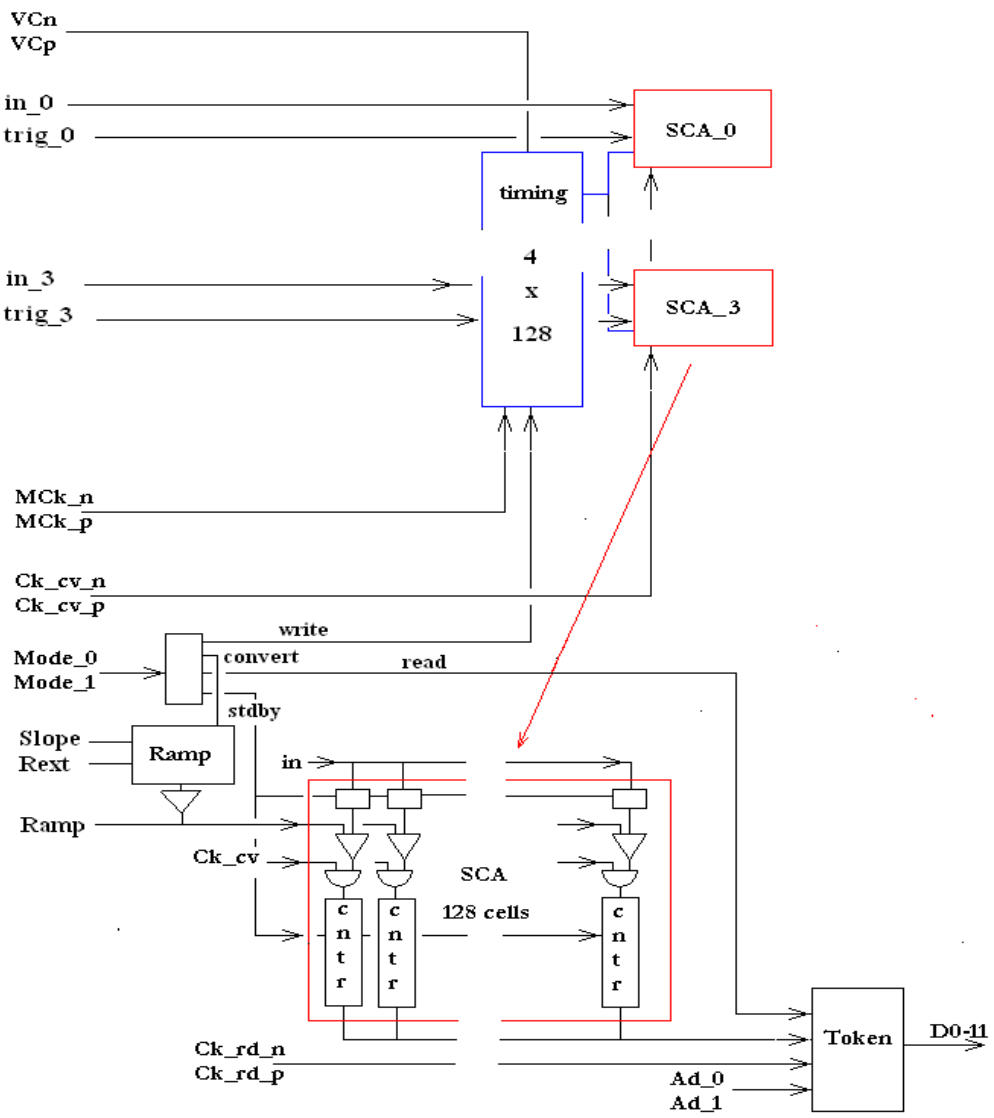
-1 Write: The timing generator runs continuously, outputs 256 phases 100ps spaced.
Each phase (sampling window) controls a write switch.
The sampling window's width is programmable (250ps-2ns)



-2 A/D Conversion takes place upon a trigger that opens all the write switches and starts 256 A/D conversions in parallel (common single ramp).
Data are available at after 2 μs (2GHz counters)

-3 Read occurs after conversion at 150 MHz (4 channels need 6 μs)

More details



Functions

The chip includes

- 4 channels of full sampling (256 cells)
- 1 channel of sampling cell to observe the sampling window

Test structures:

- Sampling cell,
- ADC Comparator,
- Ring Oscillator

Sampling cell

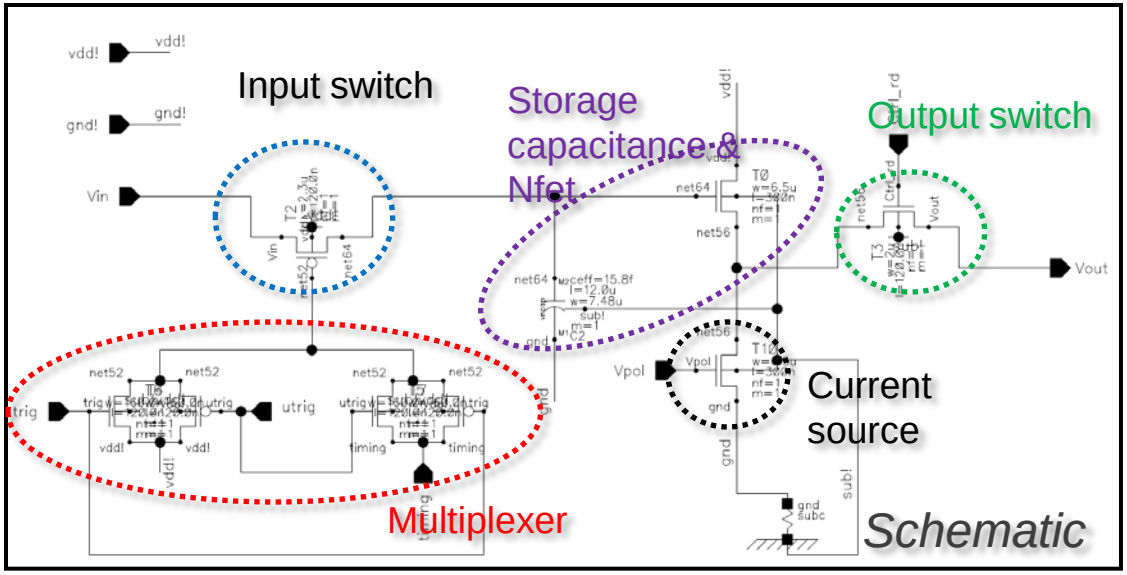
Capacitance value: 33,2fF

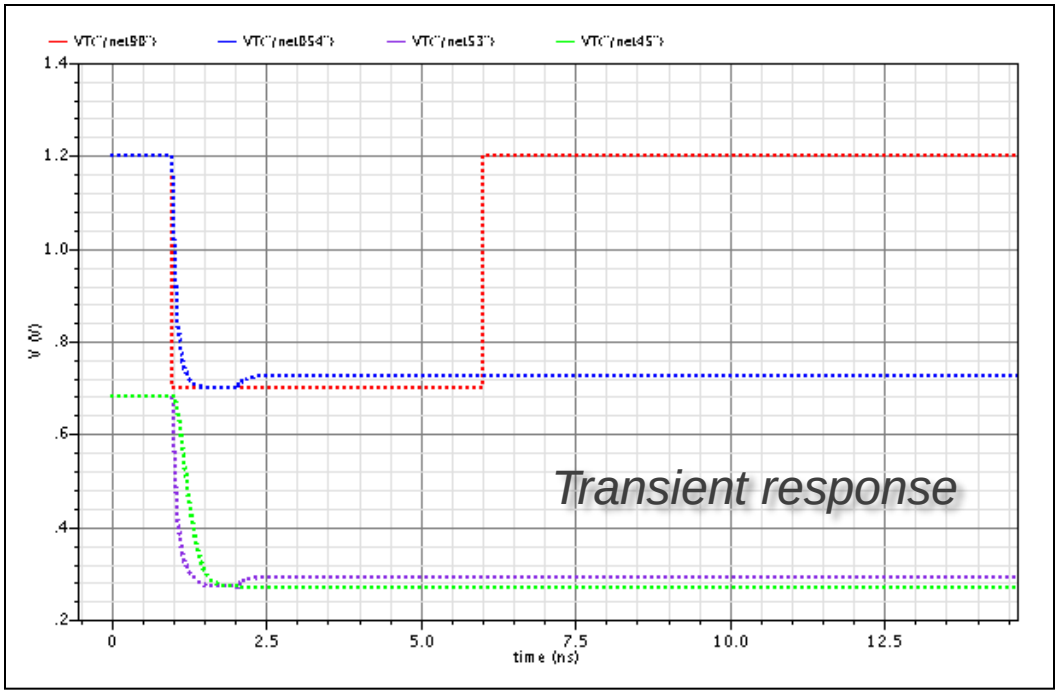
Switch resistance: 1kΩ

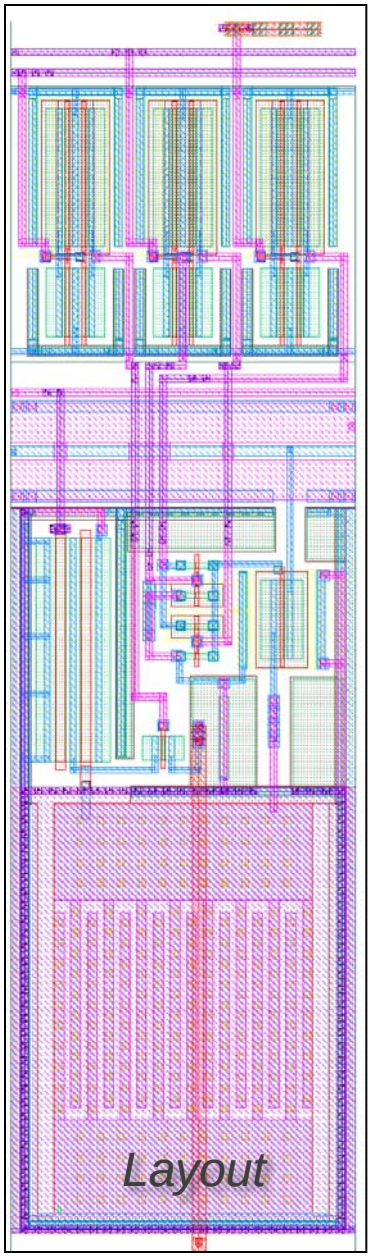
1-cell bandwidth: 1/2πRC = 10GHz

256 cells post-layout

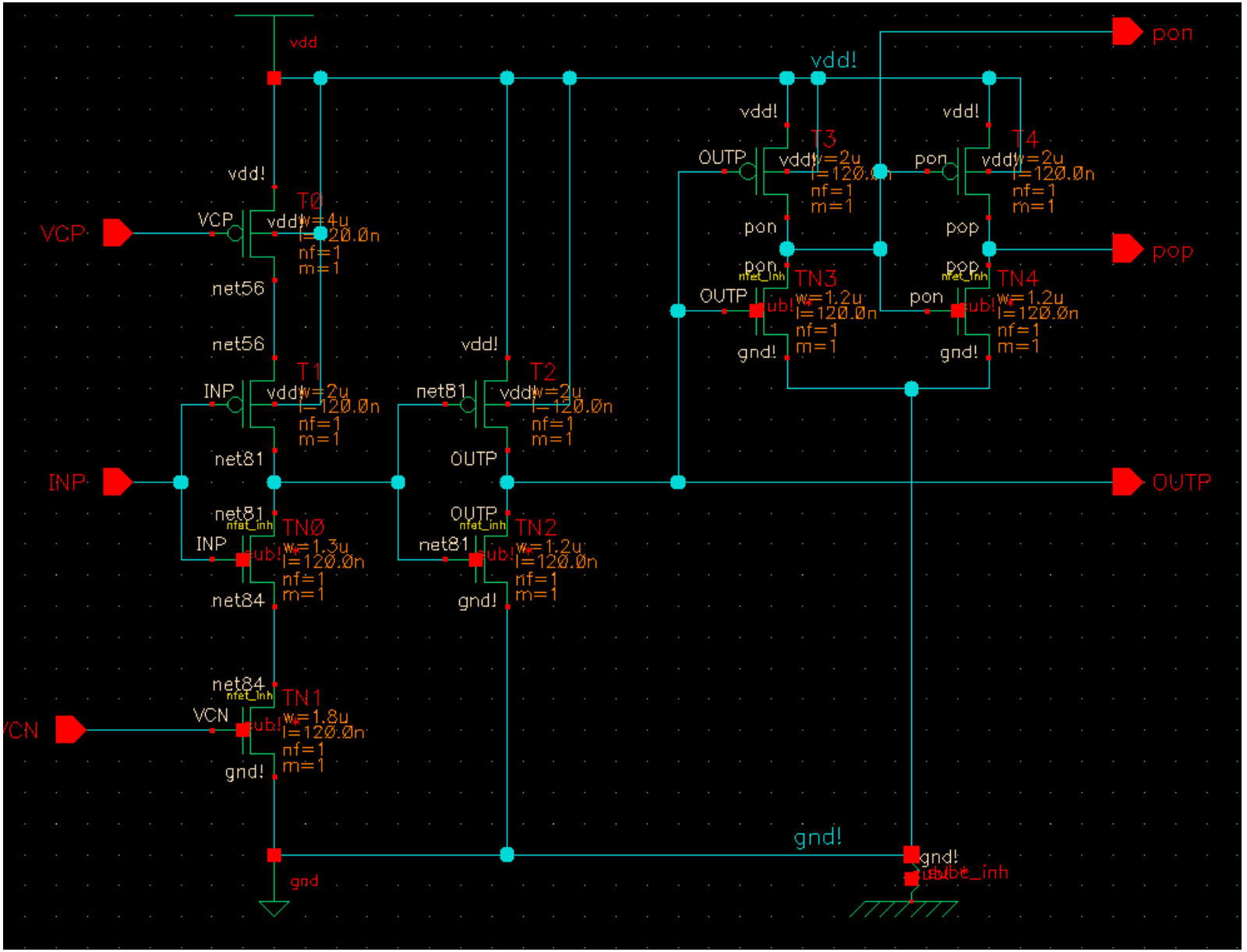
bandwidth = 3GHz



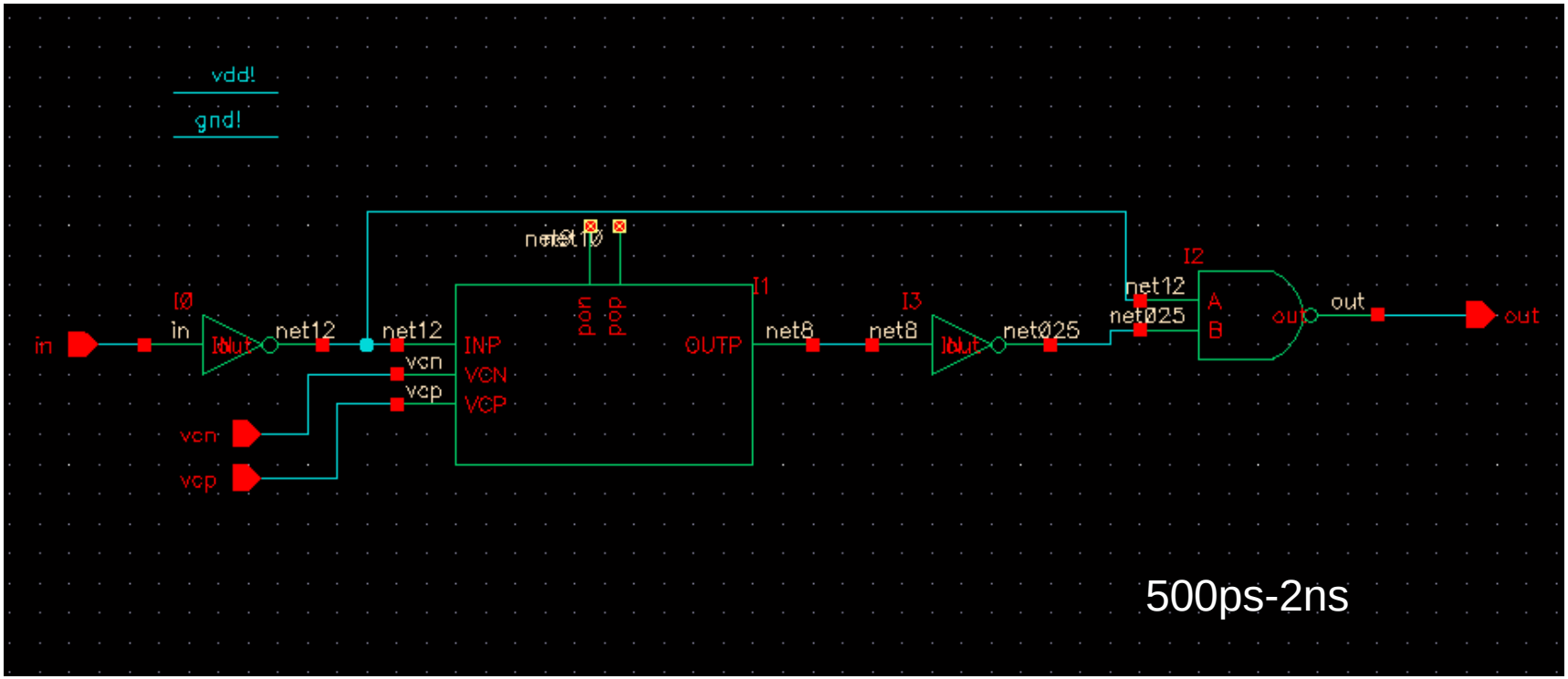




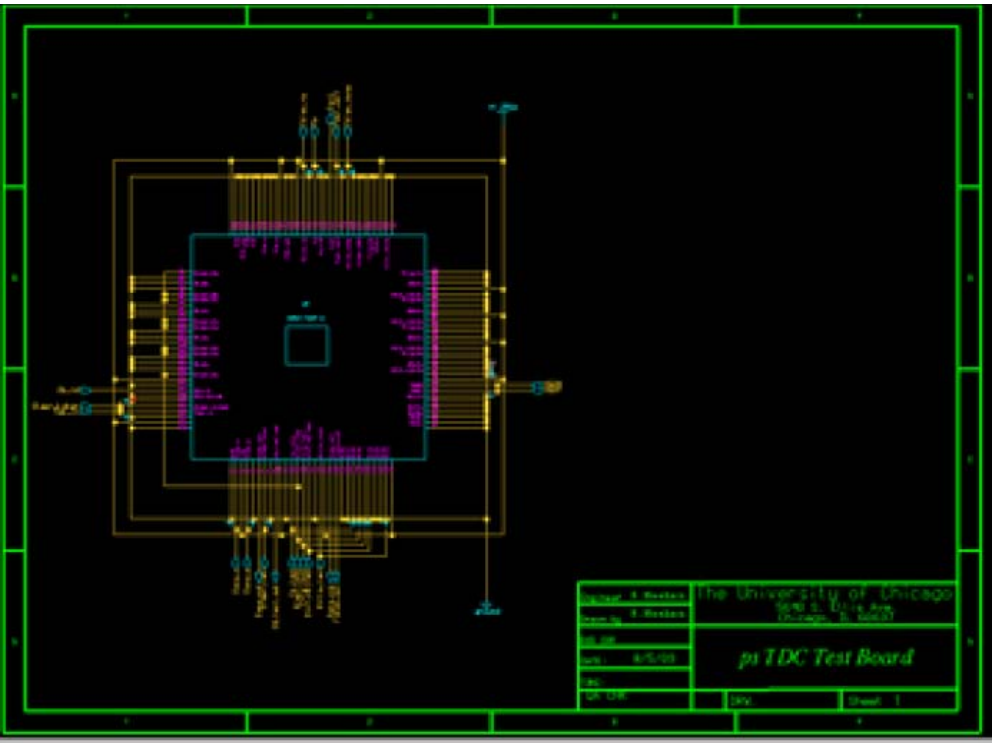
Delay generator (1 / 256 cells)



Sampling window (1/256)



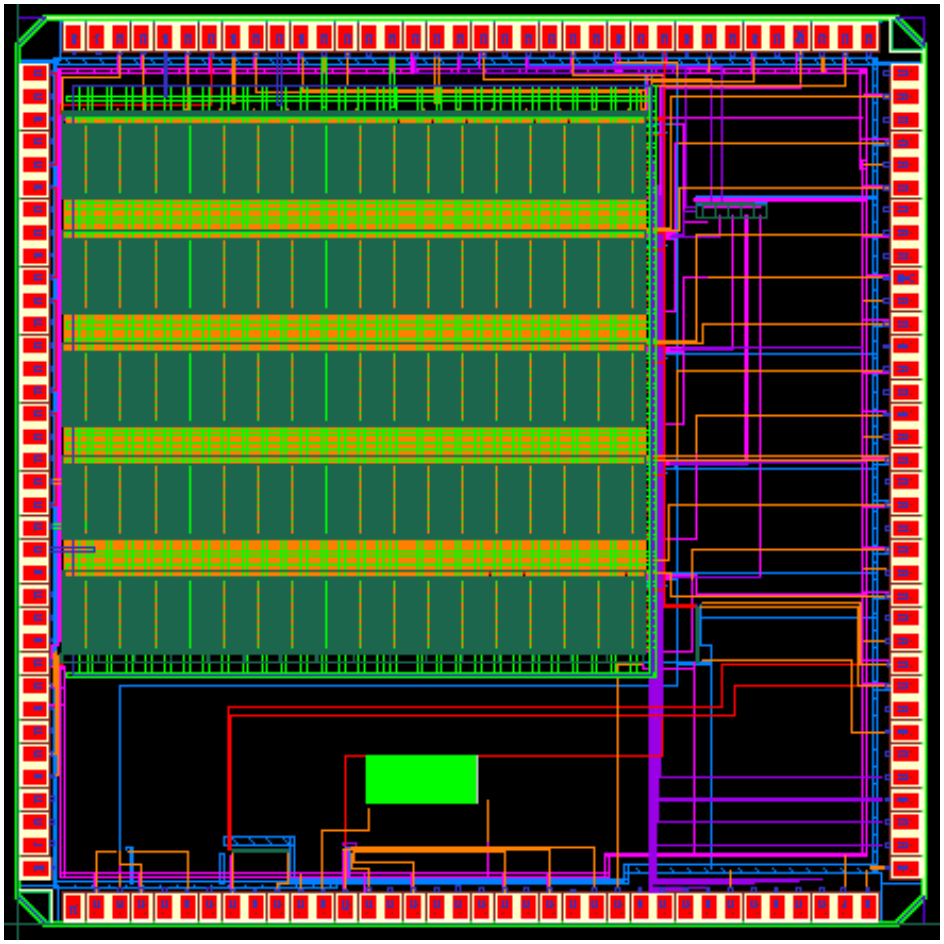
1st Test Board for Sampling Chip



Test Board Schematic

- DC tests using packaged chip from MOSIS (~1x1 in^2)
- Board layout under development
- 24 pins – 19 inputs, 5 outputs
  - Determine DC power of chip test structures
  - Observe functionality of:
    - Token
    - Ramp
    - Ring Oscillator
    - Comparator
    - Sampling Cell

Chip layout



144 pads, 4 x 4 mm^2

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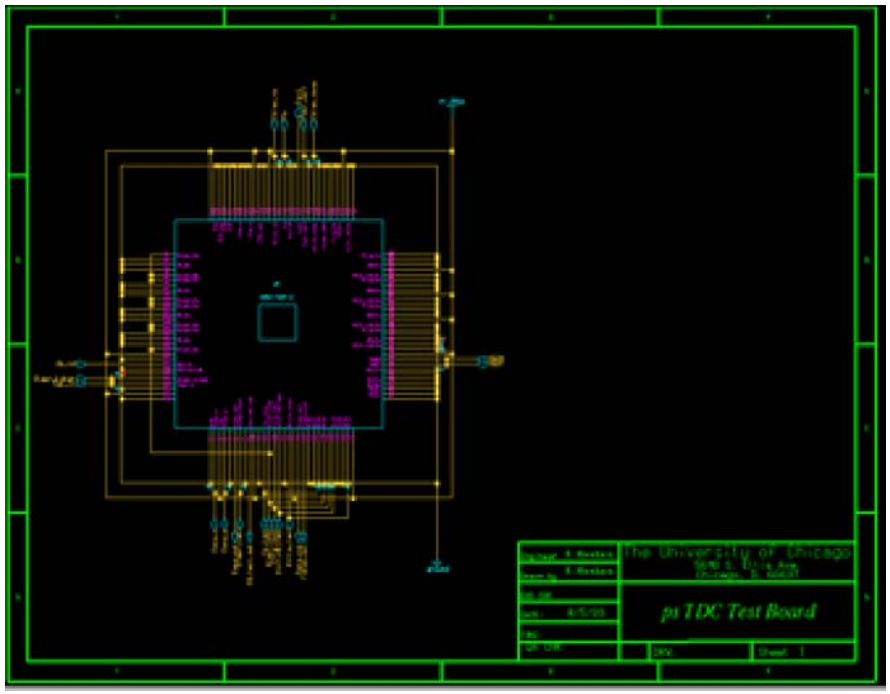

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Full test board for Sampling Chip

- 4 bare chips wire bonded to PCB
- control FPGA
- VME and/or USB interface
- IEEE 488 interface to:
  - Fast arbitrary waveform generator Tek 7102
  - Oscilloscope Tek 6154
  - LeCroy 9210 pulser
- LabView test software
- Full chip characterization

Next chip

- 16 channels
- Input discriminators
- Faster clock (> 100 MHz)
- Larger sampling rate (20-30 GS/s)
- Phase lock on clock
- Digital zero suppression

Conclusion

- First 130nm CMOS analog memory ASIC sent to MOSIS July 28th

Expect 15 GS/s max sampling rate

2 GHz analog bandwidth

A few ps timing resolution with MCP signals

- Next chip:
  - 16 channels, Phase-lock, Zero suppression