The Development of Ultra-fast Timing and the Application of HEP Technologies to Biomedical Imaging:

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OUTLINE

1. Introduction: Role of TOF in HEP, MI; unique expertise developed in HEP should be more widely available to society.
2. Three Key Developments since the 60's: a) Fast MCP's, 200-GHZ electronics, and Electronics Simulation Tools;
3. HEP Needs: Particle ID and Flavor Flow, Heavy Particles, Displaced Vertices, Photon Vertex Determination;
4. MI Needs: 3D localization (TOF); real-time filtering, reconstruction.
5. The Need for End-to-End Simulation in Parallel;
6. What We've Achieved So Far on UC, LDRD, and DOE-ADR seed funding:
7. Proposal Request and Milestones

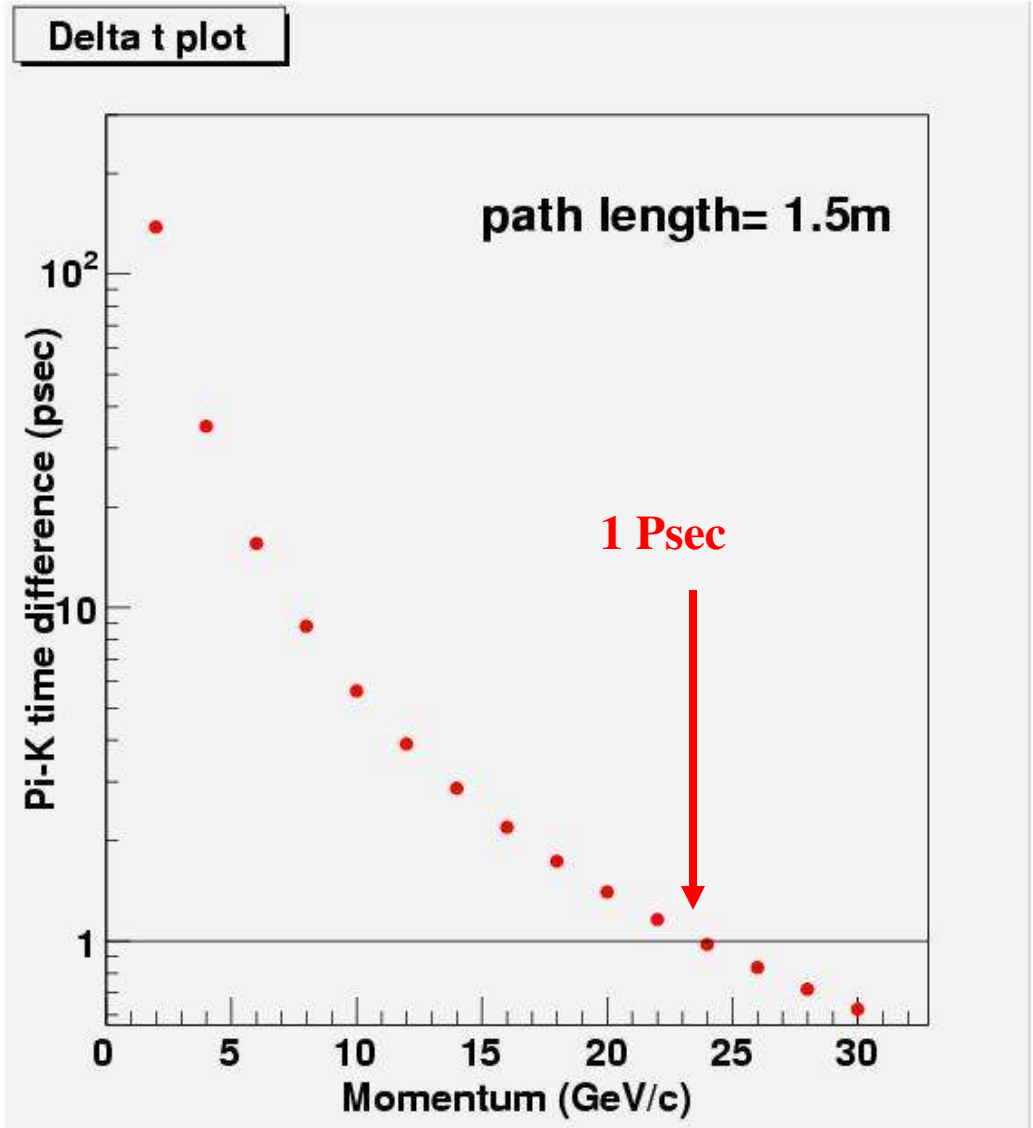
Introduction

- Resolution on time measurements translates into resolution in space, which in turn impact momentum and energy measurements.
- Silicon Strip Detectors and Pixels have reduced position resolutions to ~10 microns or better.
- Time resolution hasn't kept pace- not much changed since the 60's in large-scale TOF system resolutions and technologies (thick scint. or crystals, PM's, Lecroy TDC's)
- Improving time measurements is fundamental , and can affect many fields: particle physics, medical imaging, accelerators, astro and nuclear physics, laser ranging, ….
- Need to understand what are the limiting underlying physical processes- e.g. source line widths, photon statistics, e/photon path length variations.
- Initial studies give <1 psec for HEP; we guess ~30 psec

Possible Collider/ILC Applications

- Separating b from b-bar in measuring the top mass (lessens combinatorics => much better resolution)
- Identifying csbar and udbar modes of the W to jj decays in the top mass analysis
- Separating out vertices from different collisions at the LHC in the z-t plane
- Identifying photons with vertices at the LHC (requires spatial resolution and converter ahead of the TOF system
- Locating the Higgs vertex in H to gamma-gamma at the LHC (mass resolution); also missing mass Higgs searches
- Kaon ID in same-sign tagging in B physics (X3 in CDF Bs mixing analysis)
- Fixed target geometries- LHCb, Diffractive LHC Higgs, (and rare K and charm fixed-target experiments)
- Super-B factory (Nagoya Group, Va'vra at SLAC)
- Strange, Charm, Beauty and Baryon Flow in Heavy Ion Collisions, Etc

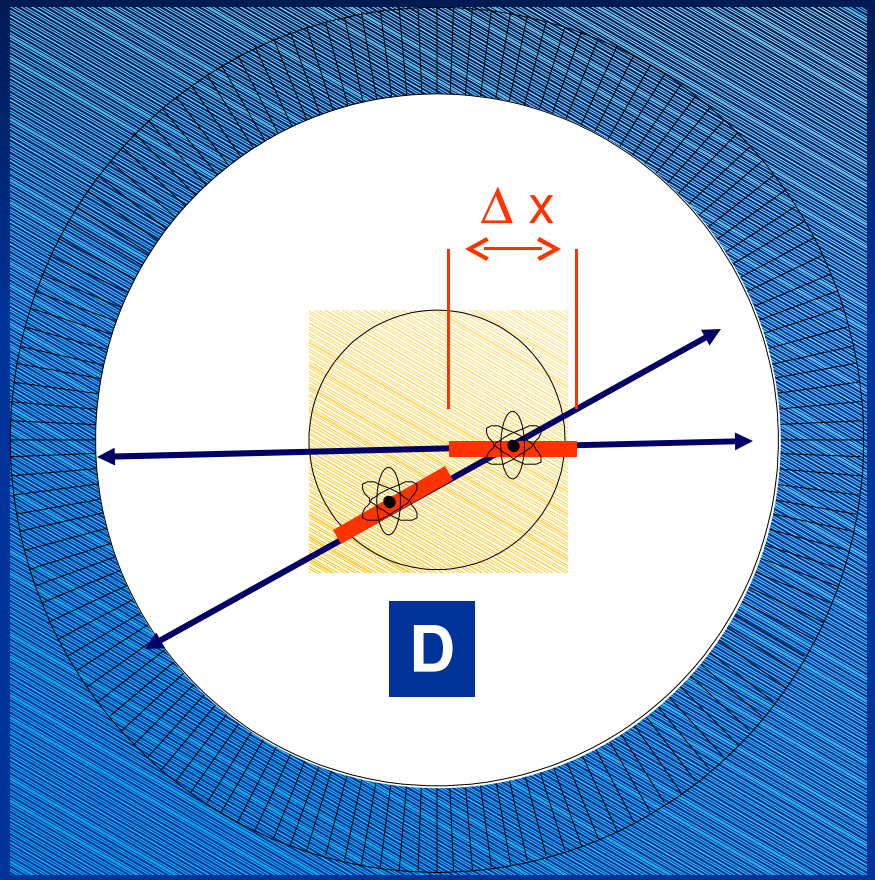
K-Pi Separation over 1.5m



Assumes perfect momentum resolution (time res is better than momentum res!)

Time-of-Flight Tomography

Slide from Chin-Tu Chen (UC) talk at Saclay Workshop



- Can localize source along line of
  depends on timing resolution of detectors
- *weighted back-projection along line-of-response (LOR)*

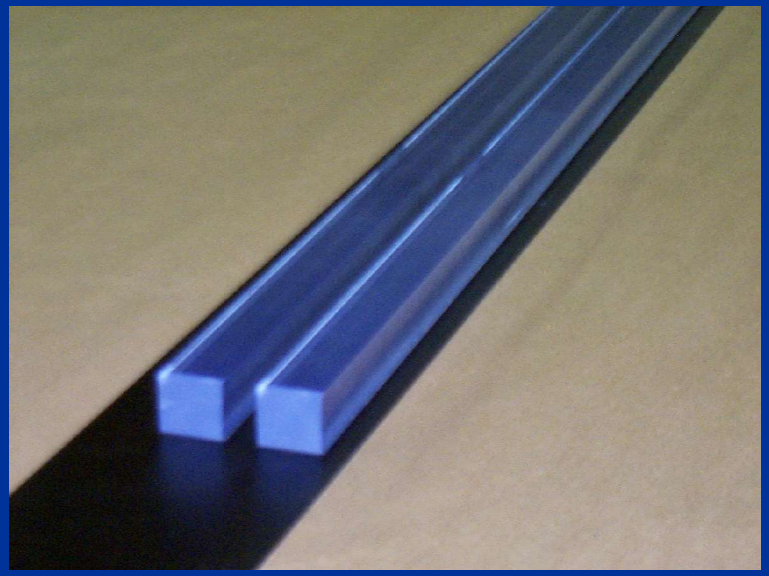
Δx = uncertainty in position along LOR

$= c \cdot \Delta t/2$

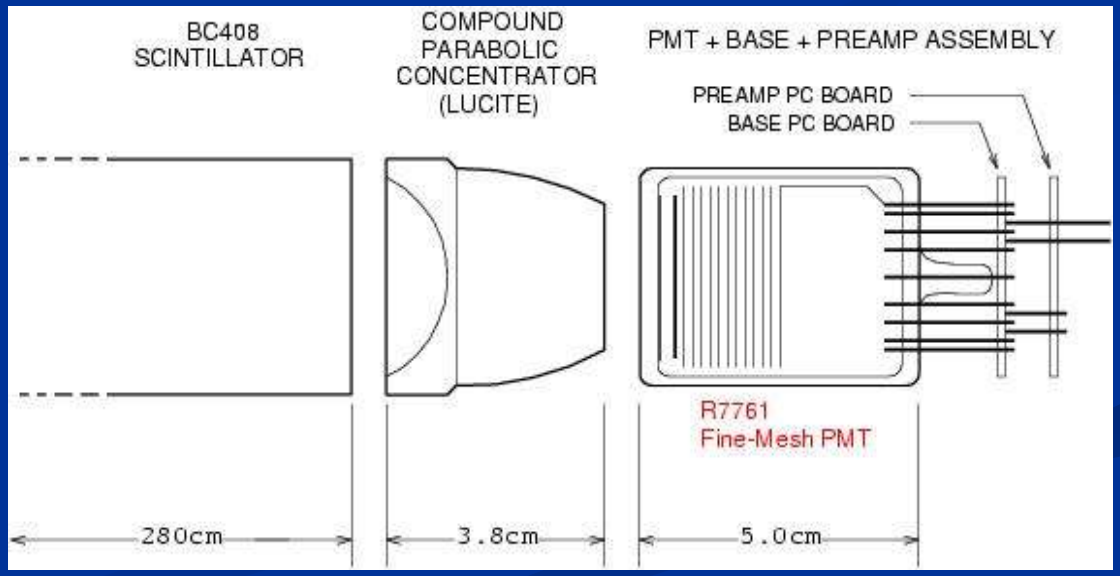
Why has 100 psec been the # for 60 yrs?

Typical path lengths for light and electrons are set by physical dimensions of the light collection and amplifying device.

These are now on the order of an inch. One inch is 100 psec. That's what we measure- no surprise! (pictures from T. Credo)

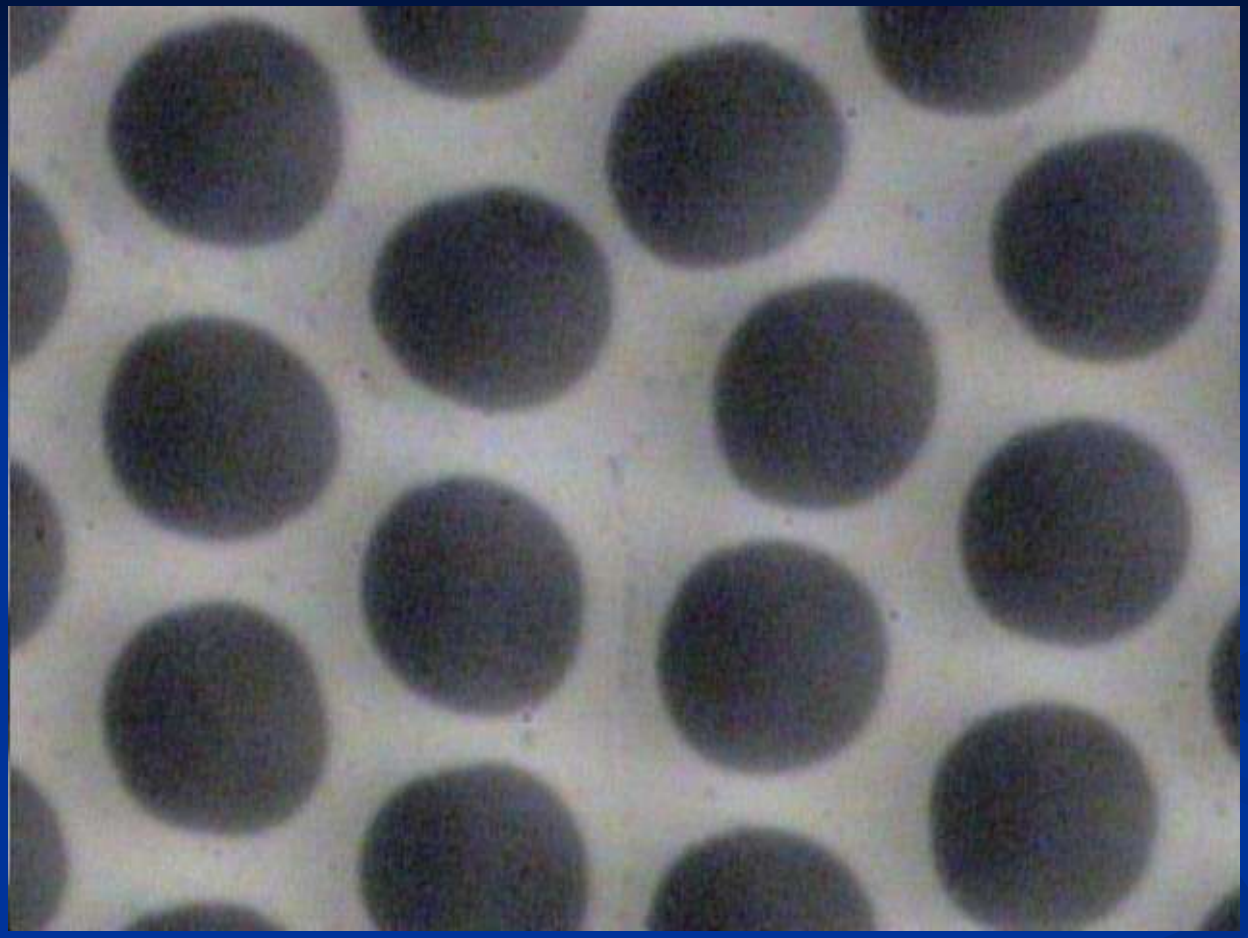


Typical Light Source (With Bounces)



Typical Detection Device (With Long Path Lengths)

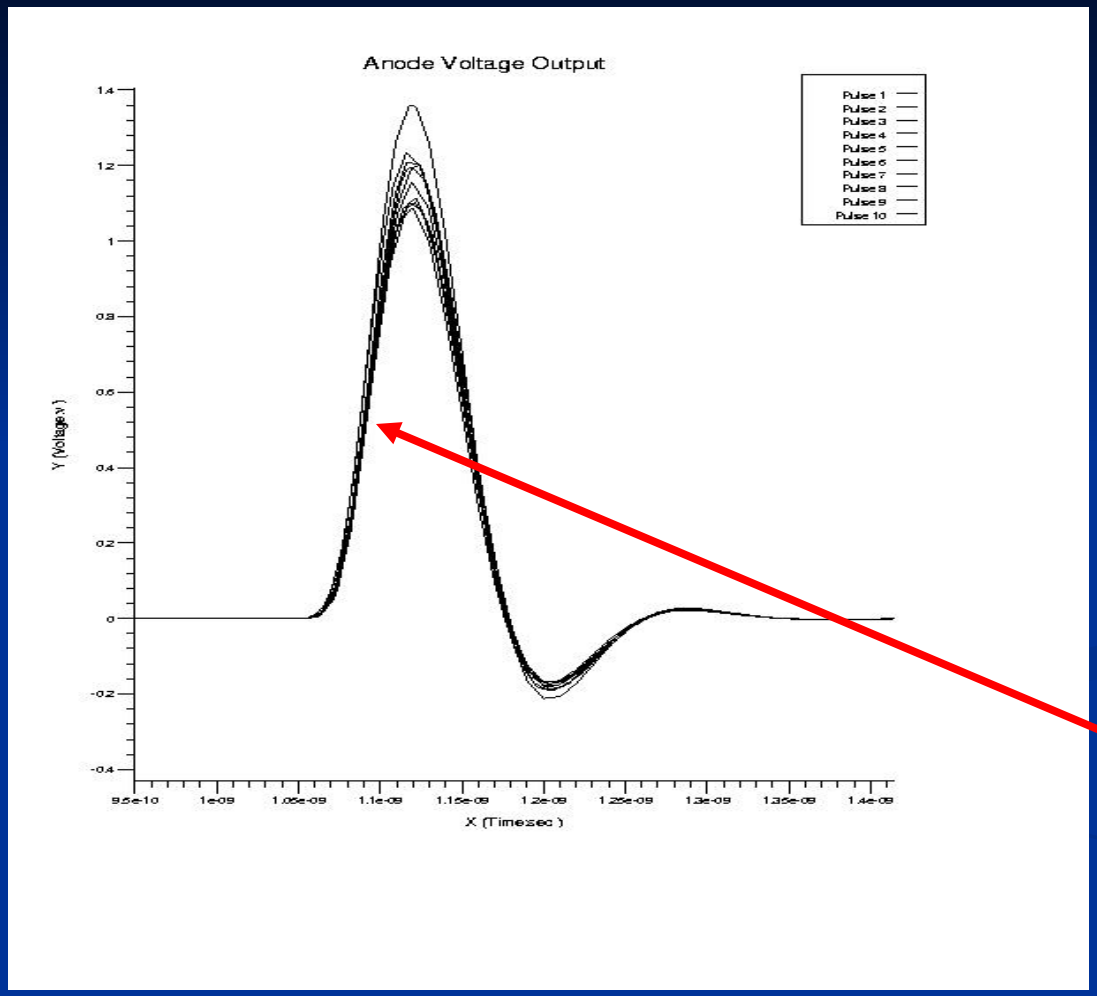
Major advances for TOF measurements:



Micro-photograph of Burle 25 micron tube- Greg Sellberg (Fermilab)

1. Development of MCP's with 6-10 micron pore diameters

Major advances for TOF measurements:

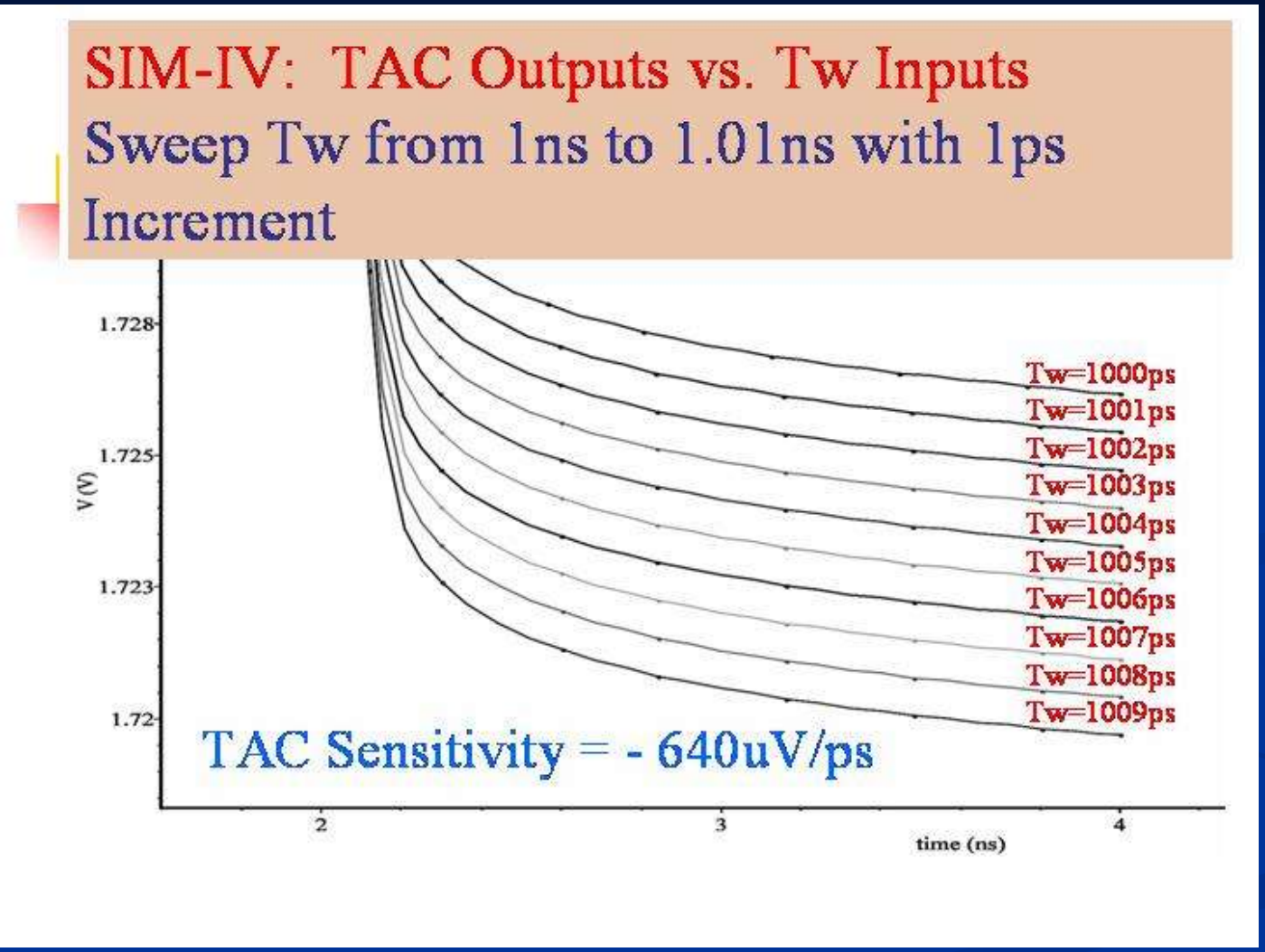


Output at anode from simulation of 10 particles going through fused quartz window- T. Credo, R. Schroll

Jitter on leading edge 0.86 psec

2. Ability to simulate electronics and systems to predict design performance

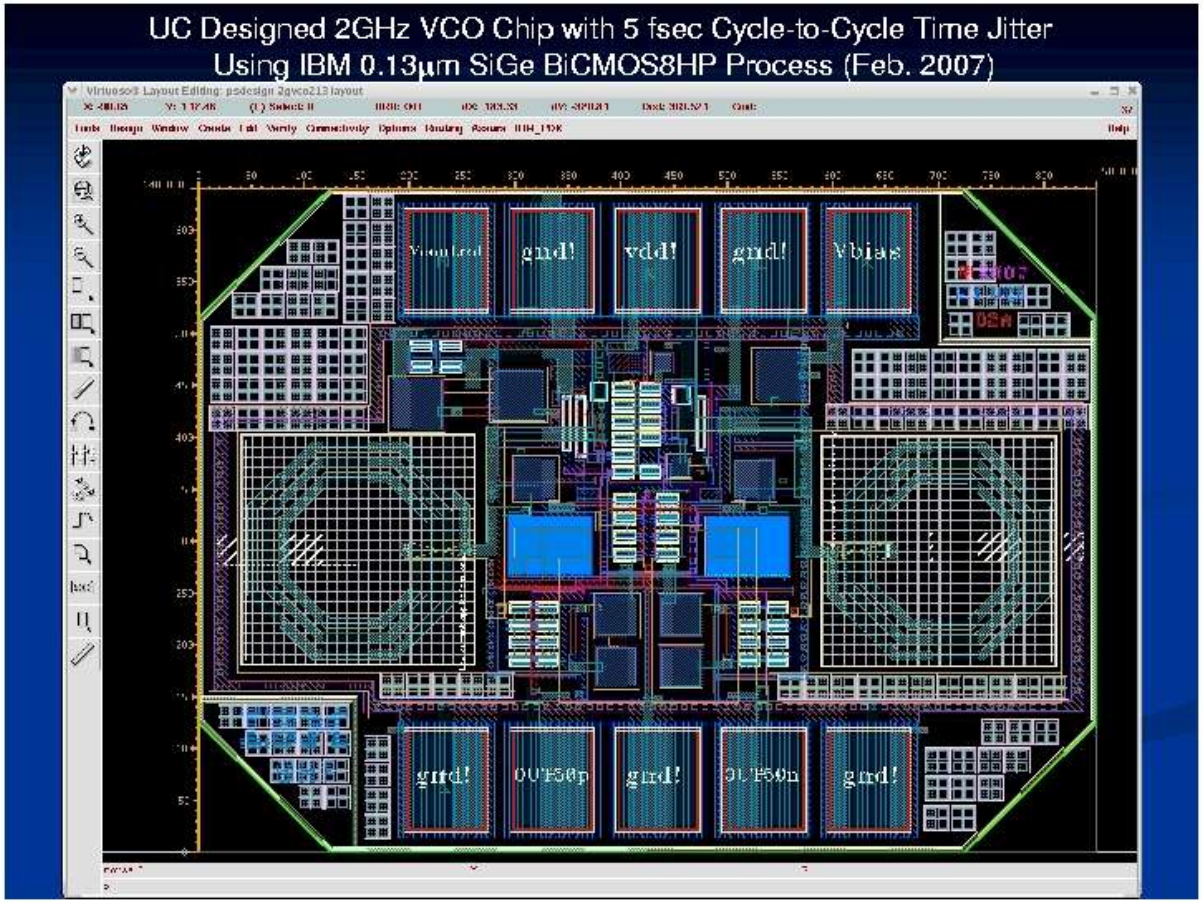
Major advances for TOF measurements:



Simulation with IHP Gen3 SiGe process- Fukun Tang (EFI-EDG)

3. Electronics with typical gate jitters << 1 psec

Major advances for TOF measurements:



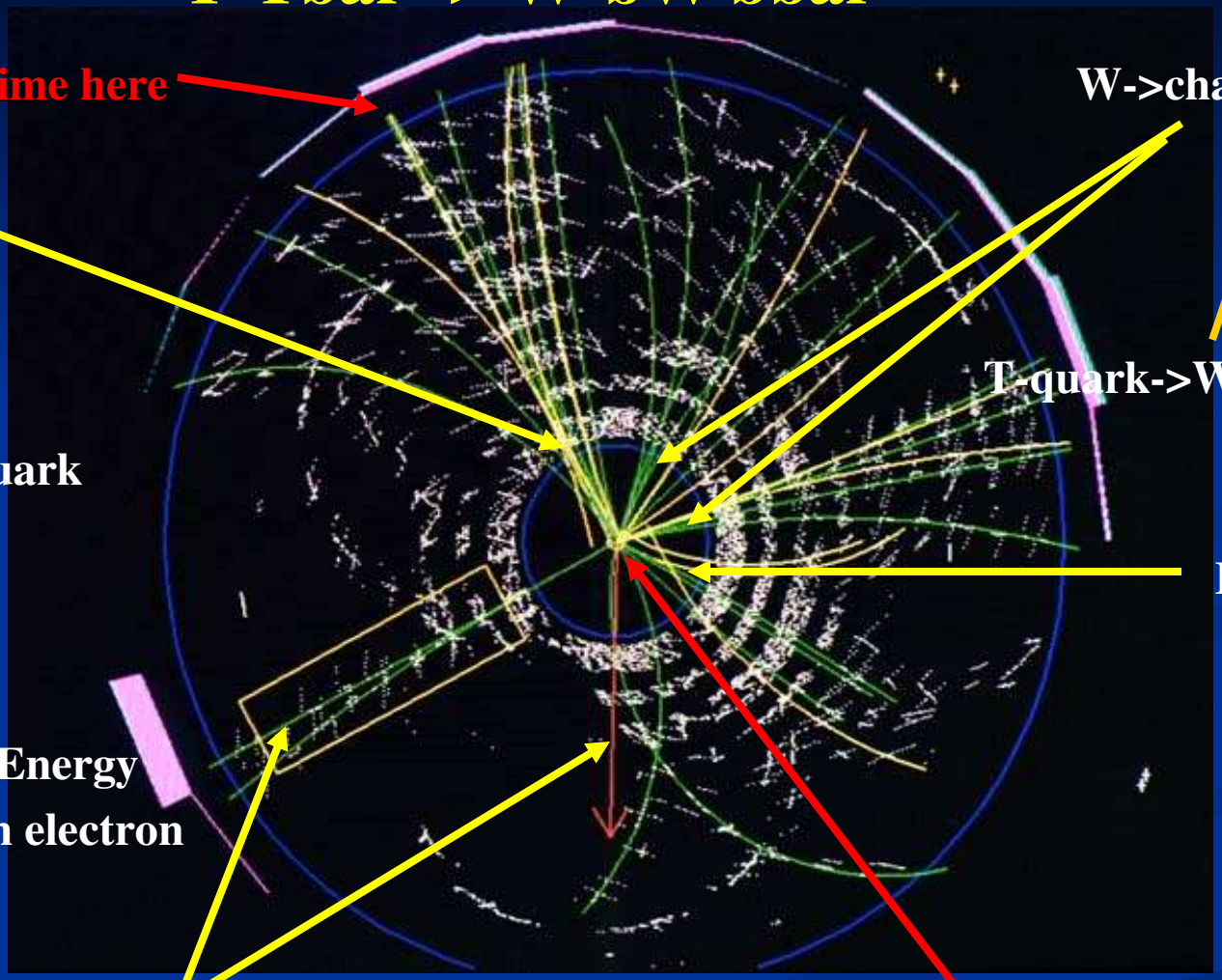
Most Recent work-

IBM 8HP SiGe process See talk by Fukun Tang (EFI-EDG) at Saclay

3a. Oscillator with predicted jitter < 100 femtosec (!) (basis for PLL for our 200:1 time-stretcher front-end chip) .

A real CDF Top Quark Event

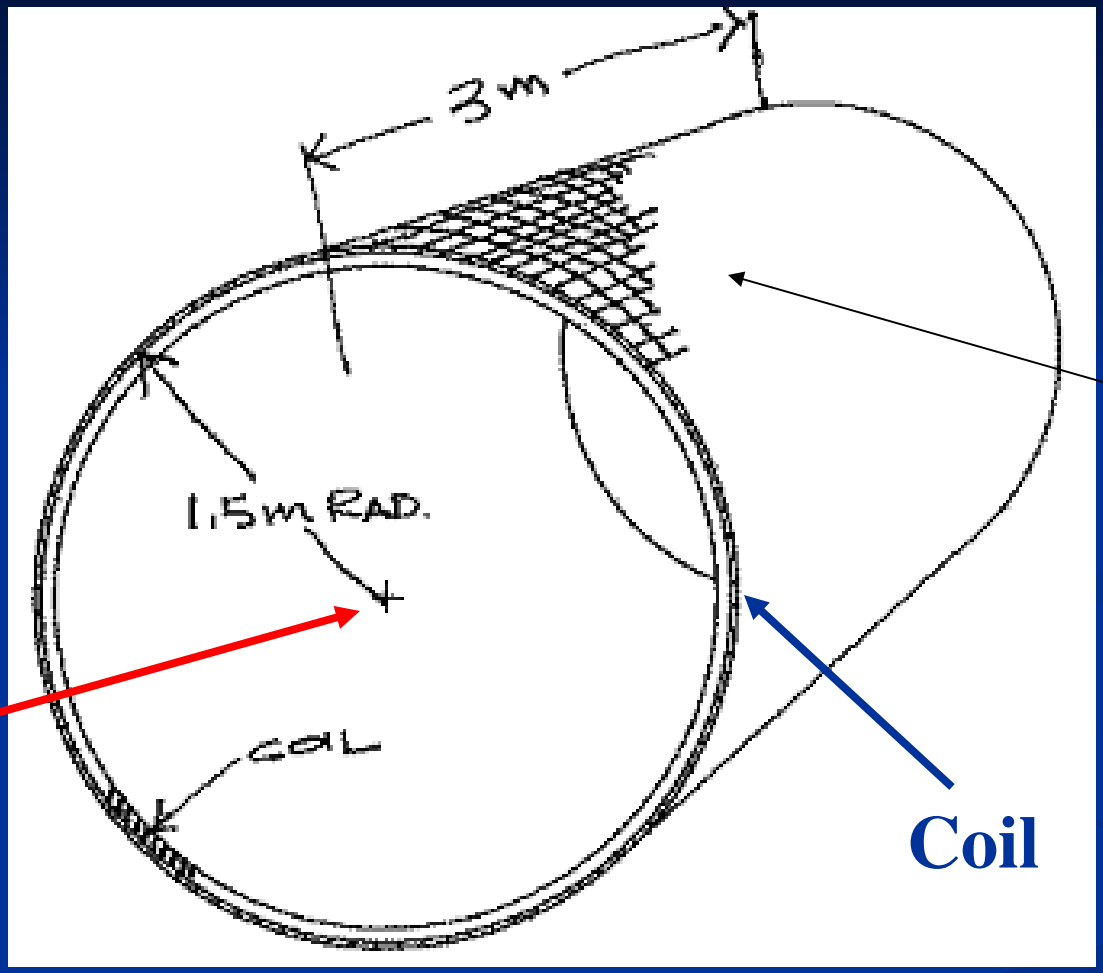
T-Tbar -> W^+bW^-bbar



Fit t_0 (start) from all tracks

Can we follow the color flow through kaons, cham, bottom? TOF!

Geometry for a Collider Detector



2" by 2" MCP's

Beam Axis

Coil

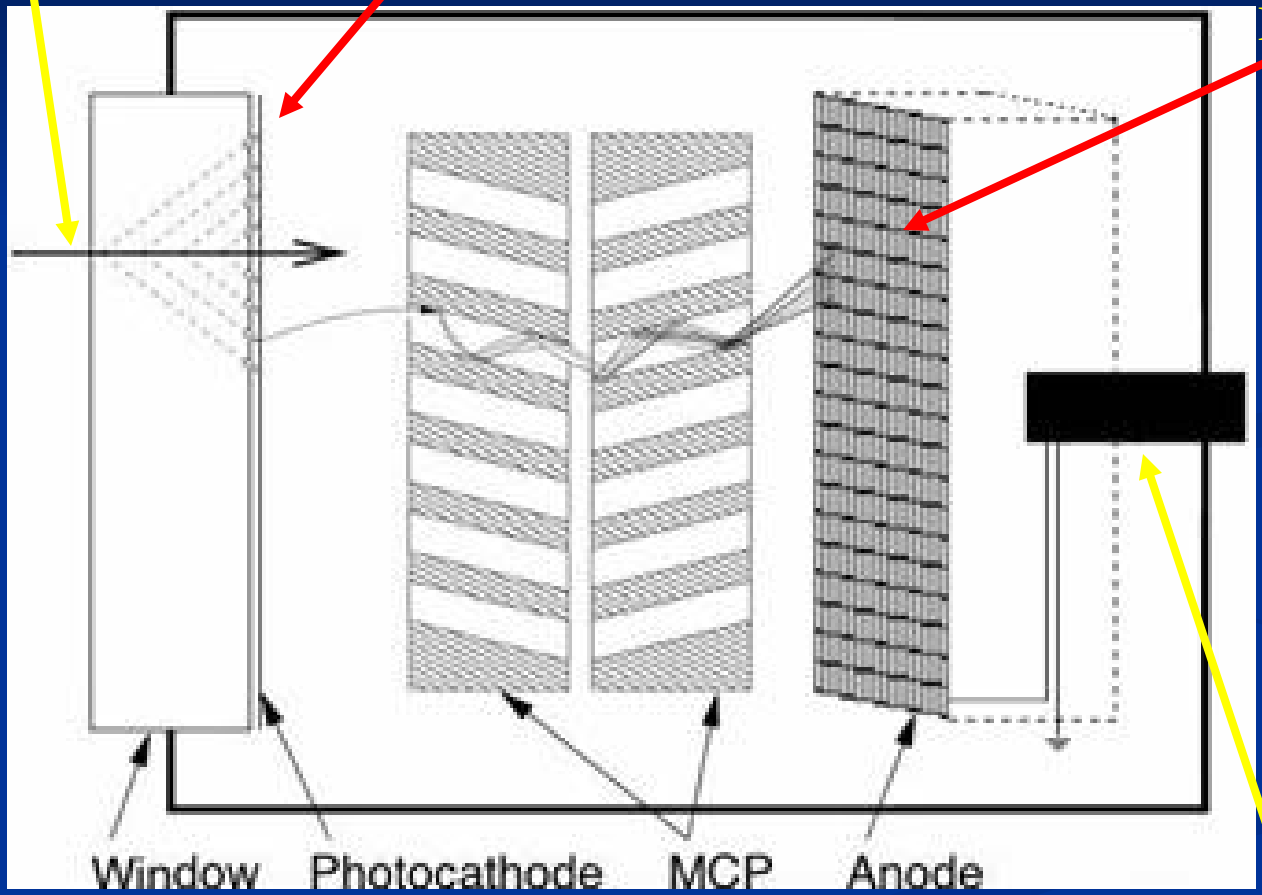
"r" is expensive- need a thin segmented detector

Idea 1: Generating the signal

Use Cherenkov light - fast

Incoming rel. particle

Custom Anode with Equal-Time Transmission Lines + Capacitative. Return

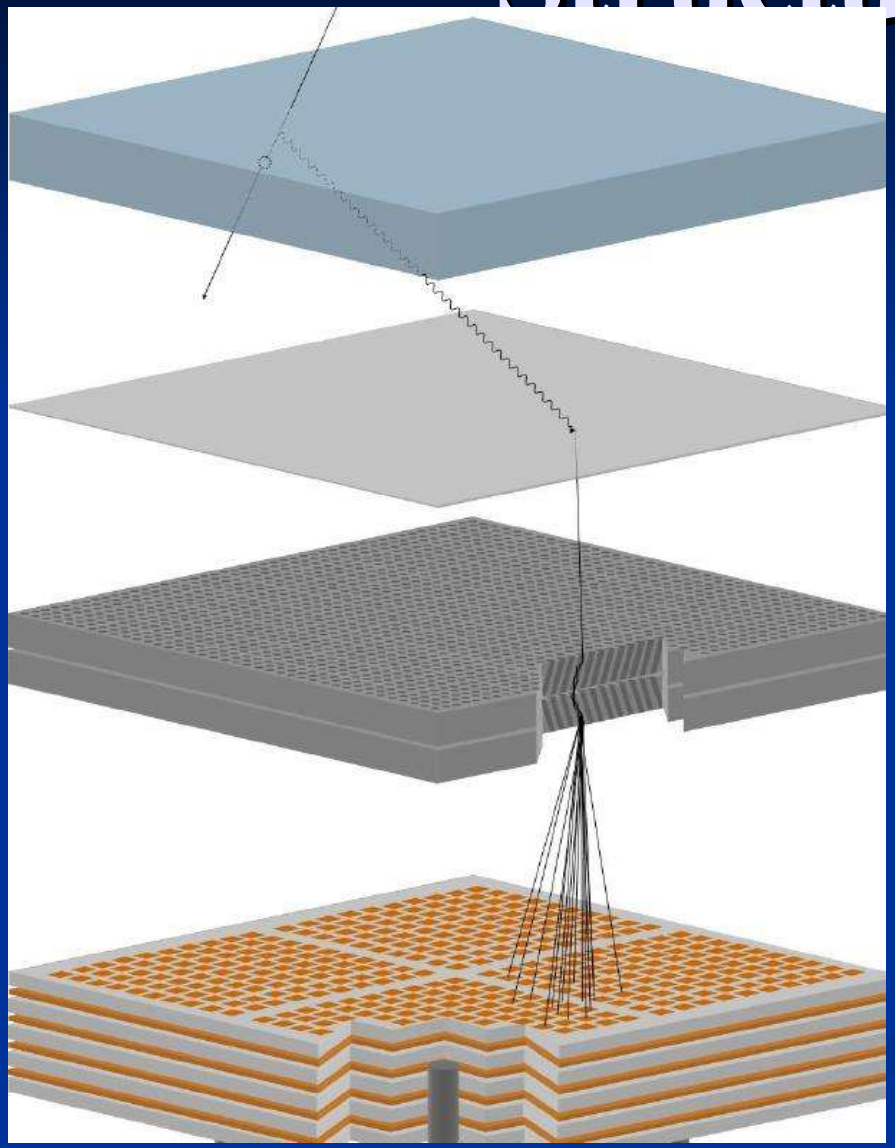


A 2" x 2" MCP-actual thickness ~3/4"

e.g. Burle (Photonis) 85022-with mods per our work

Collect charge here-differential Input to 200 GHz TDC chip

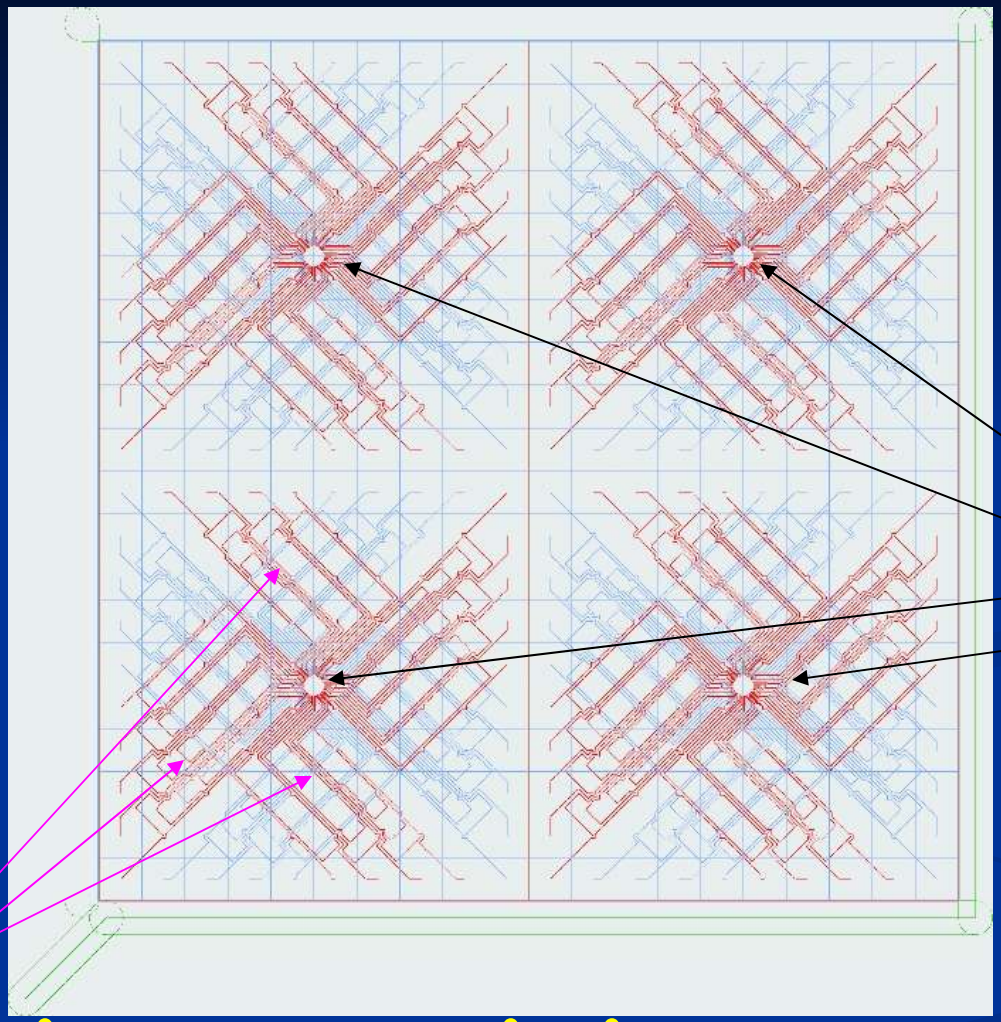
Idea 2: Equi-time Anode Structure



1. RF Transmission Lines
2. Summing smaller anode pads into 1” by 1” readout pixels
3. An equal time sum-make transmission lines equal propagation times
4. Work on leading edge- ringing not a problem for this fine segmentation

Equal-Time TL-Anode Bd

Designed by Tim Credo (IMSA)



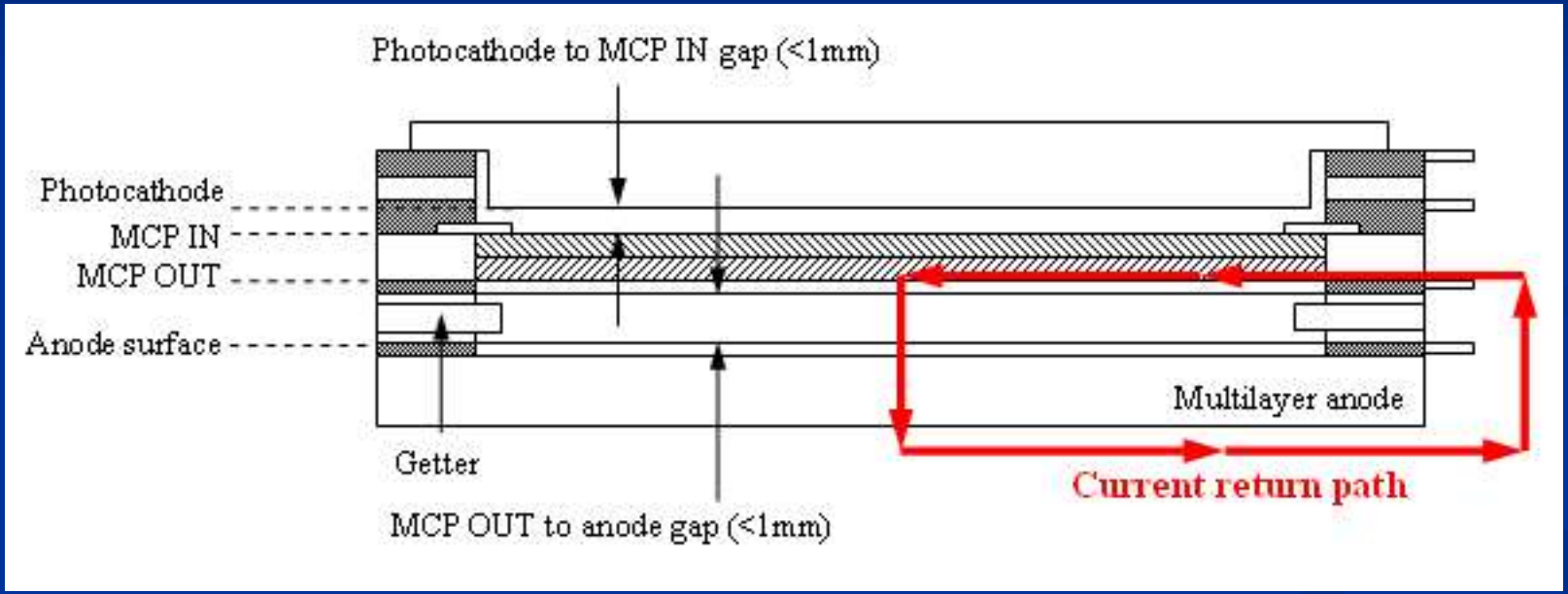
4 Outputs- each to a TDC chip (ASIC)

Chip to have < 1psec resolution(!)

-we are doing this in the EDG (Harold, Tang).

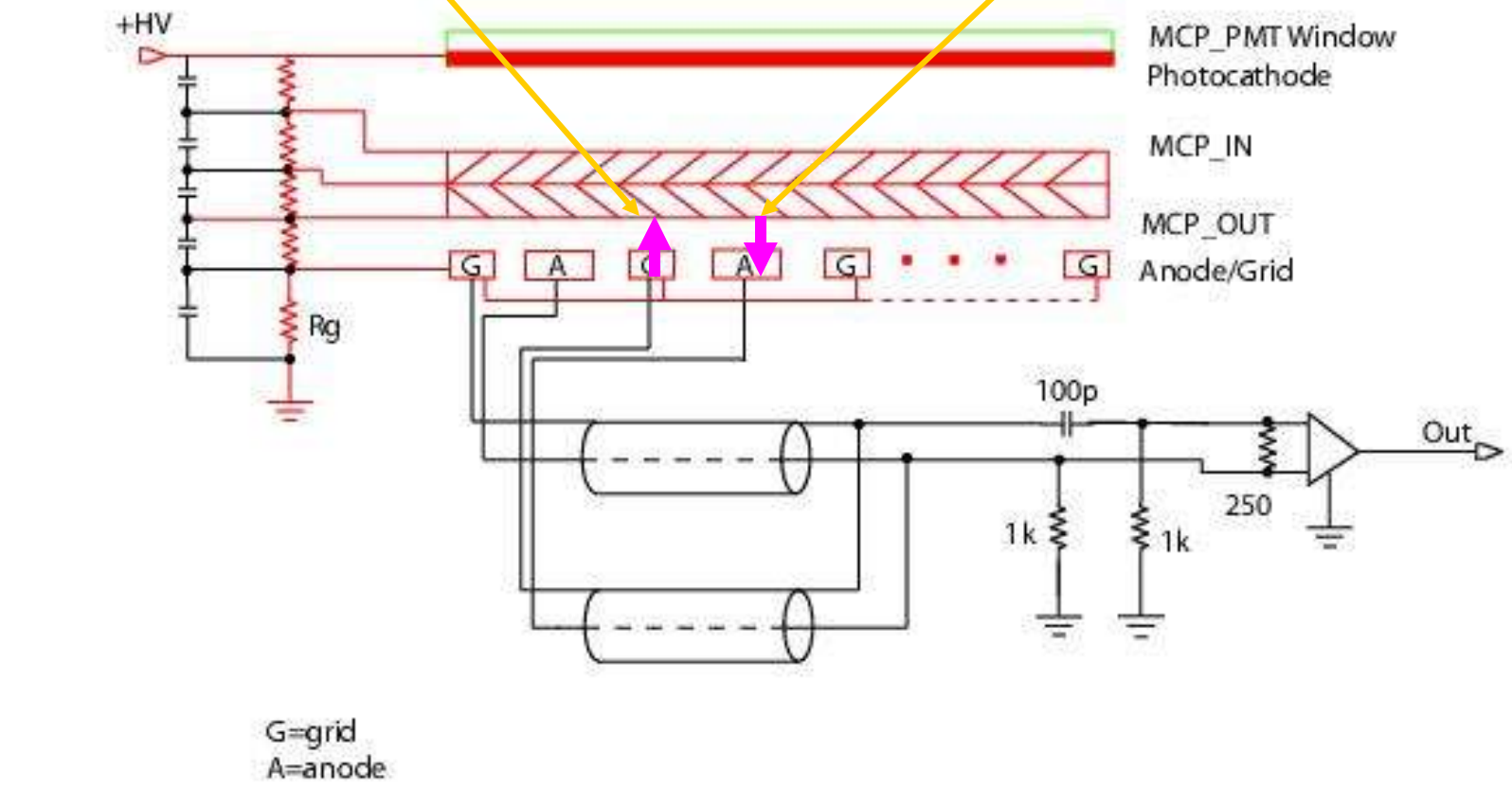
Equal-time transmission-line traces to output pin

Idea 3: Solution to the Anode Return Path Problem- Capacitive AC Return

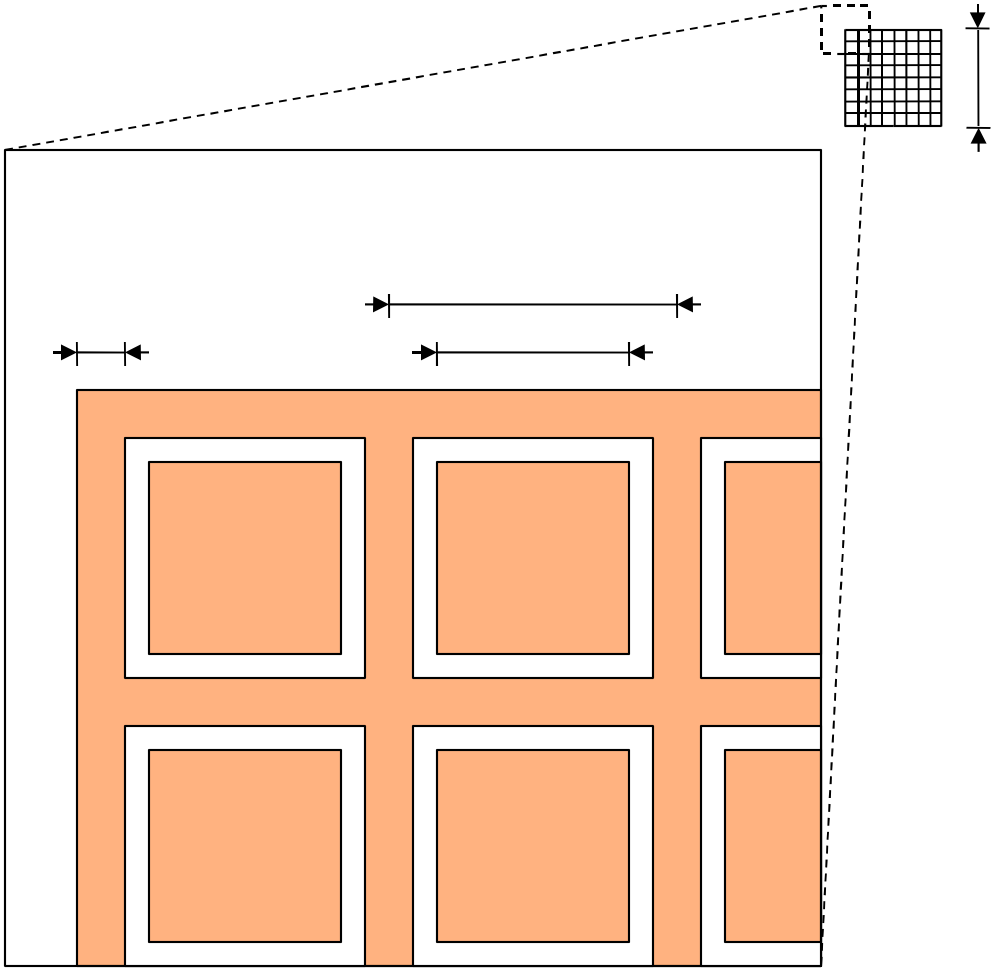


Problem is inductance, non-uniformity

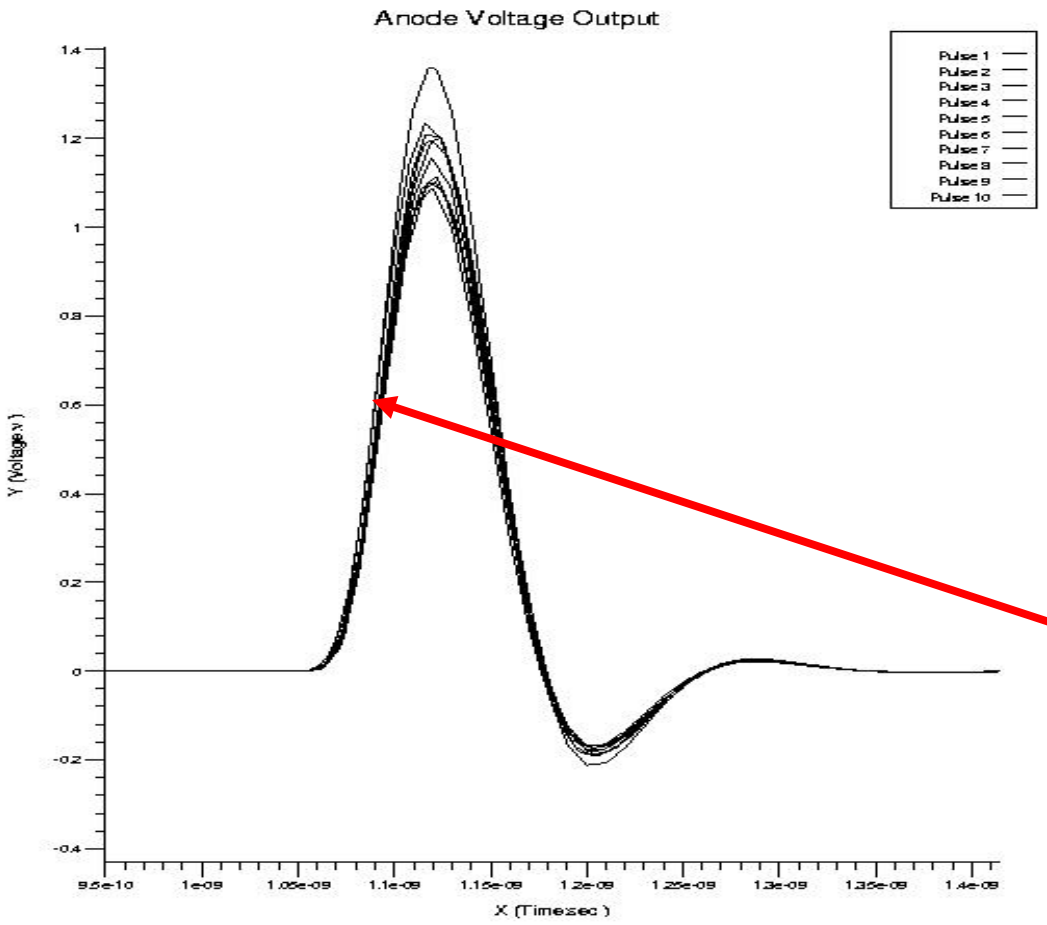
Capacitive Return Path Proposal



Solving the return-path problem



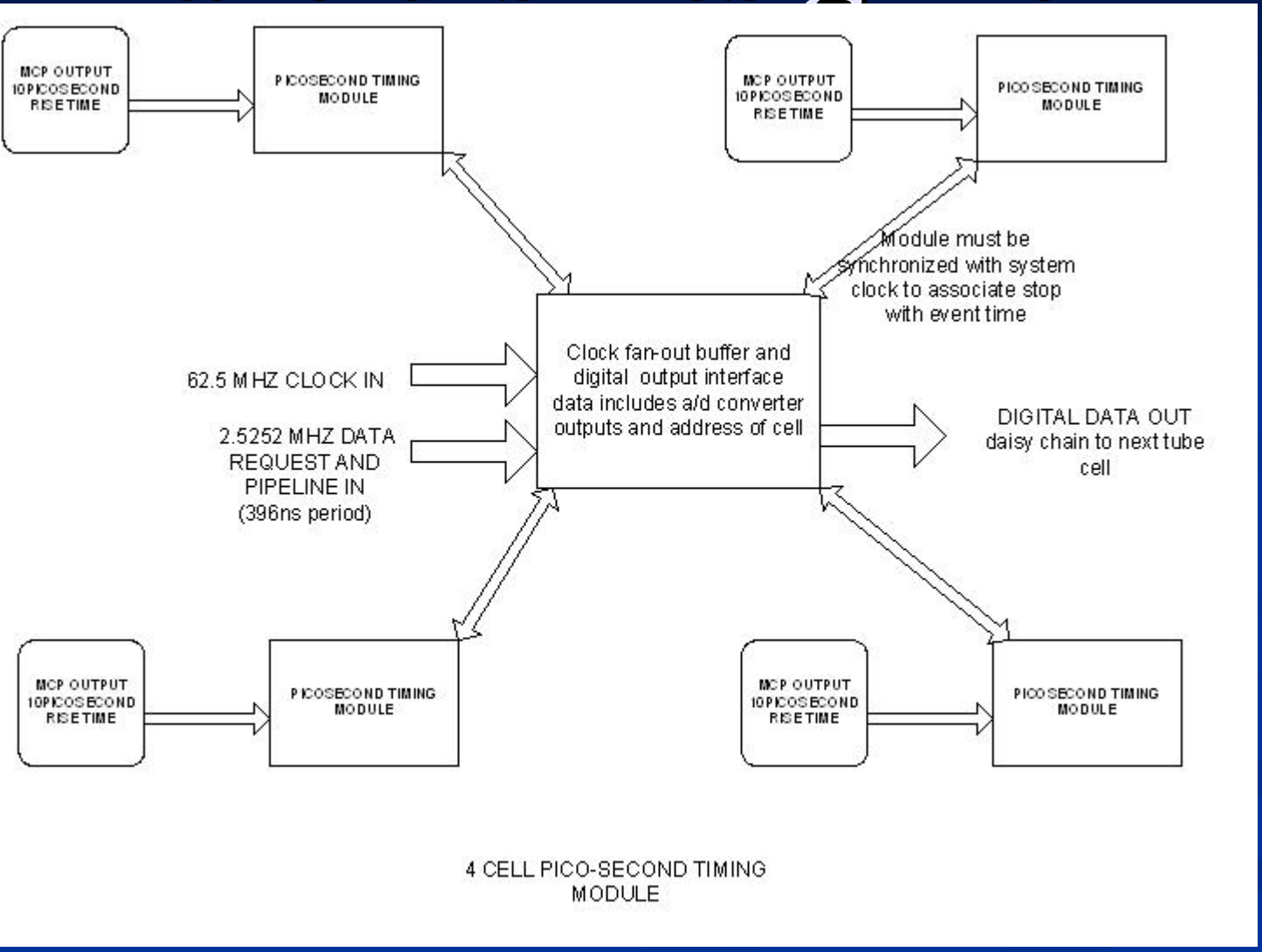
End-to-End Simulation Result



Output at anode from simulation of 10 particles going through fused quartz window- T. Credo, R. Schroll

Jitter on leading edge 0.86 psec

EDG's Unique Capabilities - Harold's Design for Readout



4 CELL PICO-SECOND TIMING MODULE

Each module has 5 chips- 4 TDC chips (one per quadrant) and a DAQ `mother' chip.

Problems are stability, calibration, rel. phase, noise.

Both chips are underway

Readout with sub-psec resolution:

Tang's Time Stretcher- 4 chips/2x2in module

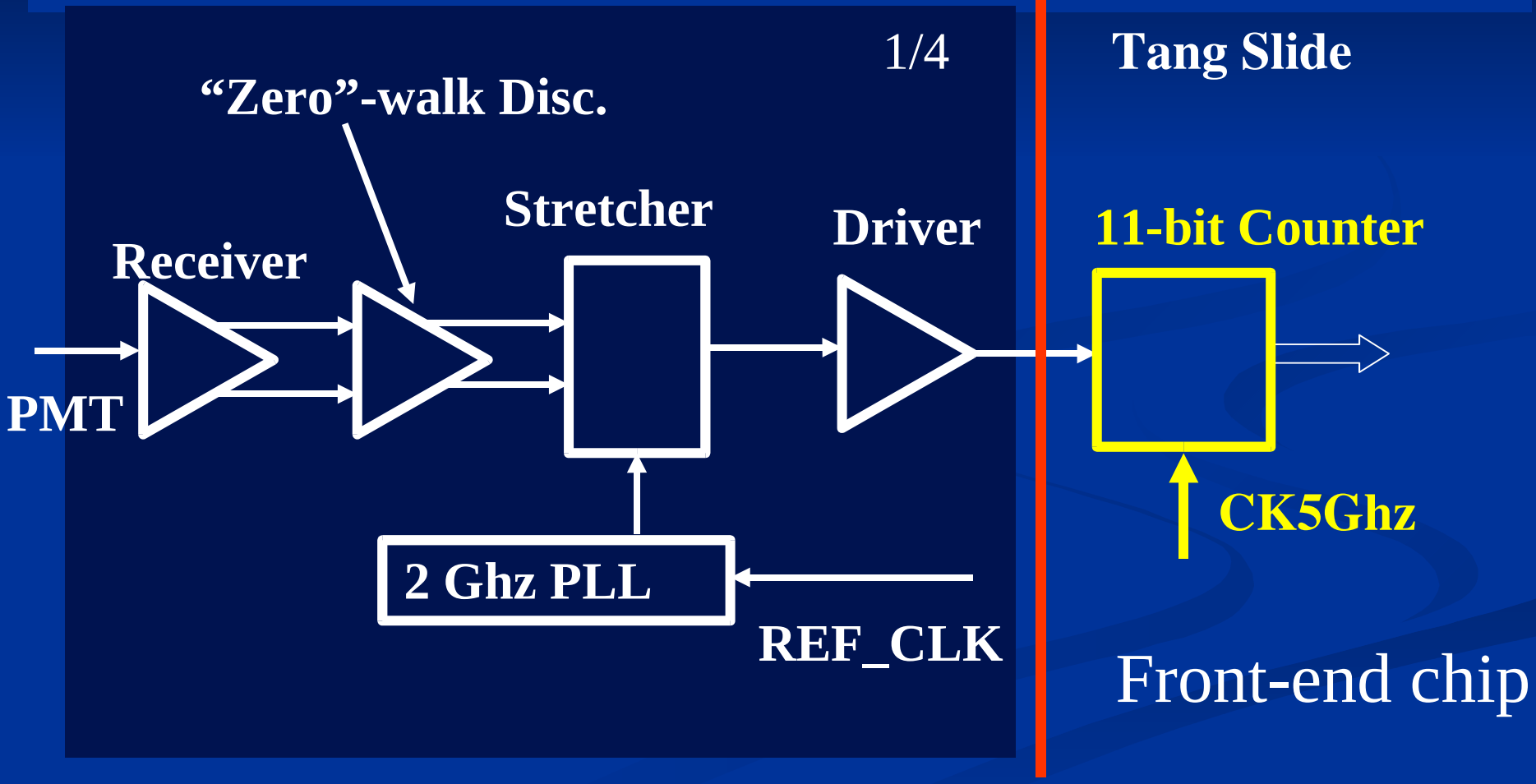
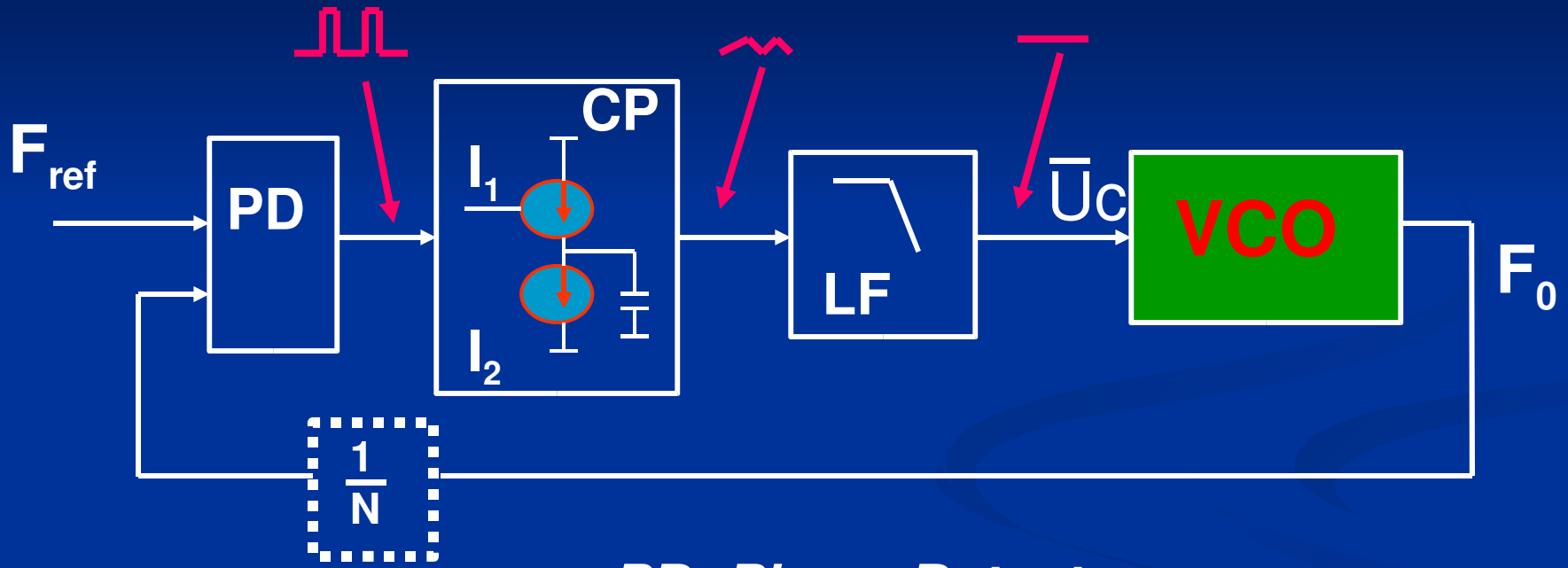


Diagram of Phase-Locked Loop

Tang Slide



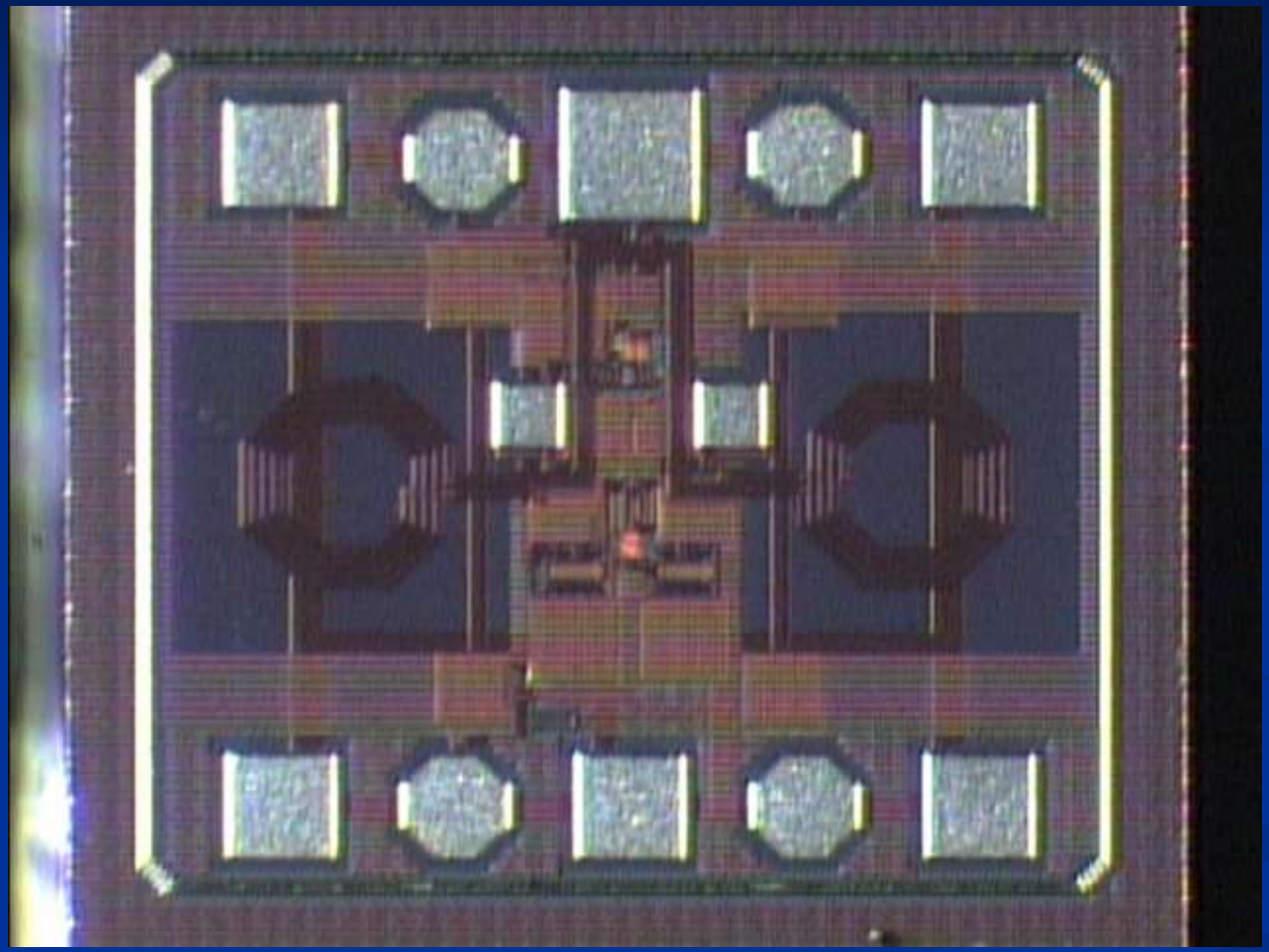
PD: Phase Detector

CP: Charge Pump

LF: Loop Filter

VCO: Voltage Controlled Oscillator

Microphotograph of IHP Chip



Taken at Fermilab by Hogan –

Design by Fukun Tang

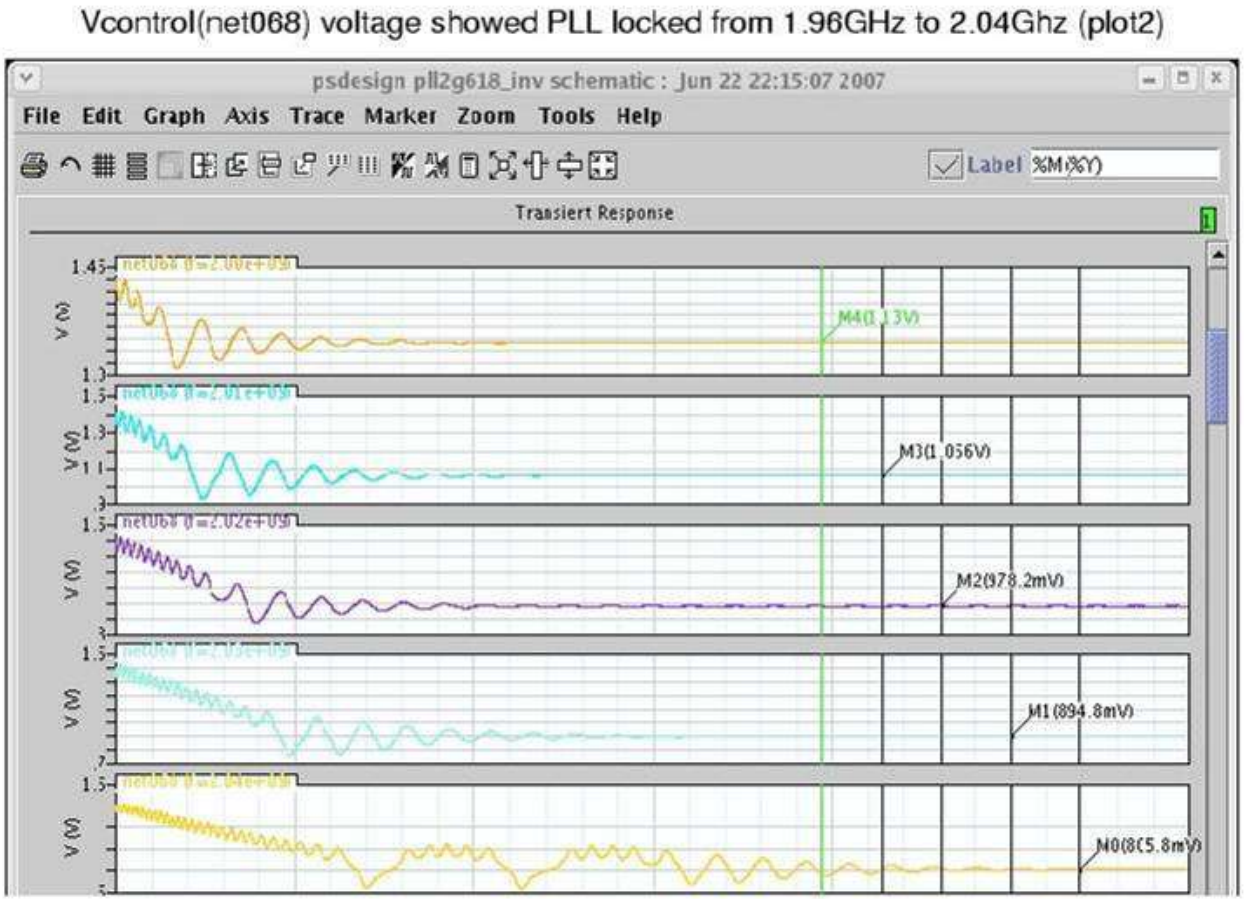
IBM SiGe BiCMOS8HP Process

- 130-nm technology
- SiGe hetero-junction bipolar transistors
  - *f_T (high performance): 200GHz, BVceo=1.7V, BVcbo=5.9V*
  - *f_T (high breakdown): 57GHz, BVceo=3.55V, BVcbo=12V*
- High-Q inductors and metal-insulator-metal capacitors
- 4 types of low-tolerance resistors with low and high sheet resistivity
  - *n+ diffusion, tantalum nitride, p+ polisilicon and p- polisilicon*
- Electrically writable e-fuse
- CMOS transistors (VDD=1.2V or 2.5/3.3V)
  - *Twin-well CMOS*
  - *Hyperabrupt junction and MOS varactors*
- Deep trench and shallow trench isolations
- 5 copper layers and 2 aluminum layers (3 thick layers)
- Wire-bond or controlled collapse chip connect (C4) solder-bump terminals

Recent progress: Stretcher Chip

Tang has designed and simulated the phase-locked loop, the heart of the sub-psec Stretcher chip.

Expect jitter < 100 fsec (!) from simulation (but have not, and do not know how to, simulate jitter on the input clock from the DAQ chip)



Recent Progress: DAQ Chip- 1/module

- Jakob Van Santen implemented the DAQ chip functionality in an Altera FPGA- tool-rich environment allowed simulation of the functionality and VHDL output before chip construction (Senior Thesis project in Physics)
- Gary Drake and John Anderson (Argonne) are trying to do this in a new Xilinx FPGA: if can do 20-30 psec in Xilinx get filtering/higher functions too! (big step for.)
- Again, simulation means one doesn't have to do trial-and-error. Great for PET and HEP.

Recent Accomplishments of ANL/UC

1. Designed, simulated, and constructed VCO block of stretcher chip in IHP process
2. Have designed, simulated full PLL (with VCO+phase detector +filter and feedback blocks) in IBM 8HP process-
3. Have visited IBM – good working relationship at high management and engineering levels (PH and TCC, e.g.- also Keith Jenkins visit)
4. Have placed an order with Burle/Photonis- have the 3st of 4 tubes and have a good working relationship (their good will and expertise is a major part of the effort): got new 10 micron tube, Burle working on capacitive-return design.
5. Harold and Tang have a good grasp of the overall system problems and scope, and have a top-level design plus details
6. Have modeled DAQ/System chip in Altera (Jakob Van Santen); ANL has started serious design in new Xilinx FPGA chip (John Anderson, Gary Drake).
7. ANL has built a test stand with working DAQ , very-fast laser, and has made contact with advanced accel folks:(+students)
8. Growing collaborative effort: have established strong working relationship with Chin-Tu Chen's PET group at UC (mention China); Ditto Va'vra at SLAC. Have MOU draft with Saclay; close working relationship with one of their top engineer (coming back for visits 2 and 3 this summer). Had very productive 2 day brain-storming with engrs inc. Bill Moses (LBL), on PET – led to new design for a CFD
9. Have found Greg Sellberg and Hogan at Fermilab to offer expert precision assembly advice and help. Submitting joint ANL/UC/Fermilab proposal to add fast timing to Fermilab test beam, help support engineering effort.

Project Milestones: p1

Version 1.0
April 17, 2007

DRAFT

Milestones for Pico-second Detector and Electronics Development

1 Year 1

1.1 Time Stretcher Chip

1. Design Phase-Locked Loop (PLL)
2. Design Constant-Fraction Discriminator (CFD)
3. Submit 1st Prototype to IBM 8HP via MOSIS

1.2 TDC/Clock/DAQ Chip

1. Define Interface to Time-Stretcher Chip
2. Define Interface to Clock, DAQ system
3. Initial Performance Specifications
4. Initiate Chip Design

1.3 PET TDC/Trigger Chip

1.4 Simulation Development

1. Survey existing software
2. Define modules and tasks
3. Initial Performance Specifications
4. Define Interfaces
5. Initiate MCP Module Code
6. Initiate PET signal generation code

1.5 Instrumentation and Laser Test Stand

1. Commission DAQ system
2. Establish test-stand baseline at 40 psec resolution with 25-micron pore tube and old electronics
3. Establish log-book and documentation framework
4. Acquire access to precision time reference, ultra-fast oscilloscope, and jitterometer.
5. Achieve 10 psec resolution with 10-micron tube and old electronics.

1

Project Milestones: p2

1.6 MCP Development

1. Receive and assemble 10-micron MCP with anode assembly
2. Measure time-resolution of 10-micron MCP with equal-time anode
3. Measure gain, time resolution vs position of 10-micron MCP
4. Specify 2nd-tube from Photon/Burle with small MCP-OUT/Anode gap

1.7 System Issues

1. Conceptual report on calibration
2. Conceptual report on clock distribution
3. Conceptual report on stability

1.8 Applications

1. FP420 (to be filled out)

2 Year 2

2.1 Time Stretcher Chip (TSC)

1. Test 1st Prototype on bench- measure stability, dynamic range, speed
2. If acceptable, connect TSC's on output pins of MCP anode plane
3. Understand, react, and, if necessary, modify design of TSC; full simulation
4. Submit 2nd Prototype to IBM 8HP via MOSIS

2.2 TDC/Clock/DAQ Chip (TCDC)

1. Finish Chip Design, full simulation
2. Submit first TCDC chip to foundry

2.3 PET TDC/Trigger Chip

1. Final Performance Specifications
2. Further develop MCP Module Code comparing to test results
3. Further develop PET signal generation code comparing to test results

2.4 Simulation Development

1. Further develop MCP Module Code
2. Validate MCP Module Code
3. Further develop PET signal generation code
4. Validate PET signal generation code

Project Milestones: p3

2.5 Instrumentation and Laser Test Stand

1. Construct precision stage and beam-splitter for 2-MCP tests
2. Refine precision time reference, jitter measurements and equipment, down to few psec level.
3. Achieve 4 psec resolution with 10-micron tube and new electronics.

2.6 MCP Development

1. Receive and commission tube from Photon/Burle with small MCP-OUT/Anode gap
2. Measure time-resolution of 2nd 10-micron MCP with equal-time anode
3. Measure gain, time resolution vs position of 2nd 10-micron MCP
4. Specify new tube from Photon/Burle with small MCP-OUT/Anode gap, plating up into exits of pores, and possibly with enhanced first-strike secondary emission.

2.7 System Issues

1. Initial design of calibration system.
2. Small scale implementation of calibration system.
3. Initial design of clock distribution

2.8 System/Beam Tests

1. Implementation of DAQ, reference clock, etc. systems
2. First single station beam test
3. Multiple station beam test

2.9 Applications

1. FP420 (to be filled out)

3 Year 3

3.1 Time Stretcher Chip

1. Submit Final Design to IBM 8HP via MOSIS
2. Characterize, Commission, and Test Final Chips

3.2 TDC/Clock/DAQ Chip

1. Submit Design for fabrication
2. Bench Test, Commission and In-Situ-Test of Final Chips

Project Milestones: p4

3.3 PET TDC/Trigger Chip

1. Fabricate and test 2nd-generation chip
2. Write and commission a first-generation DAQ software
3. Construct and characterize a micro-pet system with this readout.

3.4 Simulation Development

1. Continue development, refinement, and validation
2. Use simulation to spec an 'Nth-generation' simulation-optimized MCP
3. Use simulation to spec an 'Nth-generation' simulation-optimized micro-pet device.

3.5 Instrumentation and Laser Test Stand

1. Achieve 1 psec resolution with optimized 10-micron tube and custom Stretcher/DAQ chip electronics.

3.6 MCP Development

1. Receive and assemble 10-micron MCP with optimized internal anode assembly
2. Measure time-resolution of optimized tube
3. Measure gain, time resolution vs position
4. Specify Nth-generation tube from Photon/Burle

3.7 System Issues

1. 2nd generation Clock and Calibration system design

3.8 System/Beam Tests

1. Test a 4-station multiple-unit system with 1 psec resolution

3.9 Applications

1. FP420 (to be filled out)
2. Start construction of a 100-unit 4-station system appropriate for muon cooling (1 psec resolution)

What are we requesting?

Take Year 1 (very typical):

M&S: Chip submissions, MCP Prototypes, PC cards,… : 175K$

Equipment (Instrumentation): 40K$

Personnel: 1/3 EDG head +1 engineer 190K$
grad student+ undergrads 48K$
visitors (from Saclay, LBL, SLAC) 24K$

Travel: Domestic 10K$, Foreign 16K$

Top Priority is the EDG engineering- this is our critical path, and also corresponds to our unique collection of expertise and tools- unmatched, I (arguably) would argue…

That's All…

Backup Slides

Questions on Simulation-Tasks (for discussion)

1. Framework- what is the modern CS approach?
2. Listing the modules- is there an architype set of modules?
3. Do we have any of these modules at present?
4. Can we specify the interfaces between modules- info and formats?
5. Do we have any of these interfaces at present?
6. Does it make sense to do Medical Imaging and HEP in one framework?
7. Are there existing simulations for MCP's?

Accelerator Applications

- Momentum (velocity times known mass) Analysis in a beam (e.g. test beam). 4 single-module stations (this is our proof of principle- first step after laser)

- 6D Muon Cooling (muons.inc, hopefully) measurements- two 25-module stations replace a magnetic spectrometer (need pos. tho still 2 places)

- CERN Accelerator folks very interested (per Patrick LeDu, Saclay)

Other fields: nuclear physics, astrophysics,…..

Why is simulation essential?

Want optimized MCP/Photodetector design- complex problem in electrostatics, fast circuits, surface physics, ….

Want maximum performance without trial-and-error optimization (time, cost, performance)

At these speeds (~1 psec) cannot probe electronics (for many reasons!)

Debugging is impossible any other way.

Simulation for Coil Showering and various PMTs

Right now, we have a simulation using GEANT4, ROOT, connected by a python script

GEANT4: pi^+ enters solenoid, e- showers

ROOT: MCP simulation - get position, time of arrival of charge at anode pads

Both parts are approximations

Could we make this less home-brew and more modular?

Could we use GATE (Geant4 Application for Tomographic Emission) to simplify present and future modifications?

Working with Chin-tu Chen, Chien-Minh Kao and group, - they know GATE very well!

Interface to Other Simulation Tools

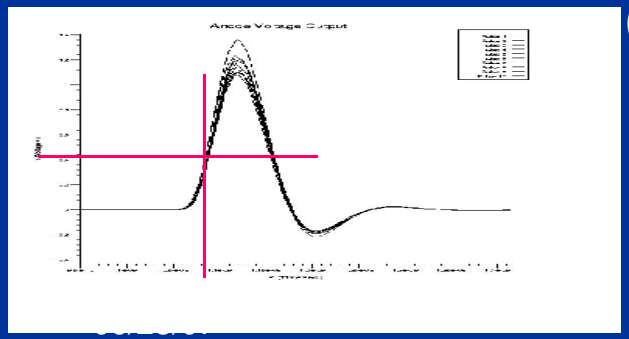
Tang slide

ASCII files:
Waveform time-value pair

ASCII files:
Waveform time-value pair

Tube Output Signals from Simulation

Tube Output Signals from Scope



Cadence Virtuoso Analog Environment

Or

Cadence Virtuoso AMS Environment

System Simulation Results

Spectre Netlist (Cadence Spice)

Spectre Library

Spectre Netlist

Custom Chip Schematic

IBM 8HP PDK

Cadence Simulator

The Future of Psec Timing- Big Questions:

From the work of the Nagoya Group, Jerry Va'vra, and ourselves it looks that the psec goal is not impossible. It's a new field, and we have made first forays, and understand some fundamentals (e.g. need no bounces and short distances), but it's entirely possible, even likely, that there are still much better ideas out there.

Questions:

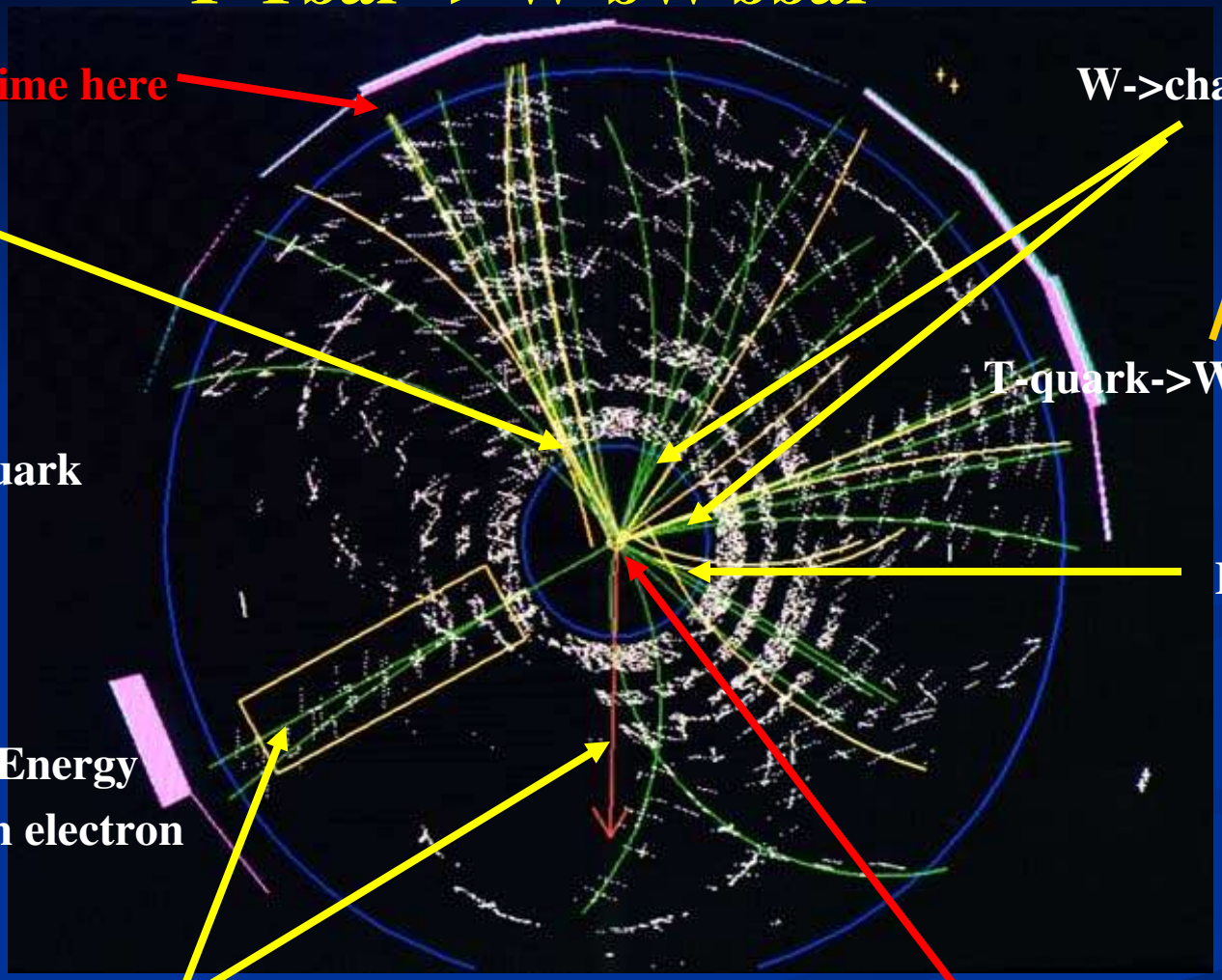
- **Are there other techniques? (e.g. all Silicon)?**

Smaller Questions for Which I'd Love to Know the Answers

- What is the time structure of signals from crystals in PET? (amplitude vs time at psec level)
- Could one integrate the electronics into the MCP structure- 3D silicon (Paul Horn)?
- Will the capacitative return work?
- How to calibrate the darn thing (a big system)?
- How to distribute the clock
- Can we join forces with others and go faster?

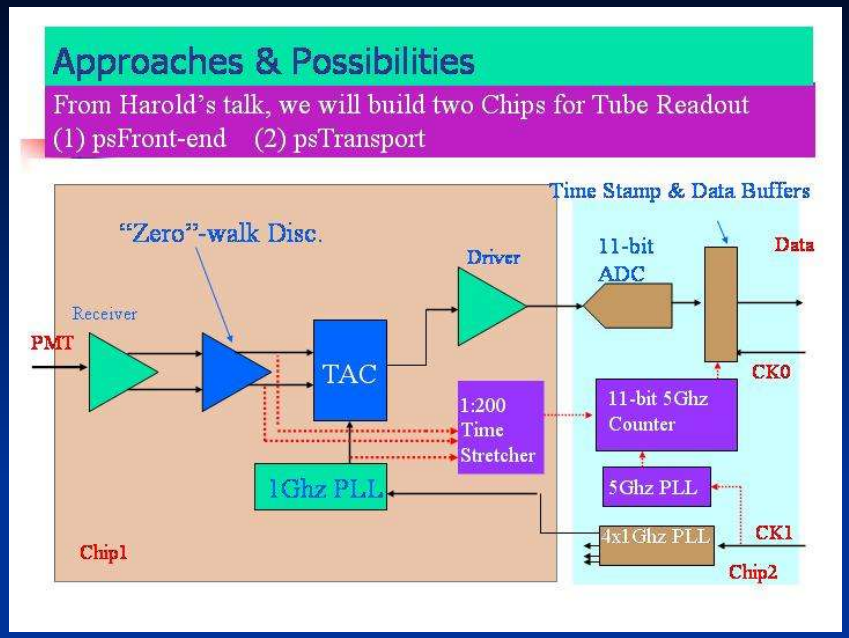
The Future- Triggering?

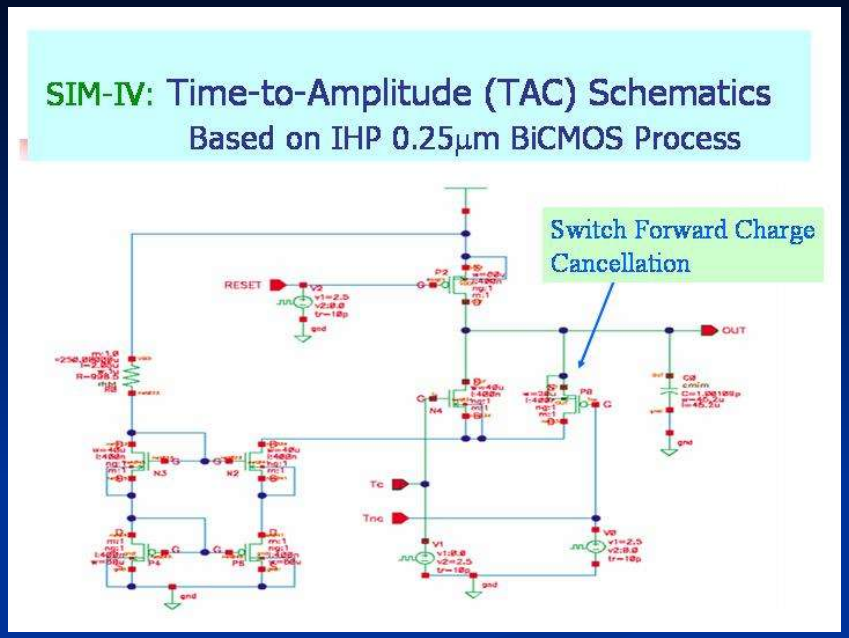
T-Tbar -> W^+bW^-bbar

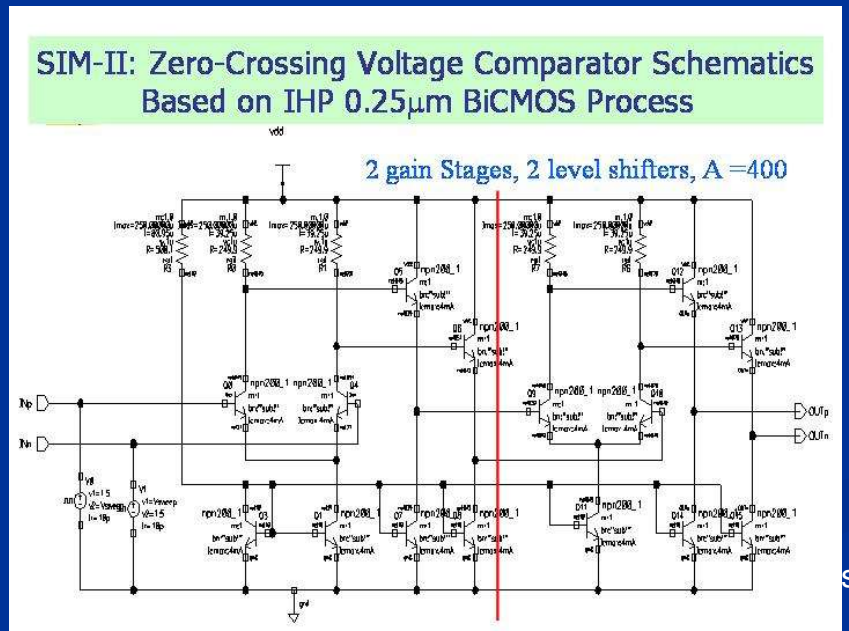


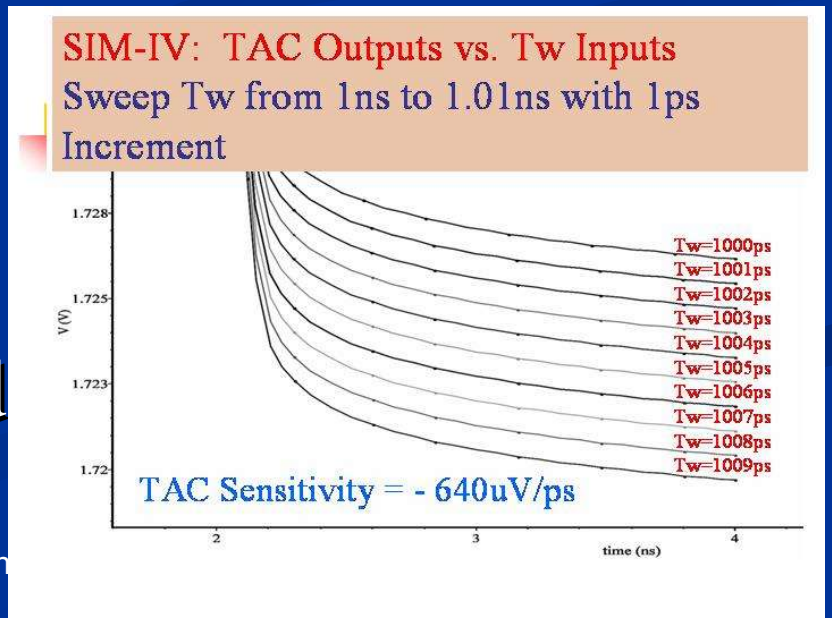
Can we follow the color flow of the partons themselves?

Simulation of Circuits (Tang)









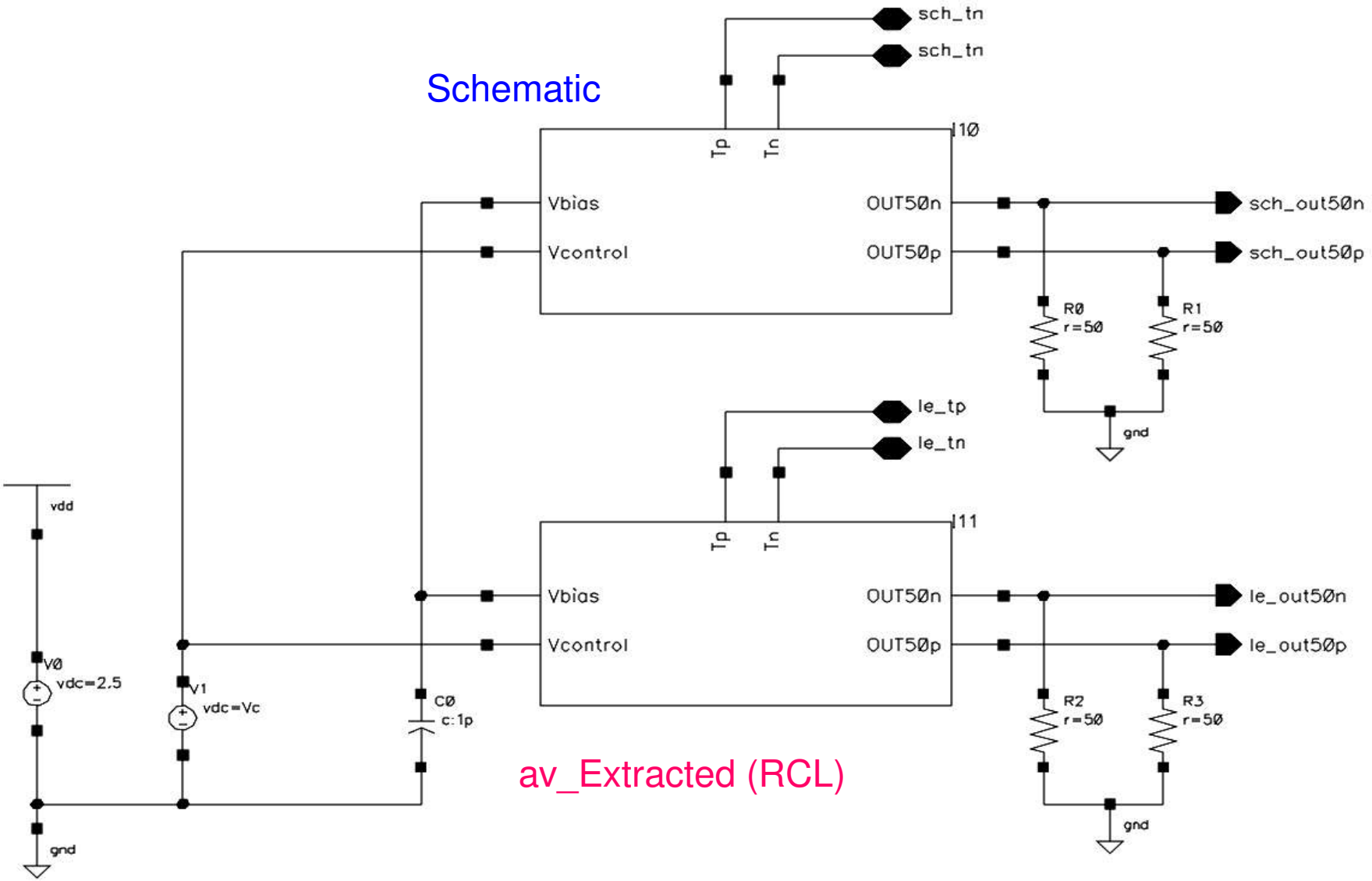
d

sit, Arlin

Mounting electronics on back of MCP- matching

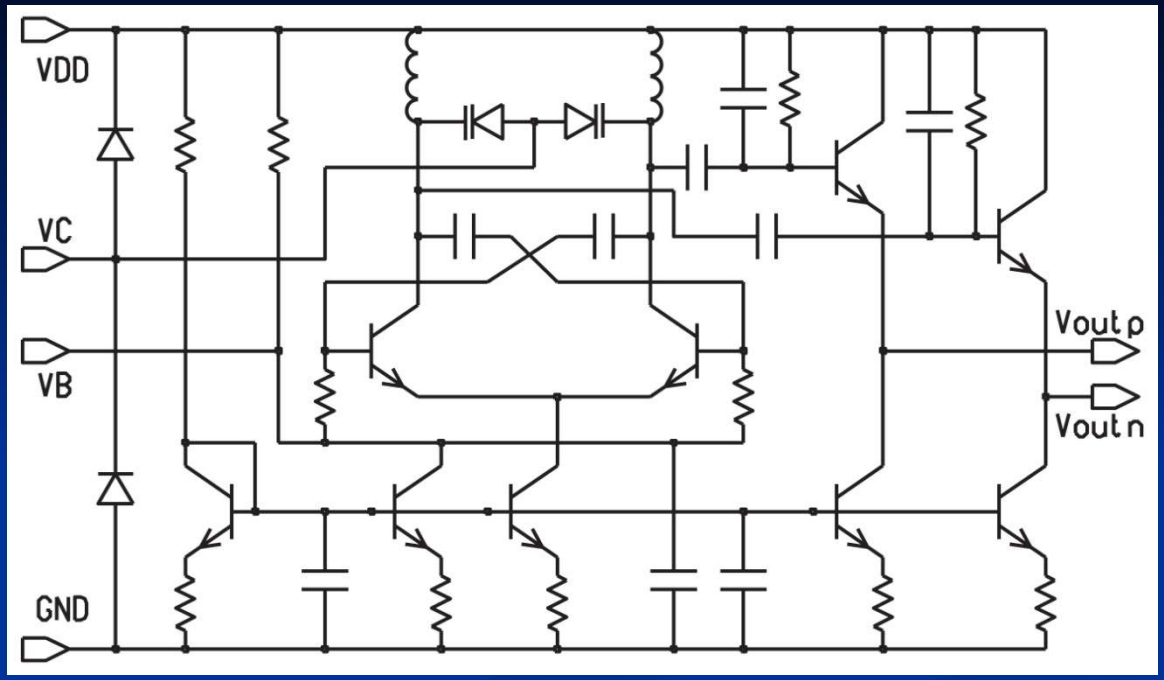
Conducting Epoxy-machine deposited by Greg Sellberg (Fermilab)

VCO Schematic & Post Layout Simulation Setup



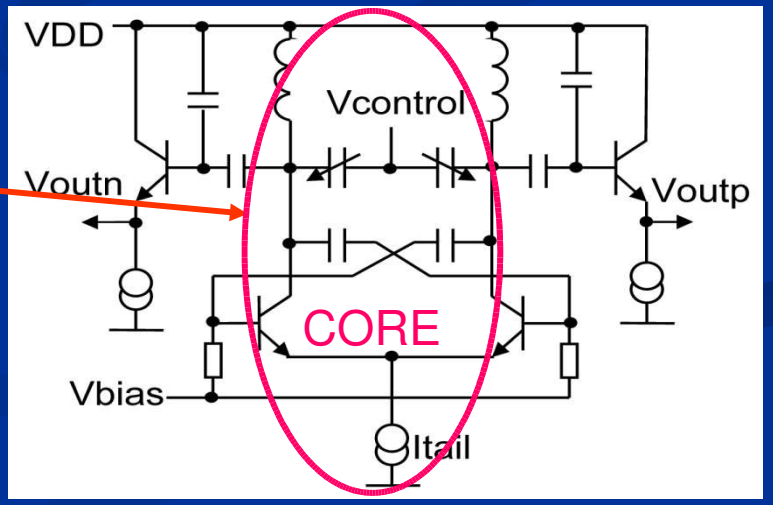
2GHz VCO Design

Simplified VCO Schematic

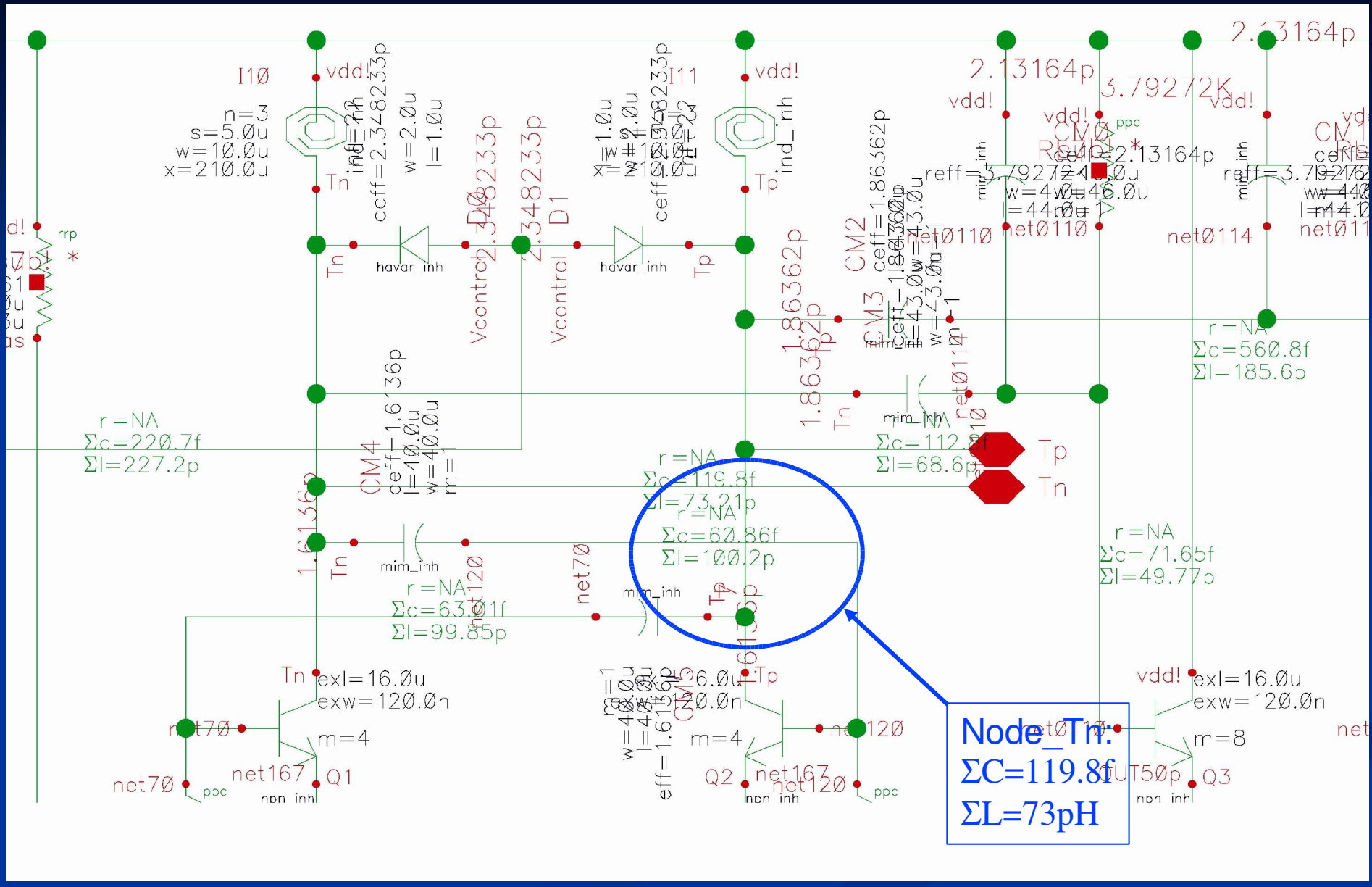


- Purely hetero-junction transistors
- Negative resistance
- 130Mhz tuning range
- On-chip high-Q LC tank
- High Frequency PN diode Varactors
- Capacitor voltage dividers
- Full differential 50-ohm line drivers
- Deep trench isolation

Core

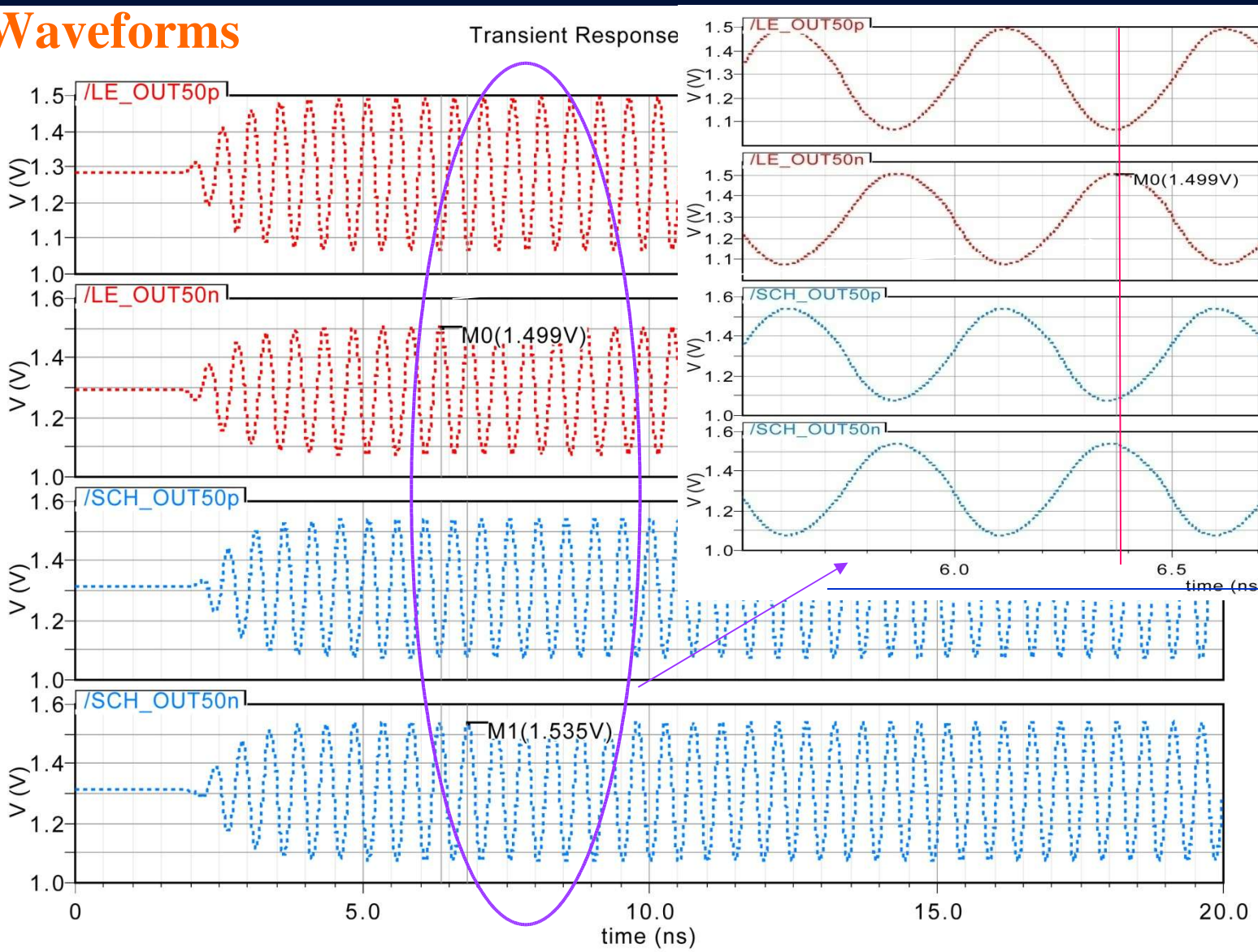


Av_Extracted Back Annotation View

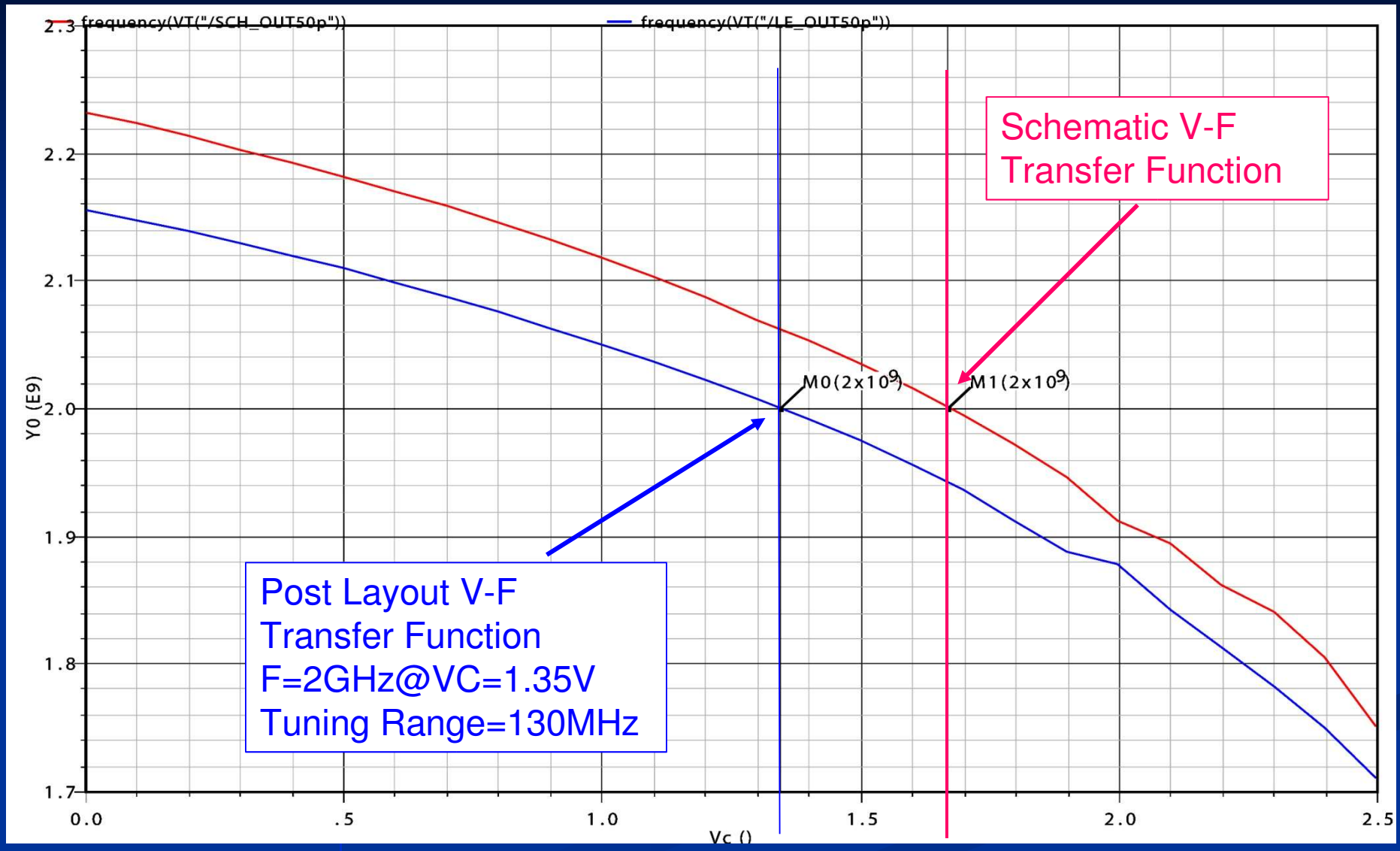


VCO Post Layout Transit Simulation

Transit Output Waveforms

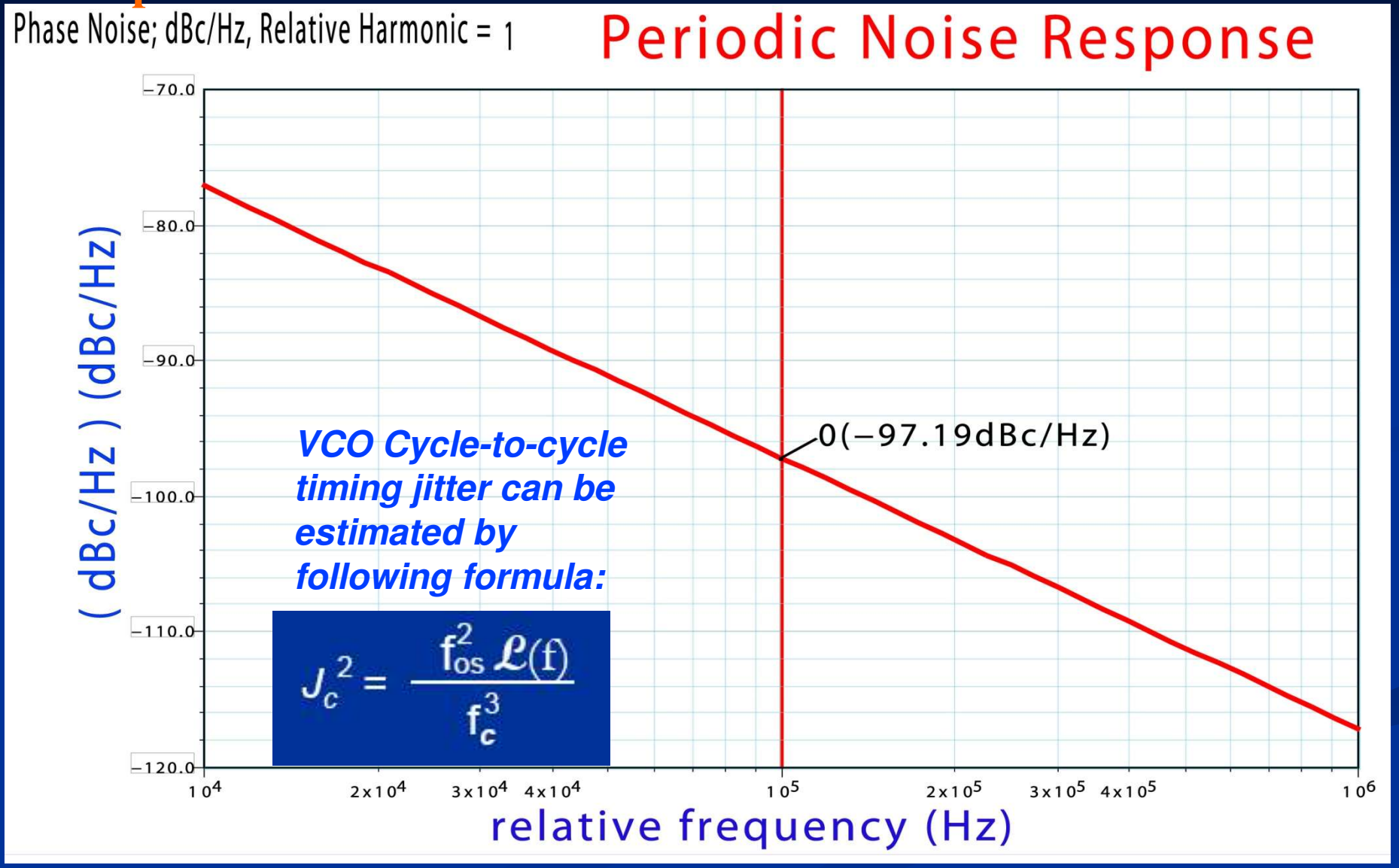


VCO Schematic and Post-layout V-F Transfer Function Plots_

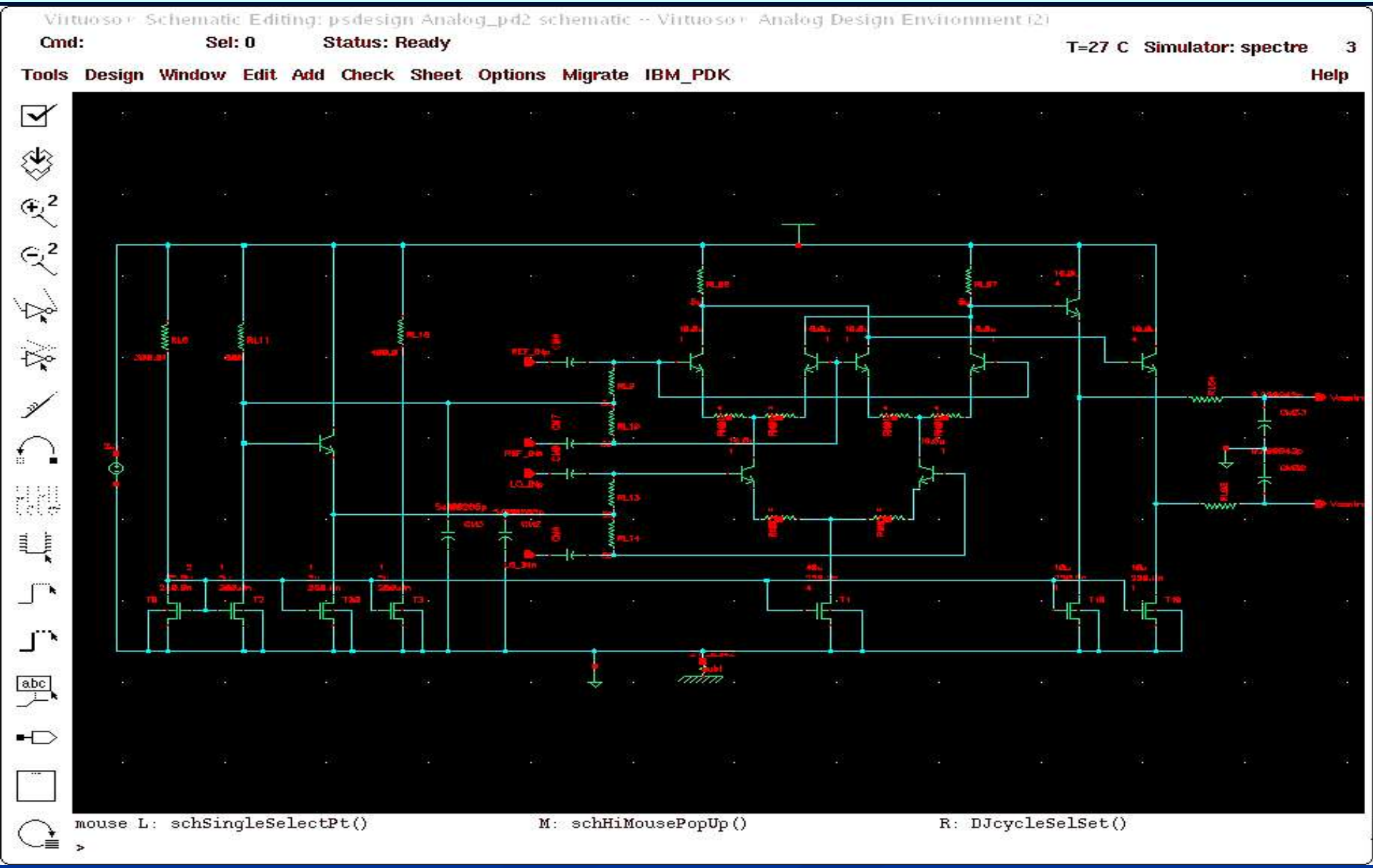


VCO Post Layout Phase Noise Simulation

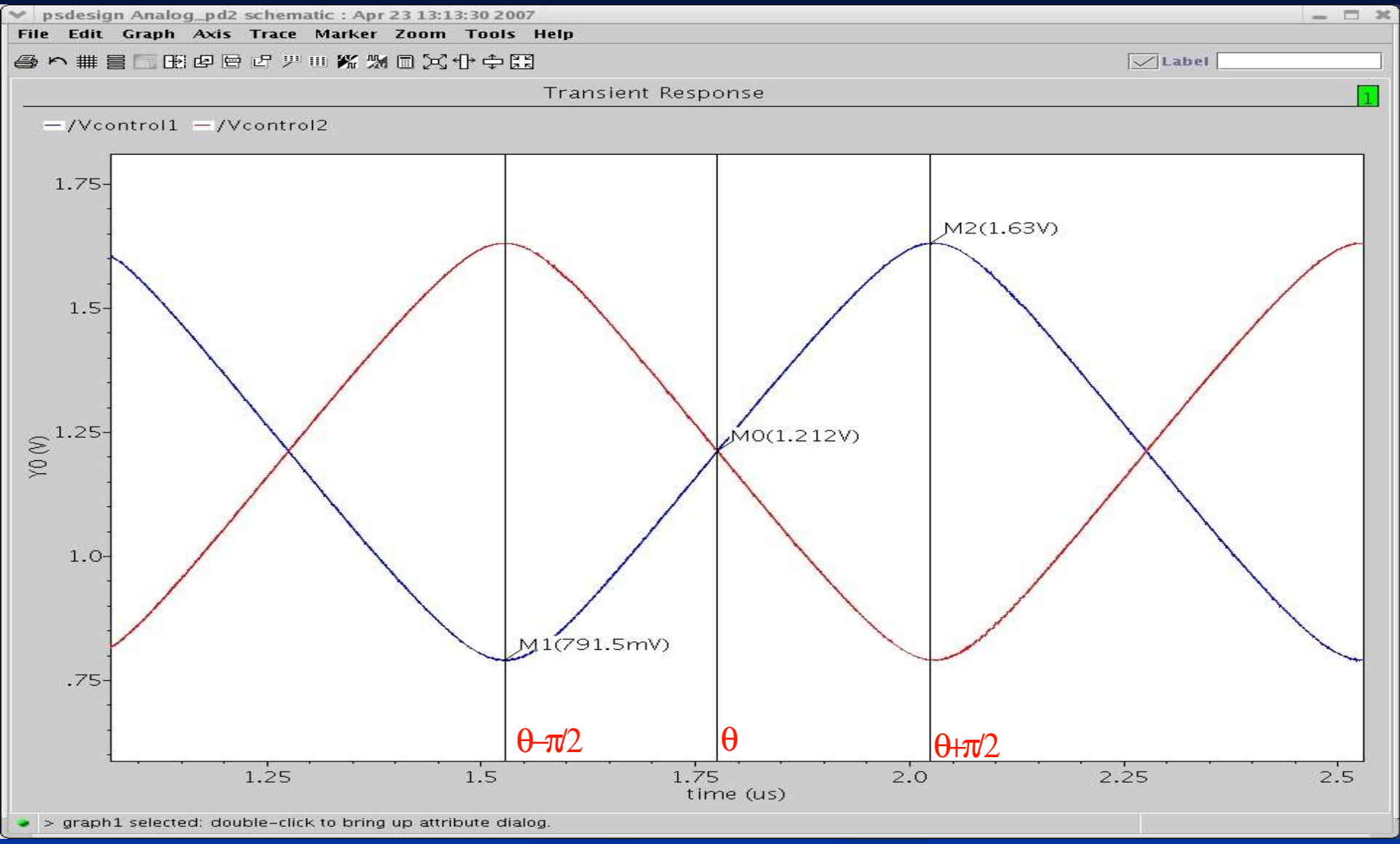
Output Phase Noise



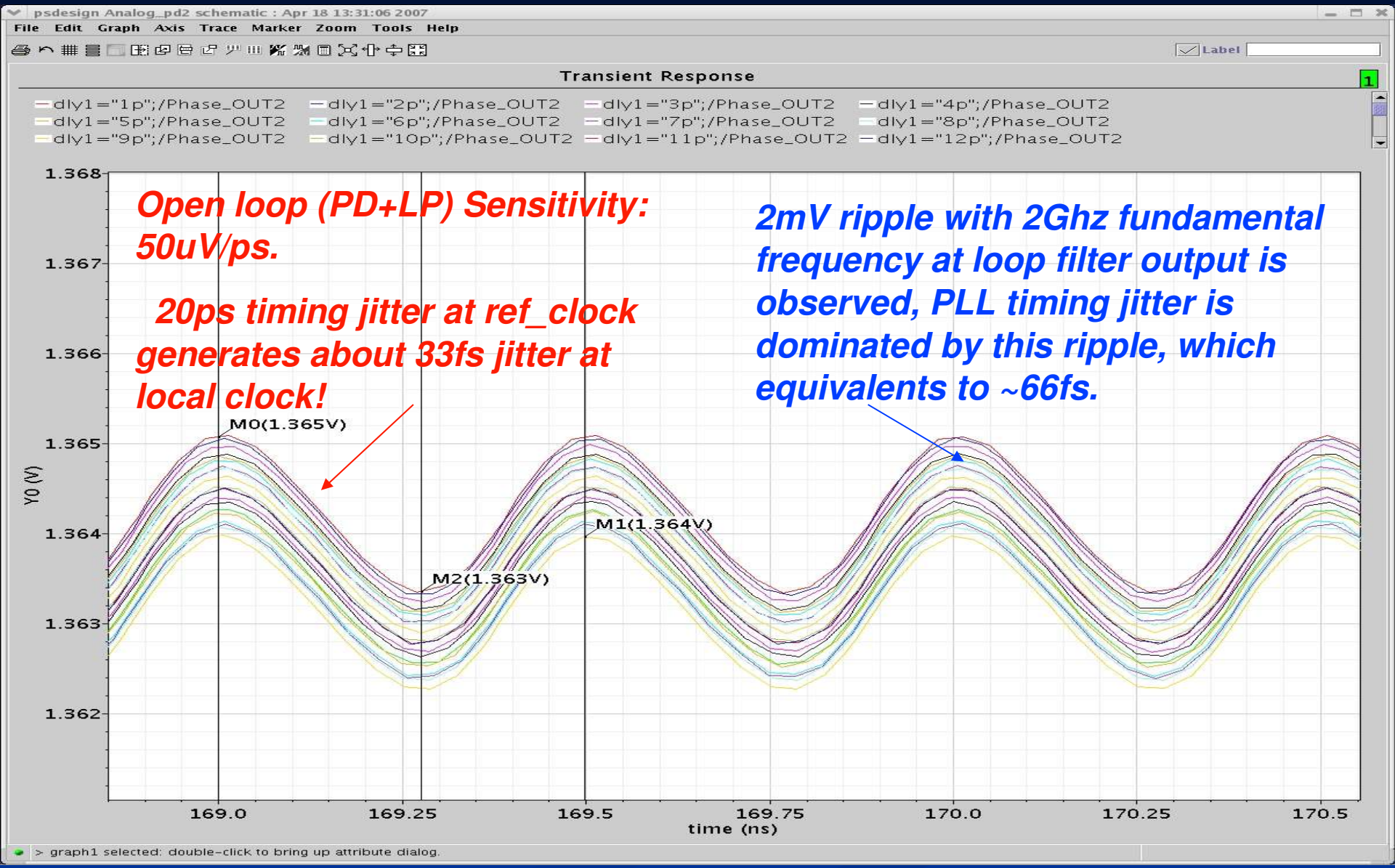
Phase Detector and Loop Filter Design



Characteristics of Four-quadrant Multiplier Phase Detector Differential Outputs with over-driven Inputs



A example showing Phase Detector & Loop Filter Open Loop Responses to the Ref_clock phase variation (1-20ps)



Shreyas Bhat slide

Input Source code, Macros Files
- Geometry
- Materials
- Particle:
  - Type
  - Energy
  - Initial Positions, Momentum
- Physics processes
- Verbose level

π + Generation, Coil Showering GEANT4

Have position, time, momentum, kinetic energy of each particle for each step (including upon entrance to PMT)

- Need to redo geometry (local approx.➔ cylinder)
- Need to redo field
- Need to connect two modules (python script in place for older simulation)

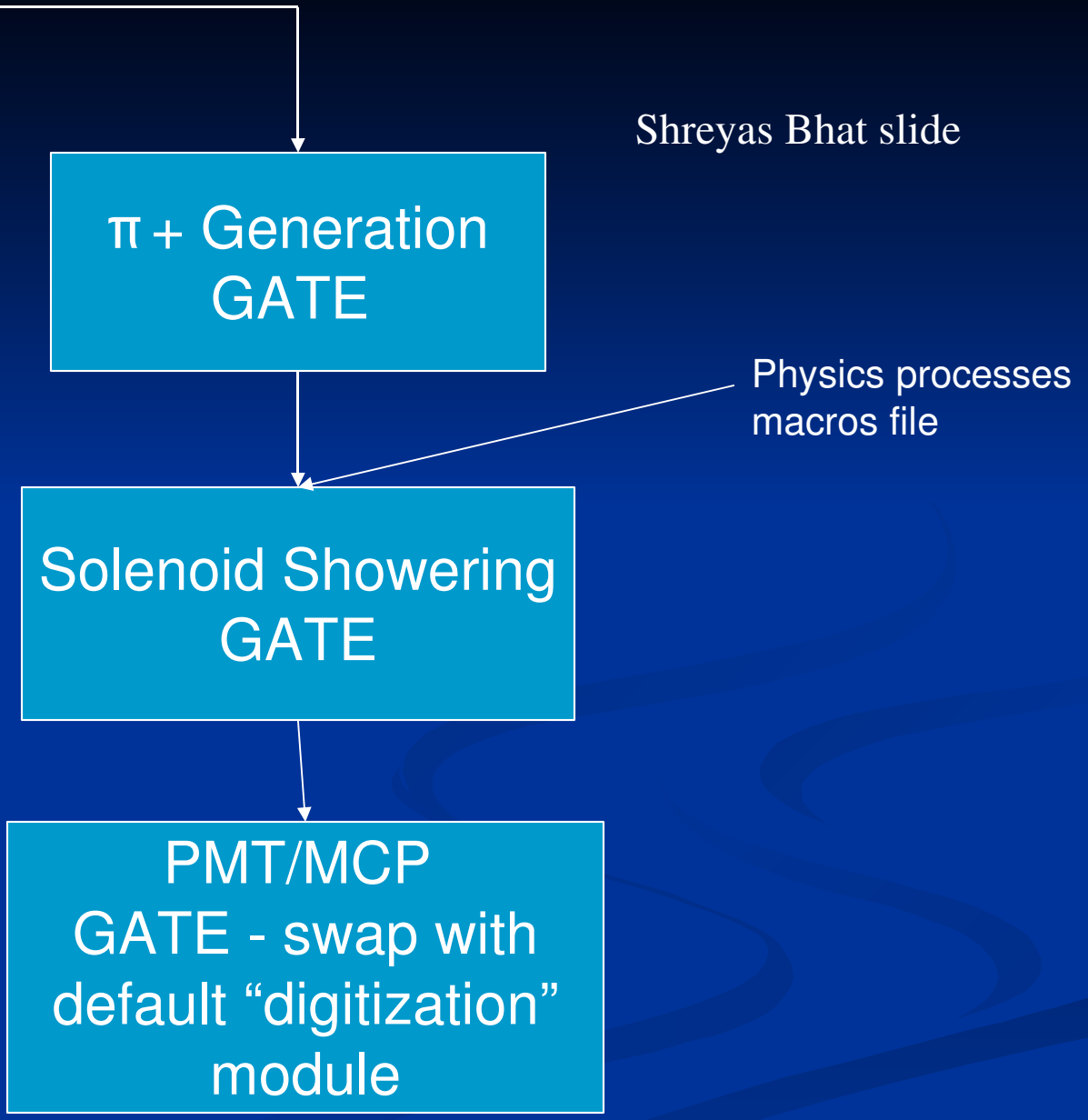
PMT/MCP GEANT4 - swappable

Pure GEANT4

Get position, time

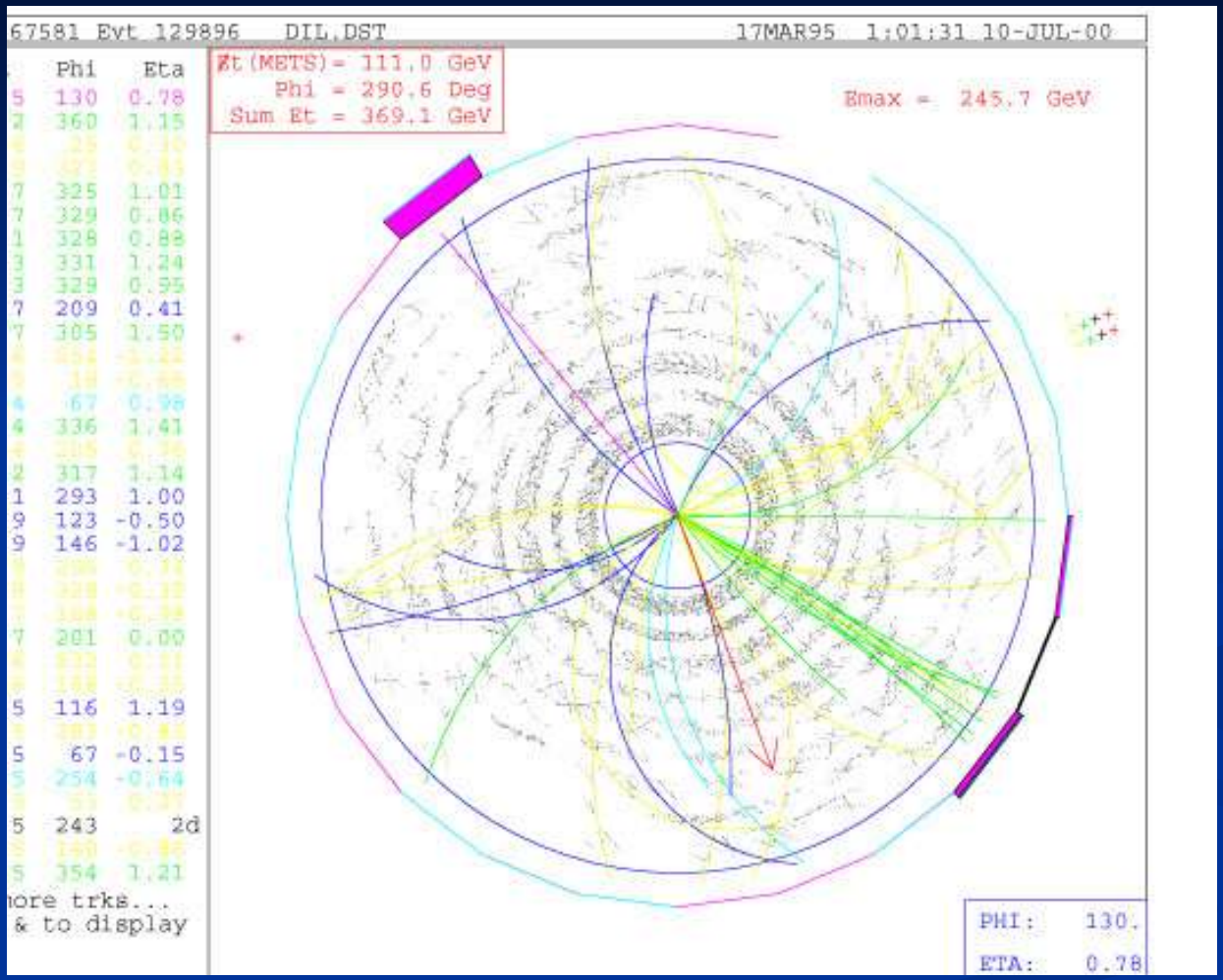
Shreyas Bhat slide

Input Macros Files - precompiled source
- Geometry
- Materials
- Particle:
  - Type
  - Energy
  - Initial Positions, Momentum
- Verbose level



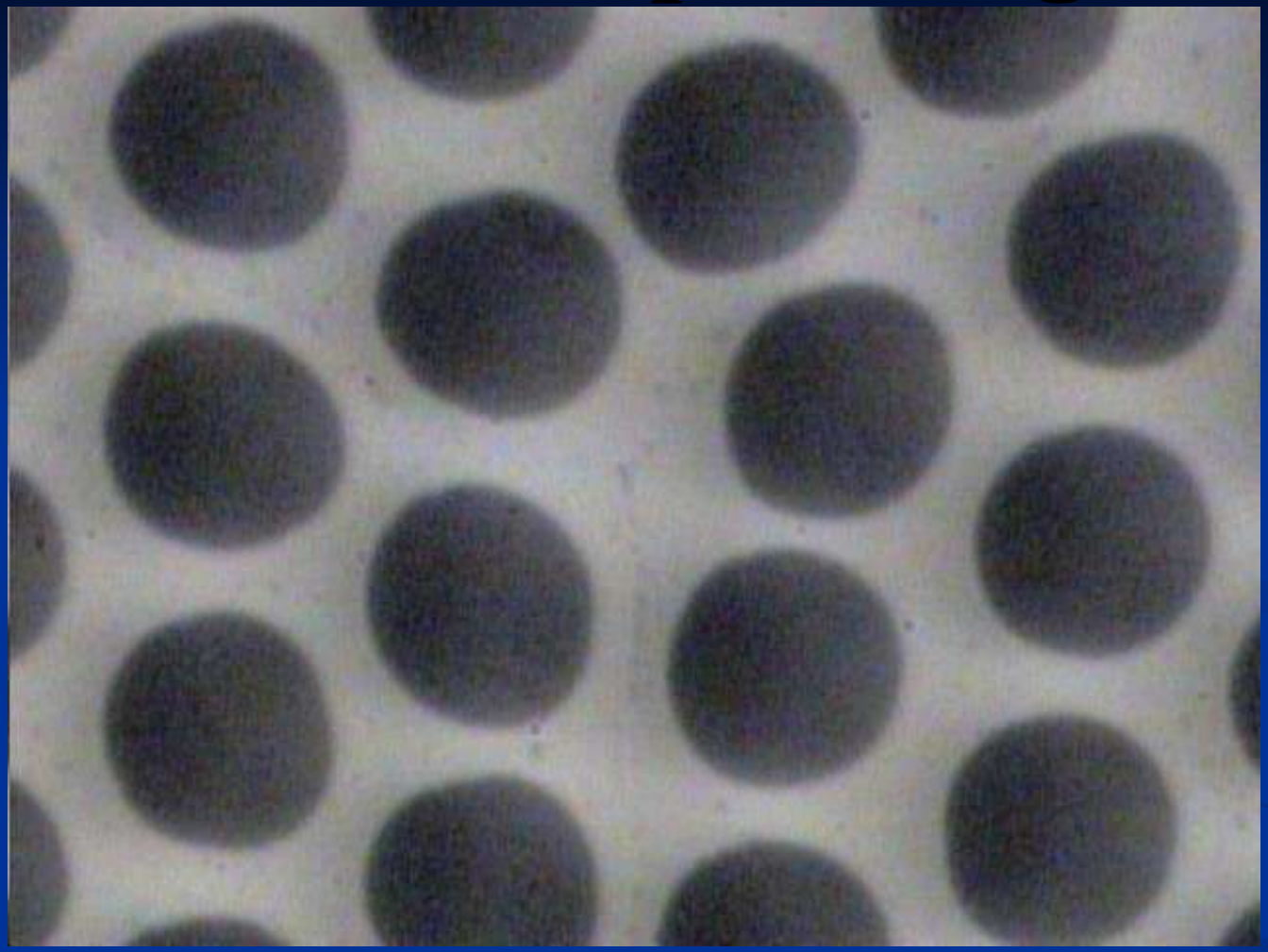
But, we need to write Source code for Magnetic Field, recompile

A real CDF event- r-phi view



Key idea- fit t_0 (start) from all tracks

MCP's have path lengths <<1 psec:

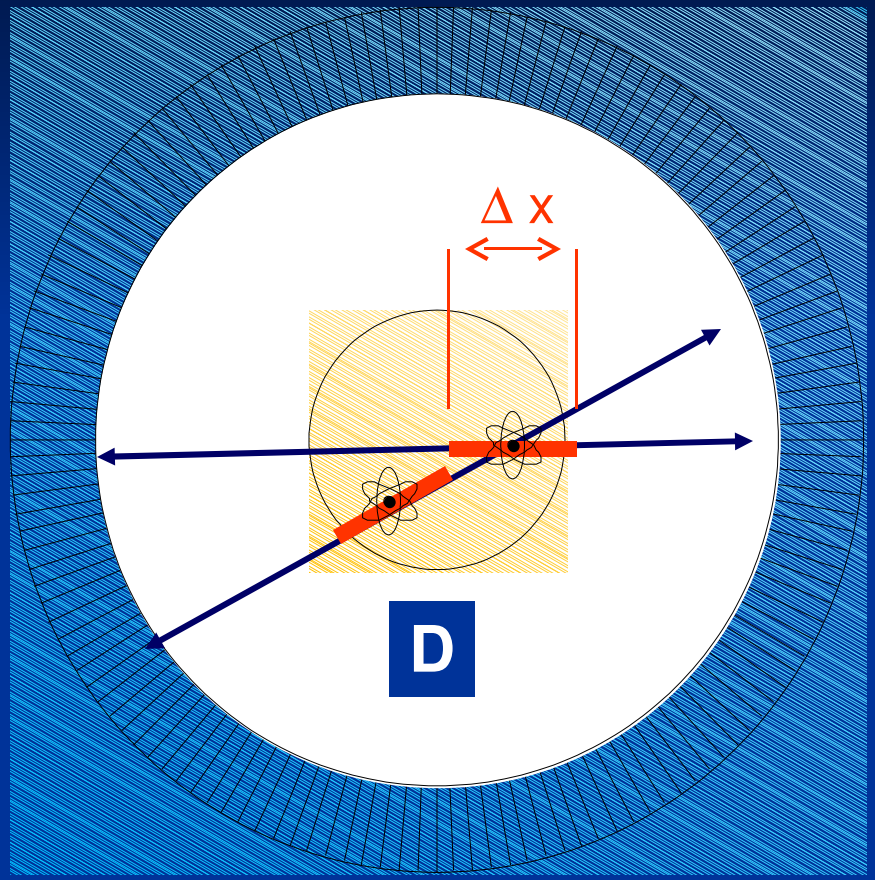


Micro-photograph of Burle 25 micron tube- Greg Sellberg (Fermilab)

Can buy MCP's with 6-10 micron pore diameters

Time-of-Flight Tomograph

Slide from Chin-Tu Chen (UC) talk at Saclay Workshop



- Can localize source along line of
  depends on timing resolution of detectors
- *weighted back-projection along line-of-response (LOR)*

Δx = uncertainty in position along LOR

$= c \cdot \Delta t/2$