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The Electrical Circuit and Internal Resistor/Capacitor Strings for Large-Area MCP-PMT's

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Abstract

In this little note we describe the electrical circuit for the large-area MCP-PMT development, including a scheme for an internal HV distribution. This current string, which is composed of series-resistors with stiffening capacitors, supplies current to the photocathode and micro-channel plates that form the amplification section of a large-area planar photo-detector. The design has the capacitors and resistors completely inside the vacuum volume, fed by metalized surfaces on the top and bottom plates of the package, with no penetrations of pins necessary through the side walls or bottom plate.

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1 Introduction

We are converging on a mechanical design for the first-generation proof-of-principle large-area 'frugal' fast planar photo-detector based on glass packaging. The plan is that this generic design could then be customized in parameter space for different applications with different requirements. For example, cost, area, and (possibly) quantum efficiency are important parameters for large water Cherenkov neutrino detectors; time resolution, occupancy, depth-of-buffer, and thinness are key for high-energy physics collider detectors; cost, footprint, data reduction, and system issues are important for medical imaging, and cost and ease of manufacture will be essential for the adoption of these for digital calorimetry.

The mechanical design is intimately connected with the electrical design, as might be expected for a large object with a high ($\approx 10^6$) gain and a bandwidth in the multi-GHz region. The paths for the high-frequency (RF) signals are now well-defined, consisting of 50-ohm strip lines on the anode, with each of the strip line pairs being read out differentially on each end by fast (20 GS/sec) wave-form sampling chips. In this note we describe the HV DC path [1].

2 Overview of the Mechanical Design: Supermodules and Tiles

The basic unit of the large-area glass-based photo-detector is an 8"-square MCP-PMT sealed tube ('tile'). These tiles will be assembled in a larger 'Supermodule' with a common readout. Figure 1 shows the basic 'SuperModule' layout of 6 tiles in a 3×2 array, forming a unit with a photo-sensitive area of 24" × 16". The components of the SuperModule are as follows:

- Tiles: the tiles are sealed glass vacuum tubes, 8.86" by 8.66", with a sensitive area of 8-inches square. HV is brought in to the vacuum volume by the electrode on the underside of the window; ground is brought in by the silver conducting surface on the anode plate. There are no other external connections (signals are collected on strip lines on the top of the anode, and these are all connected as ground at the interface between the vacuum and the outside, under the sidewall.) Figure 2 shows an exploded view of the tile. Starting at the top, one sees the window with the photocathode on its inner surface, the Gap 1 spacers, MCP-1, the Gap 2 spacers, MCP-2, the Gap 3 spacers, and the top conductor of the strip-line transmission lines.
- Tray: The supermodule tray consists of the lower anode board, the Analog board, the Digital board, and a honeycomb support structure. Figure 3 shows the 6-tile supermodule including the tiles, the Analog Board with front-end chips, and the Digital Board with the clock cleaner, FPGA, power and HV connectors, and serial interface.
- Lower Anode Board: This is a 27"-long printed-circuit card with the strips that form the lower half the strip-line pairs on its upper surface.
- Analog Boards: These are a pair of printed-circuit cards, one at each end of the Lower anode board, on which the front-end chips are mounted[2]. The analog boards provide

[1] We note that the high frequency signal path is not completely decoupled from the DC path, as charge has to return to the MCP's, and we have found that capacitive decoupling around the edges of the Burle 2" Planacons helps with ringing.

[2] There are 40 strips per tile, and so at the ends of the Tray there are 80 strips total. It may be that we want to have 2 analog cards per end with 10 chips each rather than a single one with 20.

the transition between the long strips, which are on a 0.2" pitch, and the front-end chips, which have pins (currently) spaced on a 114 microns pitch. These will be soldered onto the lower anode board with the analog board strip-side down.

- Digital Boards: These are a pair of printed-circuit cards, one at each end of the Tray on the backside (side away from the tiles) of the honeycomb support structure. The digital board houses the FPGA, the local jitter-cleaner chip [1], serial link, and power connectors, and is connected electrically to the ASIC outputs from the Analog Board.

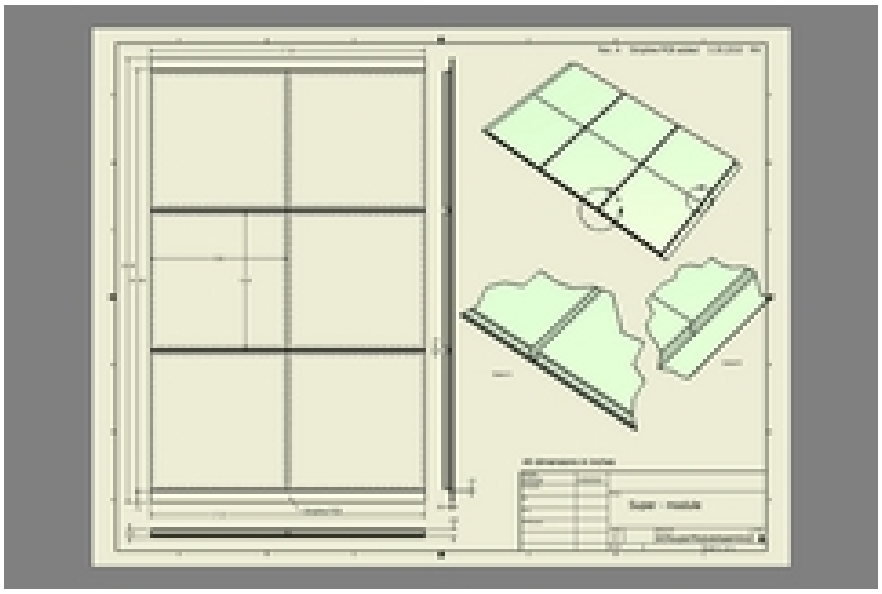

Figure 1: The basic 'SuperModule' layout of 6 tiles in a 3×2 array, forming a unit with a photo-sensitive area of 24" × 16". The tiles are fastened with a light glue or double-sticky tape onto a 'Tray' that contains the bottom anode strip lines, which run the length of the tray. On each end of the bottom anode substrate a printed-circuit card (the 'Analog Card') contains twenty 4-channel Psec ASICs. The analog card is soldered onto the anode substrate, picking up and continuing the anode strips directly into the 50-ohm inputs of the front-end ASICs. A 'Digital Card' that contains the FPGA for front-end control and data-reduction, a jitter-cleaner chip, and the optical fiber interface, is situated on the backside of the honeycomb support structure.

3 The Signal Path and the 'Inside-Out' Anode

The anode shown in Figure 2 consists of a top layer and bottom layer of transmission-line strips, with glass in-between. The width of the traces, thickness of the glass, and glass dielectric constant are all such that the lines are 50 ohms at a few GHz.

We have, however, shorted all the lines together on the top of the glass (i.e. the vacuum side) as shown in Figure 4 so that the sidewall frame can be bonded to a homogeneous silver surface, rather than having to cross the strips. The strips on the bottom layer are thus the 'signal' and those on top are the 'ground' for the signals on the lines, which are looked at differentially by the front-end chips at the ends of the lines [3]. The bottom trace then can

[3]This is analogous to grounding the center conductor of a long cable and floating the braid– one still sees the differential signal at the end of the cable, although inverted.

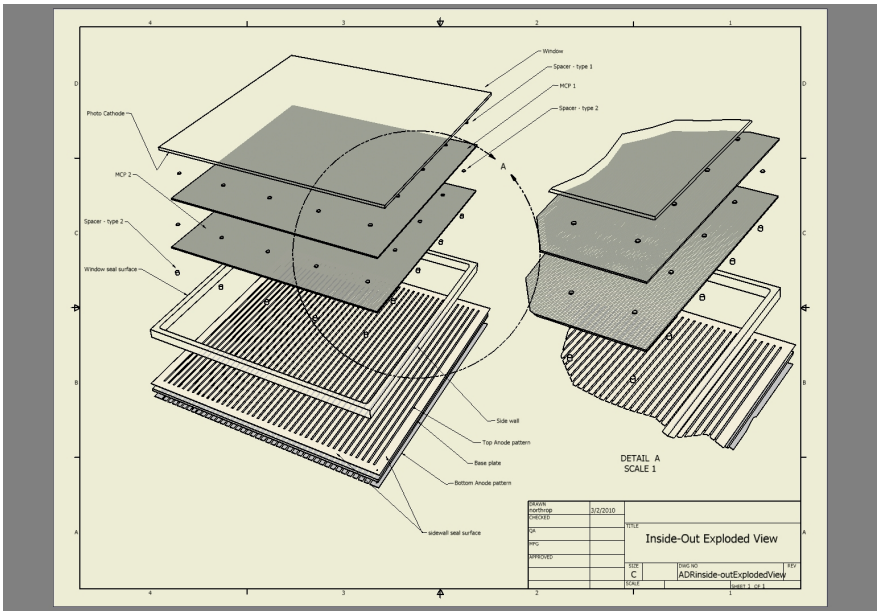

Figure 2: An exploded view of the $8'' \times 8''$ tile. Starting at the top, one sees the window with the photocathode on its inner surface, the Gap 1 spacers, MCP-1, the Gap 2 spacers, MCP-2, the Gap 3 spacers, and the top conductor of the strip-line transmission lines.

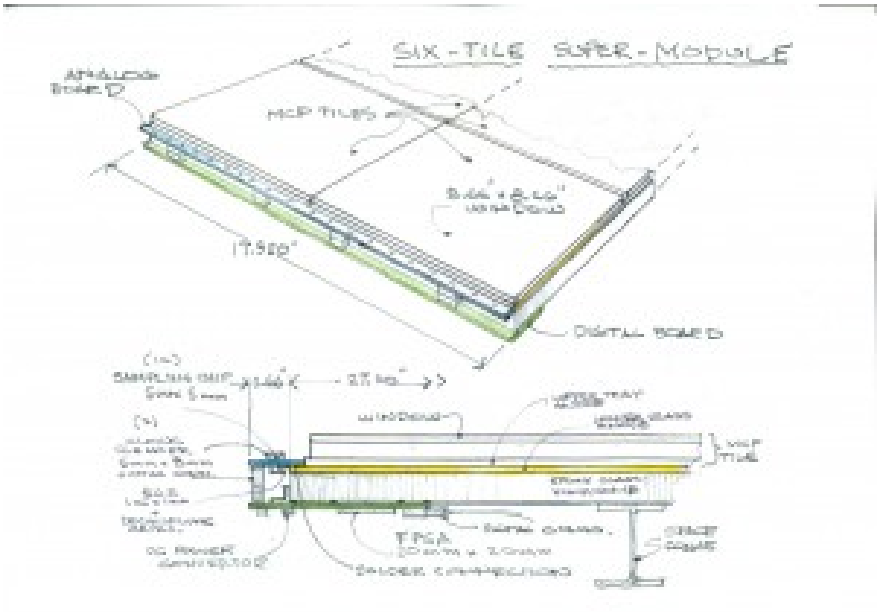

Figure 3: The 6-tile supermodule showing the tiles, the Analog Board with front-end chips, and the Digital Board with the clock cleaner, FPGA, power and HV connectors, and serial interface.

be on the top surface of the 'Tray' rather than on the bottom surface of the tile, so that there are no signals that need to brought out of the vacuum volume of the tile. One only has to connect the grounds tile-to-tile or tile-to-tray, and this can be done with a copper strip along the tile edges.

The bottom line here (no pun intended) is that no signals need to be brought out

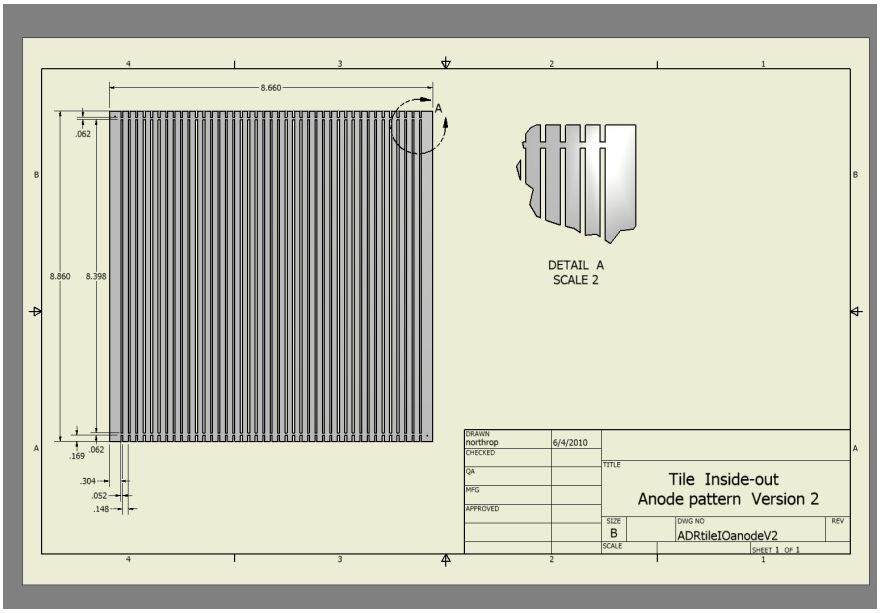

Figure 4: The 'ground' anode traces in the 'inside-out' design, showing the interconnection between the traces under the sidewall (see Detail A). The interconnection has a mechanical function, preventing a direct path for vacuum leaks through the bottom seal along the strips. Electrically it provides a dead short DC connection for the 'ground' side of the signals, while at RF frequencies the lines function independently as the top traces of their transmission strip lines pairs.

through the sidewalls or back plate- the tile needs only to be stuck down on the tray. The signal path is thus very simple to construct.

4 The 'No-Hands' High Voltage Current String

This note is to suggest a similar solution for the HV current path, with the HV transmitted to the photocathode and the four MCP electrode surfaces by metalization on the bottom side of the window (i.e. the vacuum side). The ground is the same ground as the signal, which is differential with respect to it to ameliorate power-supply common mode noise.

Figure 5 shows a side-view of the stack-up of the MCP layers. Gap 1 is at the top (Photocathode to MCP1-In), and Gap 3 is at the bottom (MCP2-Out to Anode).

4.1 The Proposed Integral Resistor/Capacitor Chain

Figure 6 shows the circuit diagram for the HV. The design requires that resistors and capacitors in each gap be integral to the spacers; we do not know if this is possible, but are hopeful that this can be done using ALD [2]. Note that C3 stiffens the HV string at the point of highest current, after MCP2 where the gain is largest by a factor of 1000 [4]

[4]We note that in a conventional PMT the voltage divider is stiffened for the last dynodes; in a two-MCP PMT as described here MCP2 has a gain of about 1000, comparable to the last 6-10 dynodes in a PMT.

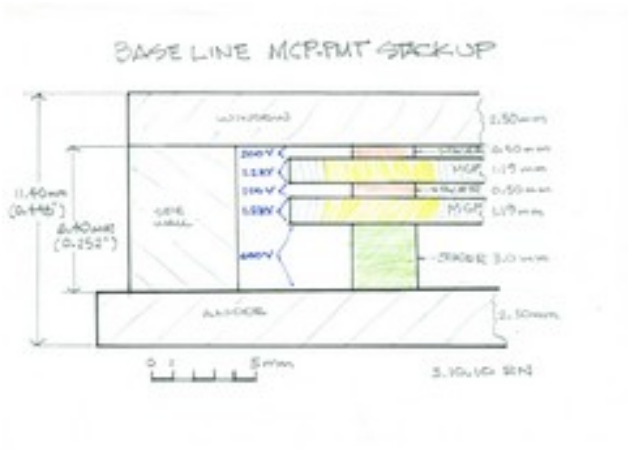

Figure 5: The 'stack-up' of the tile. Gap 1 is at the top (photocathode to MCP1-In), and Gap 3 is at the bottom (MCP2-Out to Anode). HV enters at the top of the sidewall; ground enters and leaves under the bottom of the sidewall. Note that the values shown for gaps and voltages need to be determined- for now one should use the values in Table 1.

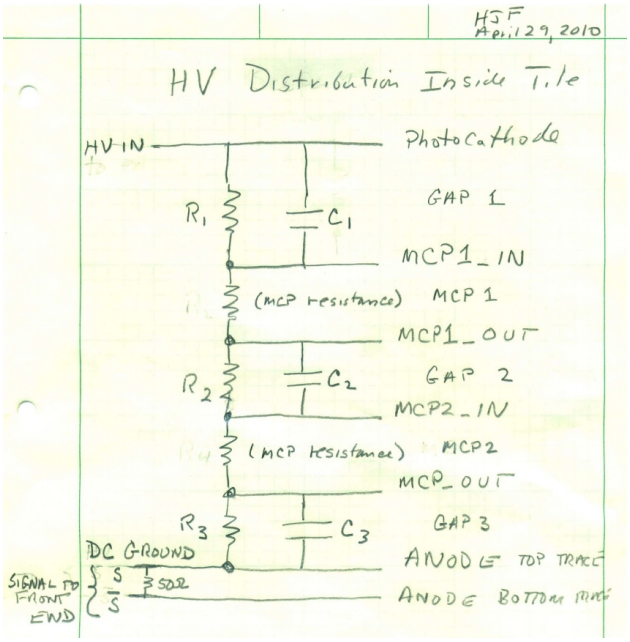

Figure 6: The circuit diagram for the HV. The design requires that resistors and capacitors in each gap be integral to the spacers

4.2 Sample Calculation of Resistor Values for the Current Supply Chain

Suppose we desire the capability of a 1 MHz rate in an 8"-square tile, i.e. 16kHz/in-sq, with a 100 mv output pulse of width 1 nsec, driving 50 ohms (this is very conservative, as the output pulses will be smaller). The average current is then:

$$I = (Rate)(I_{pulse})(\Delta t) \tag{1}$$

$$I = (1MHz)(0.1V/50ohms)(1nsec) \tag{2}$$

$$I = 10^6(2 \times 10^{-3}) \times (10^{-9}) = 2 \times 10^{-6}Amps \tag{3}$$

We would like the string to carry 10 times this peak average current of 1 μA, i.e. we need a supply string capable of supplying at least 20 μA.

Taking Ossy's recommendation for 10 MΩ for the MCP resistance (8"by8") as a starting point, and a nominal operating voltage for a single MCP plate of 1 KV for convenience of calculation, we find the current through the MCP to be

$$I = V/R = 10^3/10^7 = 10^{-4} = 100\mu A \tag{4}$$

which satisfies the current requirement by a factor of 5.

We can then calculate the resistance of each element in the string. There are a number of considerations on the gaps and voltages that can be determined by simulation and confirmed by measurements:

1. The simplest solution for the spacers is to have the spacers in each of the 3 gaps to have the same resistance per length. This allows doing all the spacers in the same batch, presumably our best chance to have them all have the same resistance and the most uniform behavior versus other factors such as temperature, aging, contaminants;
2. A higher voltage and shorter path in Gap 1 should result in a lower TTS [3];
3. A higher voltage in Gap 2 results in fewer pores being illuminated in MCP2, and hence a lower gain (fewer saturated pores) but narrower distribution (all pores saturated) [4];
4. A larger Gap3 and lower voltage spreads the charge out over more strips, possibly allowing better centroid finding and better uniformity.

The HV chain starts with an external connection (outside the vacuum) to the metalization on the bottom side (inside the vacuum) of the top window (see Figure 5). Table 4.2 gives the height, voltage, and resistance in each element. For simplicity now we will take the spacers to have the same resistance per unit length.

Name	Height	V	I	R_{Tot}	N_{spacer}	R_{spacer}	κ
G1	1.0 mm	200 V	100 μA	2 MΩ	25	50 MΩ	5000 Ω-cm
MCP1	1.2 mm	1200 V	100 μA	12 MΩ	–		
G2	0.5 mm	100 V	100 μA	1 MΩ	25	25MΩ	5000 Ω-cm
MCP2	1.2 mm	1200 V	100 μA	12 MΩ	–		
G3	2.5 mm	500 V	100 μA	5 MΩ	25	125 MΩ	5000 Ω-cm
Total	6.4 mm	3.4 KV	100 μA	32 MΩ	–	–	–

Table 1: The dimensions of the elements in the current string, shown in Figure 5. Gap 1 (G1) is the photocathode-$MCP1_{IN}$ gap, Gap 2 is between the 2 MCP plates, and Gap 3 is the $MCP2_{OUT}$-Anode spacing. Each gap has 25 spacers made of 3-mm diameter glass rods, coated with ALD to achieve the resistance R_{spacer} per spacer and hence a parallel resistance of R_{Tot}. The last column, κ, is the ALD sheet resistance in Ω-cm

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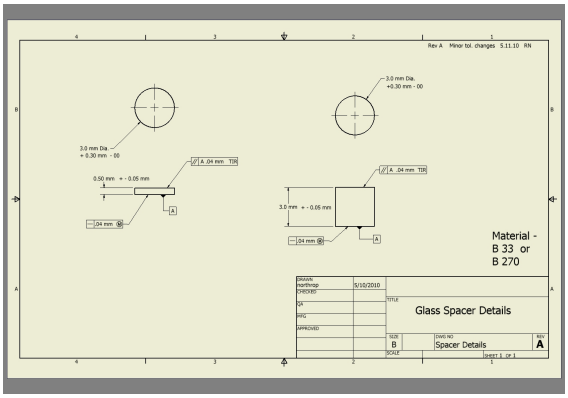

Figure 7: The dimensions of the 2 kinds of spacers- Gaps 1&2 and Gap 3.

Figure 7 shows the dimensions of the two kinds of spacers- Gaps 1 and 2, and Gap 3. Both are made from glass rod cut into precise lengths; the rod should be (more-or-less) CTE matched to the glass window and anode.

A quick approximate calculation of the ALD sheet resistance on the sides of the cylindrical spacer follows. The resistance of the spacer is given by:

$$R = \kappa L/A = \kappa L/(\pi t d) \tag{5}$$

where L is the length, A is the area of the resistive layer, d is the diameter of the spacer, and t is the thickness of the resistive layer. Putting in typical spacer values of L= 0.1 cm, d= 0.3 cm, t =100 nm = 10^{-5} cm, and R = 50 MΩ (see Table 1), we find the sheet resistance is

$$\kappa = RA/L = R(\pi t d)/L = 5000\ \Omega{-}\text{cm}. \tag{6}$$

4.3 Capacitor Values for the Current Supply Chain

In a photomultiplier one typically stiffens the last several stages with increasingly large capacitors, and also has a cap across the HV-to-ground total string. In this MCP design we have effectively only two stages, and so it is only the second MCP that needs the stiffening. Each spacer adds local capacitance, with the total being the sum of the parallel caps.

There are two functions of these caps:

1. stiffening the string so that the DC voltage doesn't dip after a pulse, and
2. providing an AC high-frequency return path for the fast pulse to diminish ringing (bypassing) [5].

4.3.1 Stiffening- Storing locally distributed charge

The charge in a single pulse is

$$I\Delta t = 2\mu A \times 10^{-9} = 2 \times 10^{-15}\ \text{Coulombs} \tag{7}$$

If we want to have charge for 1000 pulses stored locally, i.e 2×10^{-12} Coulombs, we need a capacitance of

$$C = Q/V = 2 \times 10^{-12}\ \text{Coulombs}/1000V = 2 \times 10^{-15}\ \text{Farads} = 2fF \tag{8}$$

which is tiny, and at the macroscopic level of the spacers is already supplied by the MCP plates.

4.3.2 Bypassing

We have had good success with bypassing the perimeter of the 2" Planacon with 3 capacitors per side, connecting the anode to MCP2-OUT. Each capacitor is 100 pf [7], and as they are small they are very low inductance. If we can make each spacer a capacitor we will have distributed bypassing capacitance.

5 Tolerances

5.1 Tolerances on the Resistance Values of the MCP's and Spacers: ALD Considerations

The relative resistances in the HV divider string shown in Figure 6 determine the voltages across the MCP's and gaps. As the sheet resistance between the spacers and the MCP's is different, the ALD process breaks up into two separate runs, one for the spacers and one for the MCP plates. There is no gain in the gaps, and we believe the dependence on the voltage is mild (simulation and measurements will eventually tell us if this is so). The MCP's, however, have a a strong dependence of gain vs voltage, typically a factor of 1.7 per 100V at 1.6KV [6]. Consequently the resistances of the two MCP's should be matched. For a 10% difference in gain from MCP1 to MCP2, the two should have an overall resistance difference less than 1% (18V out of 1.6KV gives a 10% gain change). Tests will show whether or not the resistances of the two plates track with temperature and use.

In summary, the tolerance for the absolute resistance of the spacers is 10-20%, and is not critical. The relative resistances for the spacers should be the same within 10%, and as they are made in the same batch, this should not be a problem.

The tolerance on the average resistance for the MCP's is also not so critical, e.g. 10%. However in this scheme the two MCP's should have the same resistance within 1-2%, which is tight.

5.2 Tolerances on the Capacitance Values

The tolerances on the capacitances are very loose- up to 50% even would be acceptable. Whatever is natural for the process we can accept; it would, however, be good if all the capacitors in a single batch come out the same within 10%, for example.

6 The Window and Anode HV Path Patterns

The pattern on the inside of the window, shown in Figure 8, serves three functions: 1) it provides a uniform metal surface for the top seal between the sidewall and the window; it distributes HV across the large photocathode so that there is no voltage drop in the PC itself; and 3) it distributes current to the resistive spacers that form the HV string to ground, providing current for the MCP amplification.

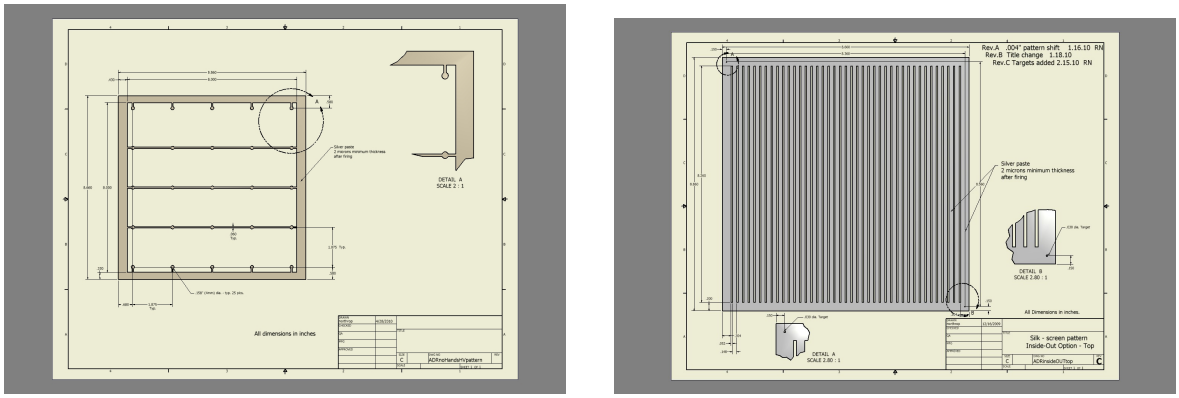

Figure 8: The electrode patterns on the window (left) and top of the anode (right).

7 Acknowledgments

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References

[1] For example, Texas Instruments CDCE72010.
See: http://focus.ti.com.cn/cn/lit/an/scaa091/scaa091.pdf for a nice introduction to phase noise/jitter.

[2] Private communication, Jeff Elam, Anil Mane, and Qing Peng

[3] Lionel DeSa; *Simulation of the Photocathode gap*, Psec Blog; Tuesday, May 20th, 2008

[4] Matt Wetstein, private communication. Also see the curves from Wiza, posted on the Blog by Matt on April 5th, 2010; *" Effect of 100 micron gap between plates at various bias voltages"*; The paper by Wiza can be found in the psec library at http://psec.uchicago.edu/Papers/.

[5] Timothy Credo, Henry J. Frisch, Harold Sanders and Fukun Tang; Developing Large-area Psec Timing: April 5th, 2010 The MCP Return-Path Problem and a Proposed Solution.
http://psec.uchicago.edu/library/doclib/ July, 2006

[6] For example, see M. Wetstein, MCP Godparent Review, March 25, 2010; linked to the Psec Library page.

[7] Johanson Dielectrics, 100pF, 500V; Model 501R15N101KV4T.