The Development of Large-area, Picosecond Resolution, Time-of-Flight Detectors

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1 Introduction

Many of the most important measurements in Elementary Particle Physics involve 'flavor'- the type of quark or lepton. The three charged lepton flavors, the electron, muon and tau, can be easily distinguished by their differing interactions with matter, as the electron makes a distinctive shower in heavy materials, the muon is highly penetrating in matter, and the tau lepton is unstable and decays. However identifying the flavor of the quarks inside long-lived hadrons remains impossible at the momenta typical of current and future energy-frontier particle accelerators, the Fermilab Tevatron (FNAL) in Illinois [2], the Large Hadron Collider (LHC) at CERN [3], or the planned International Linear Collider (ILC) [4].

The most important high-energy measurements testing the Standard Model of particle physics such as the precision measurement of the masses of the top quark and the W boson, and the discovery of the Higgs particle and precision measurement of its mass, will require the ability to identify the flavor of hadrons to reach their ultimate precision. The important measurements beyond the Standard Model, those we expect to make at the LHC, the proposed future ILC, or possibly sooner at Fermilab, will also require flavor identification to unravel the physics of the complex final states we expect from the decays of new heavy particles. These particles would arise from the existence of some new basic phenomena that must be present at energies close to those of the LHC in order to correct the predicted breakdown of the 'low-energy' effective field theory that we call the Standard Model. Possible candidates for these phenomena are Supersymmetry, Large Extra Space Dimensions, and/or new larger gauge groups, among others.

Precise measurement of the masses of heavy particles such as the Higgs, the top quark, and as-yet unobserved new particles involves being able to reconstruct the flavor of jets. The heavy flavor states produce K-mesons, which can be used to 'tag' and reconstruct the heavy flavor D and D^* mesons. These charm-flavored states, in turn can be used to tag even-heavier bottom-flavored quarks. The identification of bottom quarks is crucial to studies of the top quark, which decays into the bottom quark and a W boson, and the discovery of the Higgs boson, which decays into a bottom quark pair. In addition, charm is produced in half of all W-boson decays, and a precise measurement of the W mass will eventually need to distinguish charm jets from the lighter flavored quark jets.

The ability to measure the mass of particles produced in very high-energy collisions, such as those now at the Fermilab Tevatron, and soon to be at the LHC, has remained out of our reach beyond momenta of a few GeV. We propose here a new technique, which if successful, will allow the identification of particle type for particles with momenta 10-times higher than is presently possible, allowing substantial improvements in top, bottom, gauge boson, and Higgs boson physics at very high energy colliders [5].

The technique might also be extended to allow another now-impossible capability: the association of photons with individual vertices at the LHC [5], where there will many collisions per beam crossing, by localization in both time and space. Ultra-fast timing could possibly be used in some experiments, such as kaon rare decay experiments, in conjunction with a conventional momentum measurement to improve the momentum resolution assuming a mass.

Figure 1 shows the contours of 1-σ separation for pions, kaons, and protons versus the time resolution of the flight time over a 1.5 meter path. The simulations we have done so far give a resolution on the order of 1 psec for a single module; if this could be achieved in a large system it would allow π/K separation to 15 GeV or so at the 1-σ level.

In this proposal, we propose to make critical steps to develop, integrate, and test the electronics necessary to measure the transit time of particles ("time-of-flight", or "TOF") approximately two orders-of-magnitude better than current large-scale systems. For highly-relativistic particles this translates into an order-of-magnitude gain in the momentum range over which particles can be identified. The proposed method has some novel features: the basic detection is of Cherenkov light generated in the face window of a large array of custom micro-channel plate photomultipliers (MCP-PM's), a new charge-collection scheme at the anode of the tube, and the development of custom readout electronics, integrated with the anode, one-to-two orders-of-magnitude faster than is currently used in high-energy physics. Without the anode design a large area TOF system would have too large a number of electronics readout channels to be feasible mechanically, electrically and financially. Without custom electronics mounted directly on the devices themselves and supported by a system with sub-picosecond stability the devices are themselves not useful.

The present proposal focuses on the development of the readout electronics necessary for the large-area picosecond resolution TOF system that would be appropriate in HEP collider or fixed-target experiments. The development of time-to-digital converters (TDC's) with sub-picosecond resolution and stability is far beyond the present state of the art [6, 7, 8, 9, 10]. The electronics for signals at such high-frequencies must be integral with the sensor, rather than in a rack separated by cables.

We have identified a new IBM process [11] for fabricating integrated circuits ('chips')

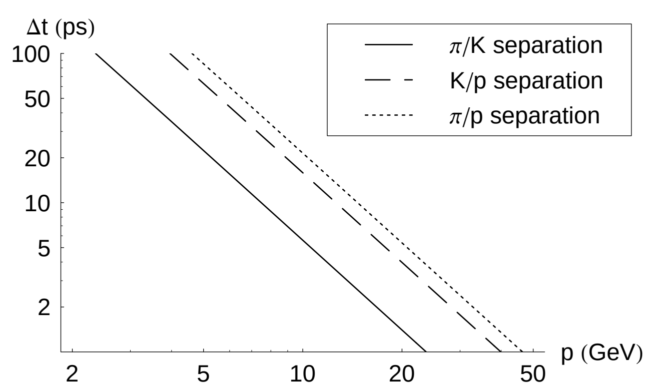

Figure 1: Contours of 1-sigma separation for pions, kaons, and protons versus the time resolution of the particle flight time over a 1.5-meter path for a detector with 1-psec resolution.

capable of the necessary precision and have acquired access to the chip foundry. In addition there is a similar process at the IHP MicroElectronics foundry available through Europractice; we have also gained access to their program and design toolset. While the IBM process is faster (jitters down to 70 femtosec), the IHP program is appreciably cheaper and still is acceptable (jitters in the several-hundred femtosecond range). One of us (Tang) has recently traveled to Europe to take a course from IHP on the new design tools; these tools are now installed and operating at the University of Chicago.

The proposed individual detectors are 5-cm by 5-cm photo-multiplier/micro-channel-plate modules, with MgF windows using the novel equal-time anode design. Figure 2 shows a schematic representation of one MCP-PM module. These modules could be assembled in large arrays of different geometries, including a cylindrical array that would cover the central region of one of the large detectors at a hadron collider such as the CDF [12] detector at FNAL, a new detector at a 'super B-factory' [13], or an upgrade to one of the LHC detectors. The addition of an array of these detectors would allow a program of precision measurements in bottom and top physics after the currently proposed programs at the Tevatron, and would enhance the detectors at the LHC and perhaps at the proposed International Linear Collider. Other geometries are possible, one example being a plane of pico-second TOF measurements in a 'forward' geometry such as LHCb or a rare-K-decay experimental setup such as the $K^0 -> \pi^0 \nu \bar{\nu}$ experiment in Japan (in the latter case the the devices would be preceded by a converter for the photons).

To cover a large collider detector will require a system of submodules, each capable of measuring times to approximately 1 picosecond (10^{-12} sec), the time it takes for light to travel 300 microns. Figure 3 shows an example layout of the submodules in the geometry of the coil of the CDF detector at Fermilab as an example. The system would consist of 10,000 individual 5-cm by 5-cm MCP-PMT detectors, arranged in a tiling pattern as shown. The submodules are less than 1-inch thick, with the readout chips directly on the back surface of the detectors (see Figure 4). The distribution of the system reference clock is by axial lines running down each row of detectors. Digitization is directly in the chips, and because the occupancy is relatively low, a sparsified readout is not a technical challenge. The challenges of stability and precision over a big system, however, are difficult, and have dominated our effort so far.

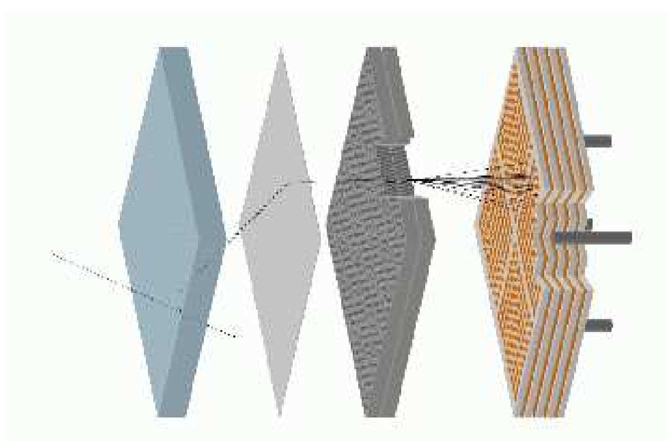

Figure 2: A schematic representation of the MCP-PM showing the construction of the custom anode assembly (the multi-layer assembly on the right of the picture).

2 Prior Work in the Field

There are two main techniques used in HEP to identify high-energy particles. The Cherenkov technique distinguishes particles by measuring the angle of light emitted by particles traversing a transparent radiator. This is the basis of the techniques used by the Belle experiment at KEK in Japan [14] and the BABAR experiment at SLAC [15]. In the limited path length available in a cylindrical collider experiment the technique provides particle identification only up to a few GeV. In addition, it can take significant radial space, which is unlikely to be available at an existing detector. The second technique is time-of-flight (TOF), in which the transit time from the creation of a particle to its arrival at an outer ring of detectors is measured. The 'start' time is inferred ('fit') from the ensemble of particles detected at the periphery. Knowing the distance traveled and the time of travel gives the velocity. The CDF experiment at FNAL uses this technique, with a typical time resolution of 110 psec [16]. In both techniques, combining the velocity measurement with the momentum measurement in the magnetic spectrometer one can measure the mass of the particle, and hence its identity (e.g. pion, kaon, or proton). The idea of using Cherenkov light for fast timing as it is made coherently by the particle is not new; one of us (HF) has used it in the early 70's for beam diagnostics, for example, and it was not new then. A test was done using micro-channel plates and externally generated (i.e not from particles traversing the window) Cherenkov radiation by C.Lu, D.Marlow and K.T. McDonald in 1994 [17]. Timing with Cherenkov radiation in quartz bars was proposed for the MUCOOL Collaboration, and a resolution of 10 psec was predicted if one used Hamamatsu MCP's [18]. A custom micro- channel plate for use in an application timing particles in a beam for momentum analysis was developed at Fermilab; this device had a single monolithic anode [19]. What is new is that our proposed device differs substantially from the Fermilab design in purpose, system layout, radiator and anode. In addition, the proposed electronics development, integrated with the anode design, is ground-breaking in HEP.

There is currently also a substantial effort in Japan along similar lines to our effort, but with some major differences [20, 21]. They have as a goal a different operating principle,

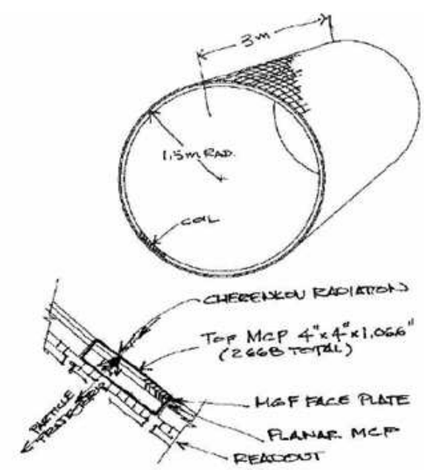

Figure 3: A schematic showing the placement of photo detectors around a detector solenoid coil. The detectors may also be placed just inside of the coil. The inset shows a sketch of a single detector (i.e. 'submodule').

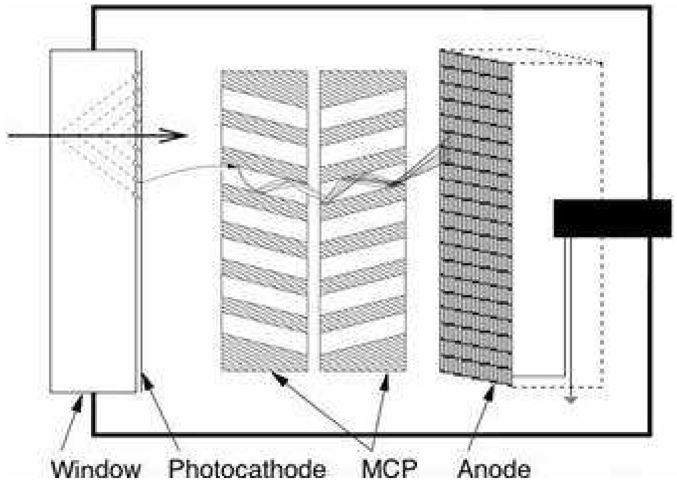

Figure 4: A 'cartoon' of a side of a MCP-PMT module, showing the Magnesium-Fluoride window at left, followed by the chevron micro-channel plate, the multi-pad anode, and the pin that penetrates the back of the device to the readout chip. The actual thickness of the module is less than 1 inch, so the true aspect ratio is more like a tile than this 'exploded' view implies. Also shown are an incoming particle making Cherenkov light in the window, and the trajectory of one photo-electron and its shower in the MCP. Typical gains are $\sim 10^6$.

namely to use the angle of the Cherenkov light and they report a time resolution of 10psec, much larger than our goal of 1 psec [22]. The features of our design we consider novel, the equal-time anode, and hence the TOF system using only the time-of-arrival of the light, and the full-coverage mask are not part of their design. Our integrated circuit development, the subject of this proposal, is unique.

Other techniques, such as Pestov counters [23], have long been under investigation, but have never been considered for resolutions on the order of 1 psec to our knowledge.

We have surveyed prior work on time-to-digital conversion in the course of our recent design and construction of a 96-channel TDC [24]. References [6, 7, 8, 9, 10] summarize different electronic strategies. We have convinced ourselves that the 'ancient' methods will still apply, provided that the intrinsic jitter of the internal switches is much less than 1 psec. However we must be able to simulate all the physical and electrical characteristics of the detector-electronics unit, as at these speeds everything is analog and everything matters.

3 The Equal-Time Anode: Electrical Simulations

The anode design with its integrated electronics is critical to achieving this performance. The technique we have proposed depends for its time resolution on the development of an anode that is finely sub-divided spatially and that delivers a signal at a time that is independent of position. Figure 5 shows our design. The anode allows a single electronics channel to cover an area much larger than corresponds to the time resolution, making an array covering the area of a typical apparatus feasible. Figure 6 shows the layout on the anode of the transmission lines.

We are developing a complete simulation of the device performance, from the particle impinging on the front window to the collection of charge on the output pin. The device simulation includes the frequency dependence of the Cherenkov light, the absorption in the window, the photo-cathode response, the time jitter in the micro-channel plate, and the path-length and electrical properties of the transmission lines and pads of the anode. The simulation predicts a resolution of 0.9 psec for a commercially available MCP with 10-psec transit time spread (TTS). Figure 7 shows simulation results of the output voltage from one of the four collectors on the back of the anode. The predicted resolution from the leading edge is 0.9 psec, comparable to our stated goal of 1 psec.

We are planning to build four of these custom devices working with Burle Industries. Burle will contribute to the cost of the MCP-PM modules.

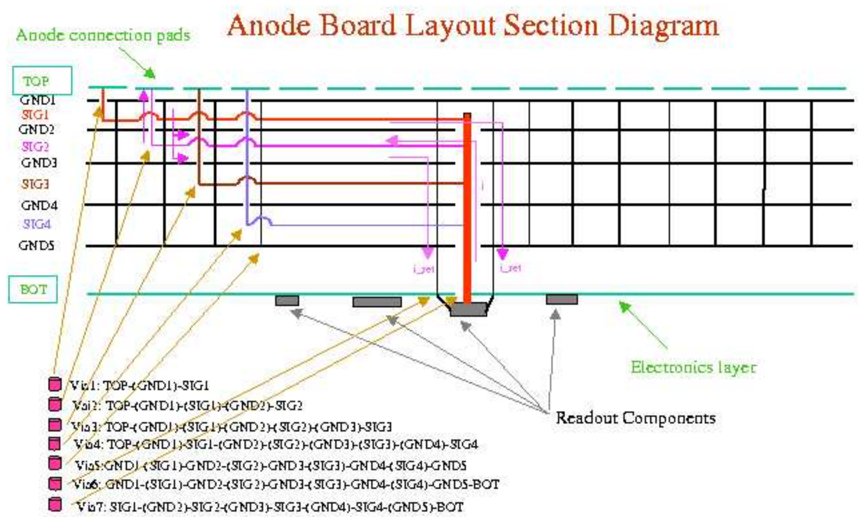

Figure 5: A schematic representation of the custom anode assembly. The top layer of the anode assembly is the actual anode, consisting of 2-mm square pads; this is the layer that receives the charge output from the micro-channel plate. The two layers of transmission line traces and their corresponding ground planes are also shown; these are constructed so that the transit time of the charge from each pad to the respective one of four central collection points is constant. Each of these collection points has a pin through the anode assembly that connects directly to the custom chip that digitizes and reads out the time of arrival

The most economical arrangement of individual MCP units to make a large- area array consists of a 'tiling', i.e. placing individual units side-by-side in a pattern much like tiles on a bathroom wall. For the large cylindrical detectors used in colliders, the tiling would be on the surface of a cylinder; for 'forward geometries' the tiling would be on a plane. The MCP modules have an active area that is smaller than the physical area of the overall device. This would lead to 'dead' areas, insensitive to particles, and hence a reduced efficiency for particle identification. We have designed a solution to the problem; a 'mask' of transparent radiating material (for example, fused silica), that covers the dead regions between the modules and transports the light to the active regions. There will be some

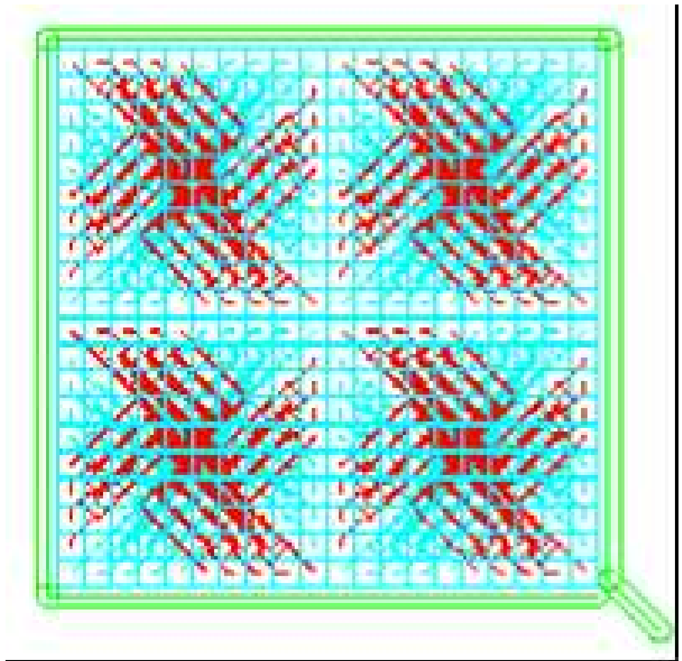

Figure 6: The layout on the anode of the transmission lines that connect the individual pads to the collection points which then directly feed the digitization chips. The transmission lines, each consisting of a trace and a ground plane, are constructed so that the transit time of the charge from each pad to the respective one of four central collection points (at the center of each large square) is constant.

degradation in timing performance, but this can be corrected 'offline' from the position of the track of the particle.

4 Picosecond Electronics: the MCP/Anode/TDC/Clock and DAQ System

4.1 Getting the Signal to the TDC

The present proposal requests support to construct the custom integrated circuits that sit directly on the anode and process the signals. The Burle 5-cm×5-cm tube we are using has a planar anode with a 32×32 array of pads. Each pad collects charge from the MCP inside the vacuum and connects to a 'via' that arrives on the back of the anode. The equal-charge collection circuit is implemented in a multi-layer PC board that 'mates' with the Burle anode on one side and has TDC and Clock/DAQ chips surface-mounted on the outer-most layer. Because the Burle device is vacuum-sealed with a low-temperature Indium alloy, the present plan is to mate the 'mating-board' with the MCP-PMT with conducting epoxy. Figure 8 shows a test in which epoxy was deposited under machine control at the juncture of four of the Burle anode pads (in this case the mating board was glass, so we could see how we did) [25].

The charge for each of the four 1-inch × 1-inch 'pixels' per MCP-PMT unit over which charge is summed is collected on a pin that back of the mating board. On each of the 4 pins per unit the collection pin connects directly to a TDC chip. The 4 TDC chips

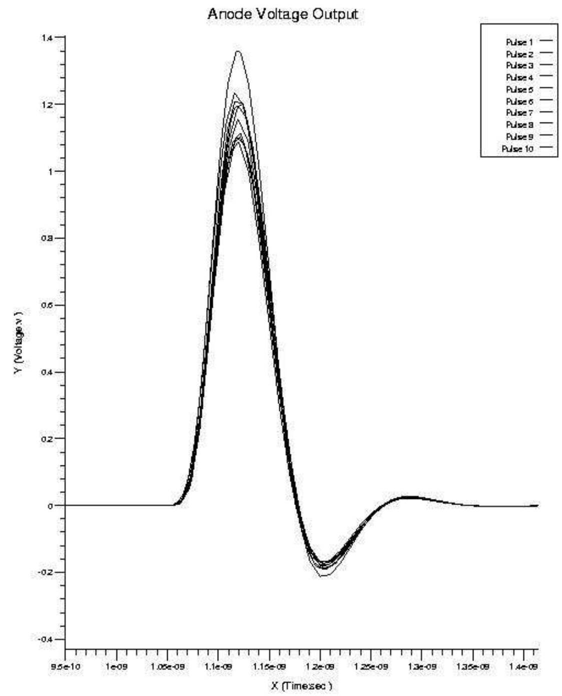

Figure 7: The output voltage from one of the four collectors on the back of the anode for 10 different simulated showers. The simulation includes the frequency response of the generation of Cherenkov light, absorption in the window, the photo-cathode response, the time jitter in the MCP, physical and temporal distributions at the anode, path length differences on the anode, and electrical characteristics of the anode. The RMS jitter on the leading edge as measured at half-height is 0.86 psec.

are serviced by a Clock/DAQ chip that multiplies up the frequency of the system clock and distributes it, and that handles the slow-control and DAQ. Figure 9 shows this for one unit.

4.2 System Issues

System considerations such as stability, calibration, clock distribution, and readout are paramount, as a complete system for a large collider detector would have ∼10,000 channels. Figure 10 shows the top-level diagram (in the CAD framework) of the TOF system electronics for the CDF detector (we have taken this only as a concrete example, as we know the environment and electronics installation of CDF exceedingly well).

4.3 Two TDC Design Alternatives

We are considering two designs for the TDC chip. Figure 11 shows the block diagram of a ‘time-expander’ front end for the TDC. Figure 12 shows the associated control block. An

Figure 8: A test in which epoxy was deposited under machine control at the juncture of four of the Burle anode pads (in this case the mating board was glass, so we could see how we did [25].

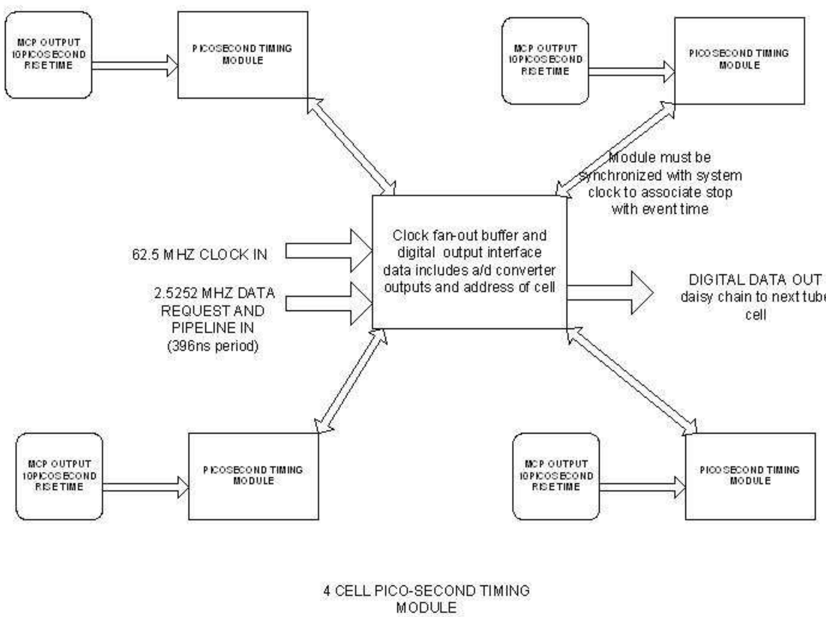

Figure 9: The layout on the back of a single MCP-PMT unit of the 4 TDC chips and the Clock/DAQ chip that multiplies up the frequency of the system clock and distributes it, and that handles the slow-control and DAQ.

alternative front-end, a time-to-voltage converter, is shown in Figure 13 (the control block is similar- we omit the figure for lack of space).

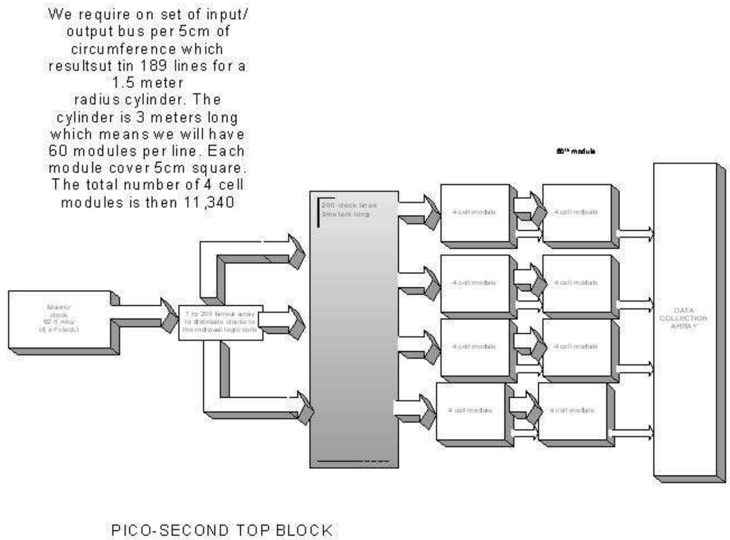

Figure 10: The top-level diagram (in the CAD framework) of the TOF system electronics for the CDF detector (as a concrete example system).

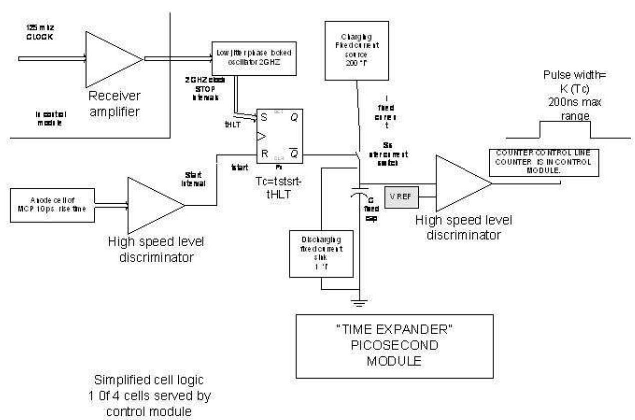

Figure 11: The block diagram of a 'time-expander' front end for the TDC.

4.4 TDC Chip Design Simulation in the IHP Process

The custom chips will be made using a new SiGe process with sub-picosecond precision and new design tools. We have renewed of our MOSIS agreement, which allows us access to the IBM foundry, and have made an agreement for access with IHP MicroElectronics through the Europractice program. One of us (Tang) recently attended a course in the design tools for the IHP process; these tools are now installed and are being used here at UC to design and simulate the performance.

Figure 14 shows the signal from the detector/anode simulation on the collection pin; this is taken as the input to the TDC chip.

Figure 15 shows the time-to-amplitude conversion (TAC) circuit as implemented in the IHP 0.25-micron BiCMOS simulation package.

Figure 16 shows the zero-crossing voltage comparator as implemented in the IHP 0.25-micron BiCMOS simulation package.

Figure 17 shows the bipolar time stretcher, again as implemented in the IHP 0.25-

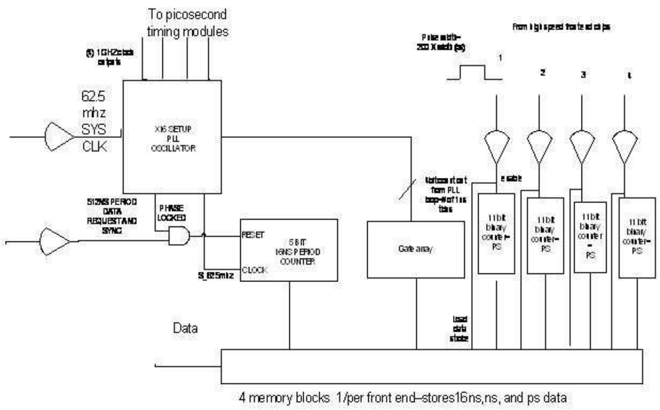

Figure 12: The control block for the 'time-expander' version of the TDC.

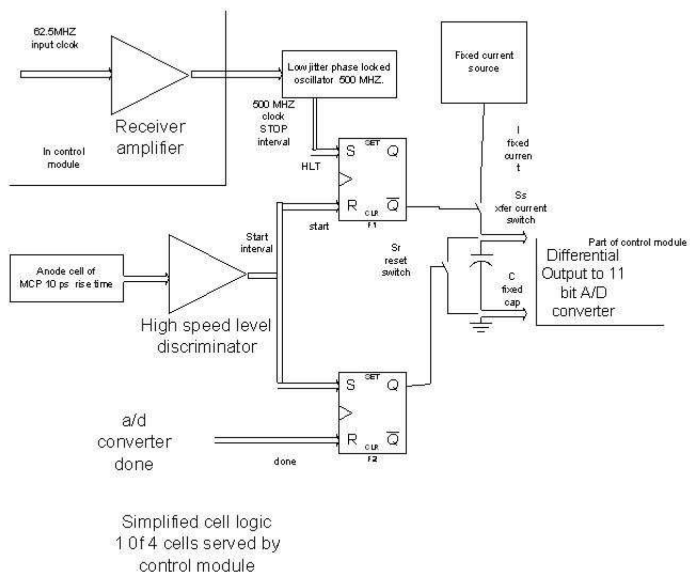

Figure 13: An alternative TDC front-end, a time-to-voltage converter.

micron BiCMOS simulation package.

The IHP simulation package allows us to take the input signal of Figure 14 and put it through the TAC circuit. Figure 18 shows the output for input displaced in successive steps of one picosecond. If it works this well we will be overjoyed.

5 Caveats and Concerns

This is not going to be easy. We have in many ways just begun. Some of our concerns at the outset we have shown or learned will not be a problem: we have simulated interactions in the coil in the geometry in which the detector is outside of the coil, and it looks to be not a problem. The Nagoya group has shown that the pulse from the primary particle traversing the MCP-PMT is negligible [22]; we were concerned about superposing the pulse from the photoelectrons on top of a shifting baseline. We have gone from being more-than-

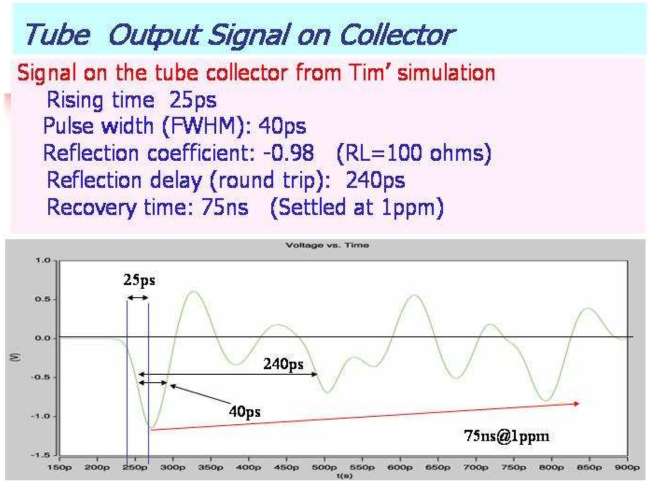

Figure 14: The signal from the detector/anode simulation on the collection pin.

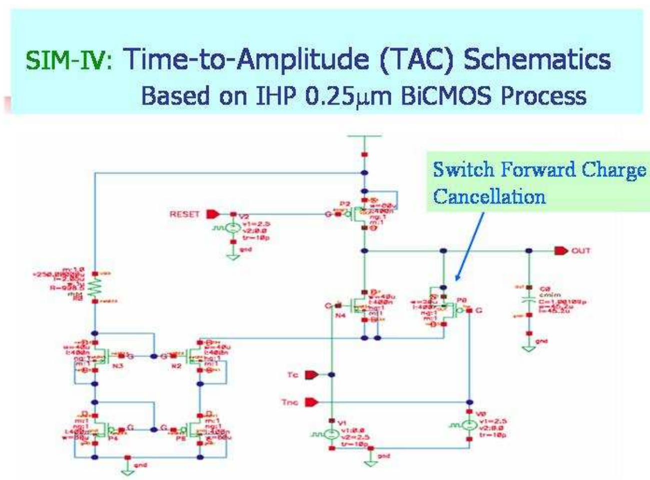

Figure 15: The time-to-amplitude conversion (TAC) circuit as implemented in the IHP 0.25-micron BiCMOS simulation package.

dubious about being able to build circuits with sub-picosecond resolution to having simulated 'working' designs. But this is a new domain in which we have as yet no hands-on experience.

6 Budget Narrative

In this section we describe the separate activities and costs for the development.

6.1 TDC Chip Prototype

A key component in the development of picosecond timing is the custom TDC chip, one of which will sit directly on each of the 4 output pins of the equal-time collector PC card on the back of the MCP-PMT unit. This chip will be submitted to the IHP MicroElectronics foundry through the Europractice program, analogous to the MOSIS program we have used

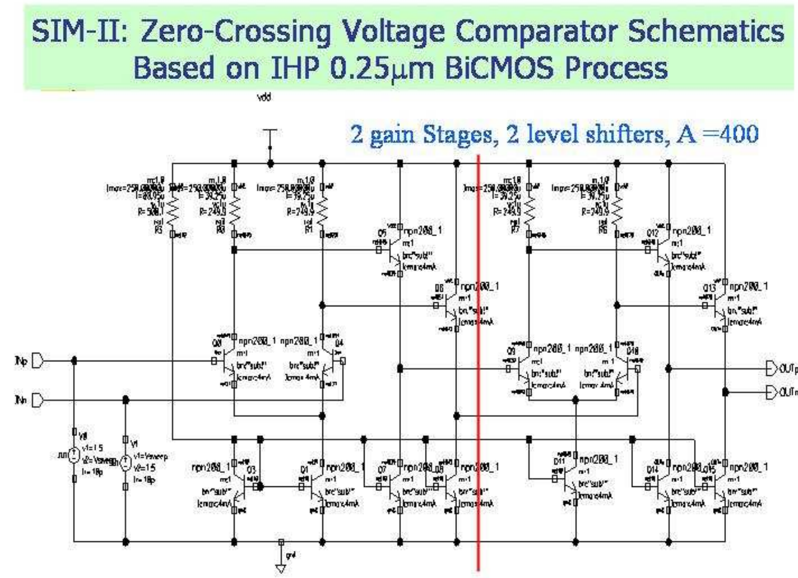

Figure 16: The zero-crossing voltage comparator as implemented in the IHP 0.25-micron BiCMOS simulation package.

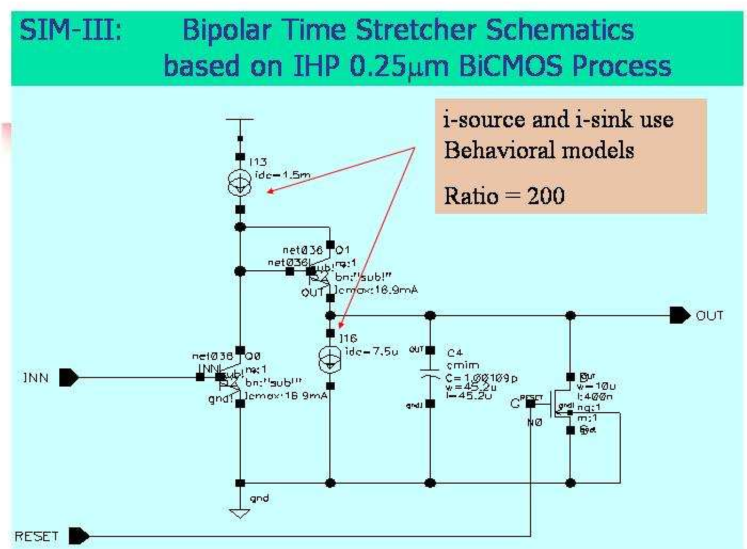

Figure 17: The bipolar time stretcher, implemented in the IHP 0.25-micron BiCMOS simulation package.

in the past. A new and *very* attractive option is that the foundry can also do testing of the chip; with this option, supplemented by a comprehensive circuit simulation, we strongly hope that we will be able to avoid building up the expensive and quickly obsolescent infrastructure used in the past to test and debug custom chips by having the foundry do the testing of the chip functionality. We have budgeted for one submission (i.e. one cycle of design, submission, and testing) in the first year. We estimate that the submission itself will cost \$15K; the cost of the testing cannot be known until we have submitted an actual design, but we have estimated that the total including testing will be covered by \$25K.

In the second year we would make a second submission. We have used the same estimate of \$25K for the sum of production plus testing.

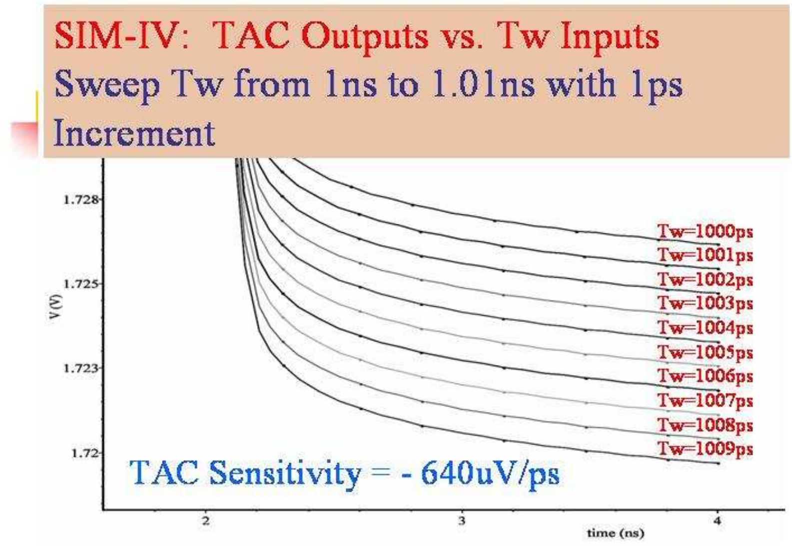

Figure 18: The output of the simulation in the IHP 0.25 μm BiCMOS process of the time-to-amplitude circuit for inputs successively displaced by one picosecond. The difference in output voltage for a 1-psec time displacement is 0.64 mV, which is quite measurable.

6.2 Clock/DAQ Chip Slow Prototype

The second custom chip on the equal-time collector PC card attached to the back of the MCP-PMT unit is the Clock/DAQ Chip. This chip takes the lower-frequency system clock and multiplies it up, and also handles the readout and slow-control for the 4 TDC chips on the MCP-PMT tile. We will first prototype the functionality of this chip at much lower speeds in an Altera FPGA, so that we can debug the functionality in an environment with well-understood tools. We have extensive experience and success in this format [24, 26, 27], and have shown that we can fully simulate the behavior of a complex chip. Once we have the functionality well-debugged, we can then move to the problem of implementing the same functionality, but at full speed, in a custom IC. Again, we would use the IHP MicroElectronics foundry through Europractice, and rely on contracting out the initial testing to them. We have started an excellent fourth-year undergraduate, Jakob Van Santen, on the Altera software with the goal of having an initial layout by the end of the year. We are requesting $8K for the parts and construction of the small PC card to support the FPGA prototype of the Clock/DAQ chip.

In the second year we will transfer the functionality tested at a slower speed in the Altera FPGA to the design tools for the IHP chip production process. We have asked for funds in this year for a submission of the custom chip to the foundry. We again use the estimate of $25K for production, including testing. As with the TDC chip, the actual cost of testing cannot be priced until the actual design is submitted, but we will have experience at this point from the previous year.

6.3 Interface Board

Testing the TDC chip will require the ability to input and output signals, supply power, etc. These functions require building a small PC card that will interface between the chip and the computer that will control the testing. We estimate this card will require two passes at

$2K each plus $4K parts to get what we want, and so have put $8K in the budget for parts and construction.

6.4 CAD/Sim Software

We depend on our sophisticated system of computer-aided design and simulation software, which is comprised of several packages from several vendors. We use this software to train our students in design in the process of making electronics for our experiments; the layout of the equal-time collection board that mates to the Burle anode has been done entirely by a young student, Timothy Credo, who has recently graduated from IMSA (Illinois Math and Science Academy), and who will enter college next year [28, 29]. The FPGA prototype board for the Clock/DAQ chip is being laid-out by a fourth-year undergraduate. We hope to entice an incoming graduate student to work on the chip layout.

We have asked for $5K for licenses for new packages and updates for software, as the typical cost to a university licensee is $2-3K per license, and typically we need 1-2 per year [30].

6.5 Testing and Instrumentation

We plan the tests at design resolution to be with a test beam at Fermilab using three [31] of the MCP-PMT units with the equal-time mating cards and the on-board TDC's.

6.6 Personnel

We have requested support for 15 weeks of engineering time for Fukun Tang.

The Electronics Development Group (EDG, or 'Eshop') of the Enrico Fermi Institute is a service group to the multidisciplinary Institute faculty, students, and staff. The EDG charges $71 per hour for Tang's time; the rate includes overhead, computer system support, administrative and stockroom support. The rate is this low due to substantial subsidy by the University. Harold Sander's time will be paid for by the University as an additional, major, subsidy. Additional engineering time will be supported by the 'blanket' NSF grant that supports multiple efforts in HEP.

We request $10K for support of a graduate student for one quarter. The expense covers the standard stipend plus tuition. Previous PhD students who have worked with Frisch on electronics and have gone on to be hardware-expert in their careers include Joseph Incandela (now Prof., UCSB), Sacha Kopp (Asst. Prof., UT Austin), David Saltzberg (Assoc. Prof., UCLA), and Sunil Somalwar (Prof. Rutgers), among others.

Two undergraduates are working for us now: Tim Credo (technically not yet an undergraduate, as he has not yet entered college) started as an IMSA intern with us two summers ago. He delayed entry to Harvard by a year, and has continued with us on this project. A third-year student, Shreyas Bhat, has been simulating the interaction of particles in material ahead of the MCP (for example, if the TOF system were mounted outside of a solenoid coil in a collider detector such as CDF or at a Super-B factory or linear collider.). A third undergraduate, unpaid, is doing his Senior Thesis on the FPGA design. We ask for support for one undergraduate, who will replace Tim when he goes to college.

For the second year we have multiplied the first year costs by 1.03 for inflation.

6.7 Travel

Fukun Tang, from the Electronics Development group, took a course on the IHP MicroElectronics design tool package in Brussels, Belgium in October, 2005. We have budgeted one such training trip for the coming year as there will be new tools introduced. We have also budgeted one trip to an IEEE conference for an engineer to present recent results from this work. Tim Credo, still a high school student, presented his work on the equal-time anode at the Rome IEEE conference last year. We have budgeted a domestic trip for a student to present their work. We have also budgeted $1K for transportation,housing and subsistence for a student working at Fermilab during the beam test.

7 Budget Summary

We summarize the budget requests, not including overhead, in three tables below- one for each year, and a summary.

7.1 Year 1

The budget request for year 1 is shown in Table 1.

Budget Request Year 1				
Category	Item	Unit Cost	Total Line	Total Category
Interface Board				8K
	2 submissions, Parts	—	8K	
TDC Chip Prototype				25K
	1 Submission	15K	15K	
	Testing	10K	10K	
DAQ Chip Prototype				8K
	FPGA Prototype Parts	3K	3K	
	FPGA PC test card	5K	5K	
CAD/Sim Software				5K
	1 Module License	5K	5K	
Instrumentation				5K
	Pulse Generator	2K		
	Misc	3K		
Personnel				59,740
	1/4 Grad Student	40K	10K	
	1 Undergrads(+summer)	7,140	7,140	
	Engineering (15 wks)	2,840	42,600K	
Travel				6K
	Engineer: Conference	2K		
	Engineer: Training	2K		
	Student: Conference	1K		
	Student: Beam Test	1K		
Total				$116,740

Table 1: Year 1 Budget Request

7.2 Year 2

The budget request for year 2 is shown in Table 2.

Budget Request Year 2				
Category	Item	Unit Cost	Total Line	Total Category
Interface Board				0K
TDC Chip Prototype				25K
DAQ Chip Prototype				25K
	1 Submission	15K	15K	
	Testing	10K	10K	
CAD/Sim Software				5K
	1 Module License	5K	5K	
Instrumentation				3K
	Misc	3K		
Personnel				61,153
	1/4 Grad Student	40K	10,300	
	1 Undergrads(+summer)	7,354	7,354	
	Engineering (15 wks)	2,925	43,878K	
Travel				6K
	Engineer: Conference	2K		
	Engineer: Training	2K		
	Student: Conference	1K		
	Student: Beam Test	1K		
Total				$125,153

Table 2: Year 2 Budget Request

7.3 Total: Years 1+2

The total budget request for years 1 and 2 together is shown in Table 3.

Total Budget Request: Years 1+2			
Category	Year 1	Year 2	Total Category
Interface Board	8K	0K	8K
TDC Chip Prototypes	25K	25K	50K
DAQ Chip Prototypes	8K	25K	33K
CAD/Sim Software	5K	5K	10K
Instrumentation	5K	3K	8K
Personnel	59,740	61,153	120,893
Travel	6K	6K	12K
Total			$241,893

Table 3: Years 1+2 Total Budget Request

8 Acknowledgments

The initial detailed simulations were done by Robert Schroll, to whom we are very grateful. We thank Paul Hink, Bruce Laprade, Scott Moulzolf, and Wilma Raso, from Burle Industries; and Mario Kasahara, from Hamamatsu Corporation, for their assistance on the properties of MCP PMTs. We also thank Alan Bross, Kastsushi Arisaka and Jaroslav Va'vra for useful discussions and guidance. We owe great thanks to Greg Sellberg for his ingenuity and skill in solving the problem of how to mate the equal-time PC board to the MCP-PMT anode.

References

[1] No funds are requested in this proposal for the Argonne collaborators; the work for which support is requested here will be done at the University of Chicago with the exception of the (small) request for travel support for a UC student to help with beam testing, which will be done at Fermilab.

[2] For a description of the Tevatron, see http://www.fnal.gov/

[3] For a description of the Large Hadron Colliders (LHC) at CERN, see http://lhc-new-homepage.web.cern.ch/lhc-new-homepage/.

[4] For a description of the International Linear Collider (ILC), see: http://physics.uoregon.edu/ lc/randd.html.

[5] H. Frisch, *Visions of Experimental Particle Physics– Where Are We Going?*, Aspen Winter Conference, Aspen Co., Jan. 26, 2003 (http: hep.uchicago.edu: frisch).

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[11] The IBM silicon germanium technology is described at: http://www.physorg.com/news5660.html

[12] For a description of the CDF, see: http://www-cdf.fnal.gov/.

[13] For a description of HEP plans for a future super B-factory, see http://www.phys.hawaii.edu/superb/

[14] http://www.kek.jp/intra-e/

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[19] A.Bross, private communication

[20] K.Arisaka, private communication.

[21] M.Akatsu, et al., Nucl.Instrum.Meth. A528:763-775,2004

[22] At the workshop (http://hep.uchicago.edu/workshops/2005-picosecond/) we held November 18 T. Ohshima reported on results from a setup very similar to that we had proposed. The Nagoya group has now achieved a 4.7 psec resolution. We are discussing collaborating, in particular making the electronics developments proposed here available to them if we are successful.

[23] U. Frankenfeld *et al.* [ALICE/PesTOF Collaboration], *Investigation of new gas mixtures for the Pestov counter*; GSI reprintGSI-98-22; March, 1998

[24] M. Bogdan, H, Frisch, M. Heintz, A. Paramonov, H. Sanders, et al. *A 96-Channel FPGA-based Time-to-Digital Converter* Nucl.Instrum.Meth. A554 (2005) 444-457, and arXiv: physics/0502062

[25] We are indebted to Greg Sellberg for this technique and the test.

[26] B. Ashmanskas, M. Bogdan, T. Liu, H. Sanders et al.; *CDF Level 2 Trigger Upgrade: the Pulsar Project*; Proceedings of the 10th Workshop on Electronics for LHC and Future Experiments, Boston 2004

[27] K. Anikeev, M. Bogdan, R. Demaat, W. Fedorko, H. Frisch, et al.; Submitted to IEEE, Nov. 2004; available at:
http://hep.uchicago.edu/ thliu/projects/Pulsar/Pulsar_doc/Pulsar_IEEE_submit

[28] Tim took his work on the simulation and design of the equal-time anode to the national Intel Science Talent search, where he took 2nd place. Tim also presented his work at the IEEE, Rome, Italy, Oct. 2004 [29]. Detector development work is a wonderful pedagogic experience in addition to its intrinsic merit.

[29] T. Credo, H. Frisch, H. Sanders, R. Schroll, and F. Tang; *Picosecond Time-of-Flight Measurement for Colliders Using Cherenkov Light*; proceedings of the IEEE, Rome, Italy, Oct. 2004.

[30] The cost if we did not use these for teaching would be prohibitively high. We are really appreciative of the subsidy provided by the vendors, and very proud of the electronics skills of the students who have gone on to use their skills as faculty at other institutions.

[31] We plan to use three units so to get two velocity measurements as for these devices, if they work, the assumption that all relativistic muons are traveling at $v = c$ is no longer valid and so one needs more than one velocity measurement.