Design of an 8-Channel 40 GS/s 20 mW/Ch Waveform Sampling ASIC in 65 nm CMOS

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Abstract

1 ps timing resolution is the entry point to signature based searches relying on secondary/tertiary vertices and particle identification. We describe PSEC5, an 8-channel 40 GS/s waveform-sampling ASIC in the TSMC 65 nm process targetting 1 ps resolution at 20 mW power per channel. Each channel consists of four fast and one slow switched capacitor arrays (SCA), allowing ps time resolution combined with a long effective buffer. Each fast SCA is 1.6 ns long and has a nominal sampling rate of 40 GS/s. The slow SCA is 204.8 ns long and samples at 5 GS/s. Recording of the analog data for each channel is triggered by a fast discriminator capable of multiple triggering during the window of the slow SCA. To achieve a large dynamic range, low leakage, and high bandwidth, the SCA sampling switches are implemented as 2.5 V nMOSFETs controlled by 1.2 V shift registers. Stored analog data are digitized by an external ADC at 10 bits or better.

Specifications on operational parameters include a 4 GHz analog bandwidth and a dead time of 20 microseconds, corresponding to a 50 kHz readout rate, determined by the choice of the external ADC. PSEC5 has been submitted for fabrication.

Keywords:

Digital Design and Implementation for the PSEC5 40 GS/s waveform-sampling ASIC

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Abstract

We have designed PSEC5, a mixed-signal waveform-sampling ASIC targeting 1 ps timing resolution, 200 ns buffer length, and multi-hit capability. PSEC5 has digital control for readout and sampling, which has been implemented using SPI. The digital blocks were written in System Verilog, a hardware description language. The System Verilog codes were then synthesized into Register-Transfer Level (RTL) and implemented using Cadence Genus and Innovus. In this talk, we will walk through the procedure for designing, implementing, and verifying digital ASICs.

A Modular Test System for the PSEC5 40 GS/s waveform-sampling ASIC

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Abstract

We have recently submitted for fabrication PSEC5, an 8-channel mixed-signal waveform-sampling ASIC targeting 1 ps timing resolution, 200 ns buffer length, and multi-hit capability. Here, we describe the architecture and development process of a modular test system for PSEC5. The system consists of two PCBs: a Design Under Test (DUT) Board, and a Control Board. The Control Board is based on the Kria K26 FPGA module. The DUT Board contains PSEC5. The boards are being designed in KiCad; the FPGA firmware is being written in Vivado. The system has been designed by a team of undergraduates with guidance from experts.

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The Role of Young University Undergraduates Guided by National Lab Experts, in the Design of PSEC5, a 40 GS/sec 4GHz 8-Channel Mixed-Signal ASIC

Advanced ASIC design requires specialized knowledge and skills rarely found in undergraduates. In the PSEC5 project, undergraduates led the design of a 40 GS/s 4GHz 8-channel waveform sampling ASIC targeting 1-ps resolution. The project required precision analog and custom digital design, and RTL design using Verilog and System Verilog, the pathfinder's design has been sent for fabrication, and we are currently developing an FPGA-based system for chip testing. Remarkably, most of the project was accomplished by a university/national lab collaboration comprising four undergraduates guided by several experts at Fermilab through regular weekly Zoom meetings. The students had no prior experience in circuit design beyond a first-year electro-magnetism course. In addition to the benefit of the students, the difference in cost/hour for undergrad versus a top ASIC engineer shifts the optimum of simulation vs testing and multiple submissions as student time is so cheap and they can `simulate the heck out of it,' while getting an education unavailable in an electronics course.