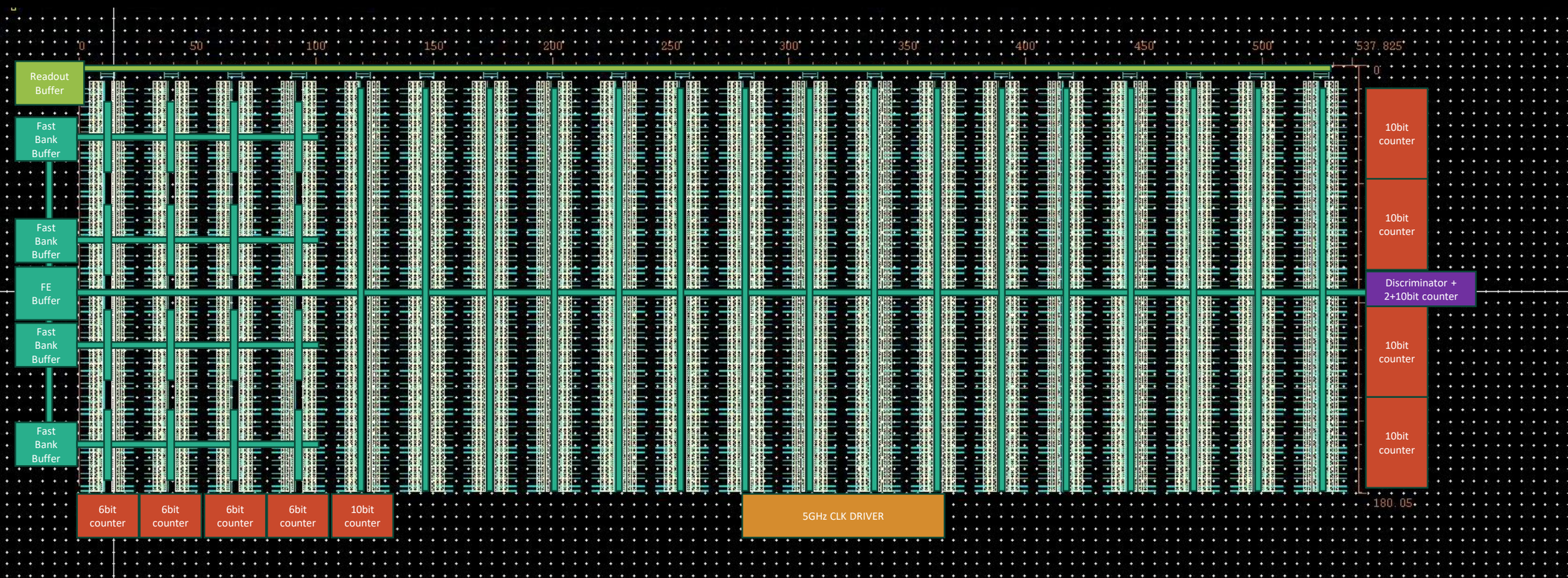
PSEC5 Layout

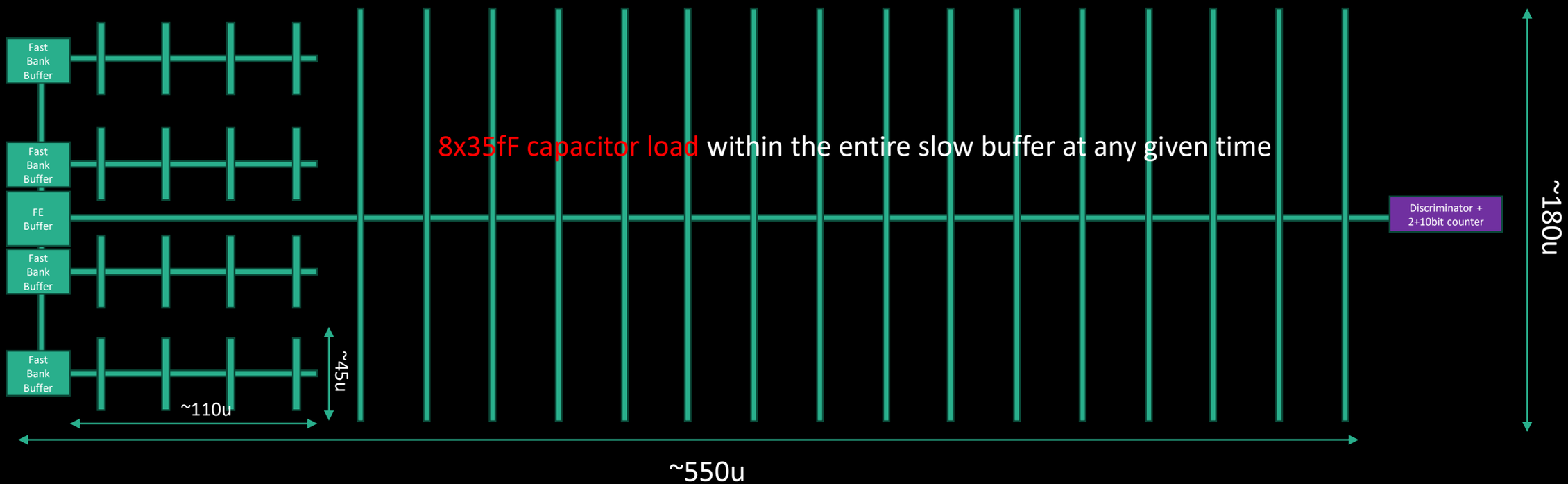
Dec 2023

Single Channel Overview



Signal Transmission

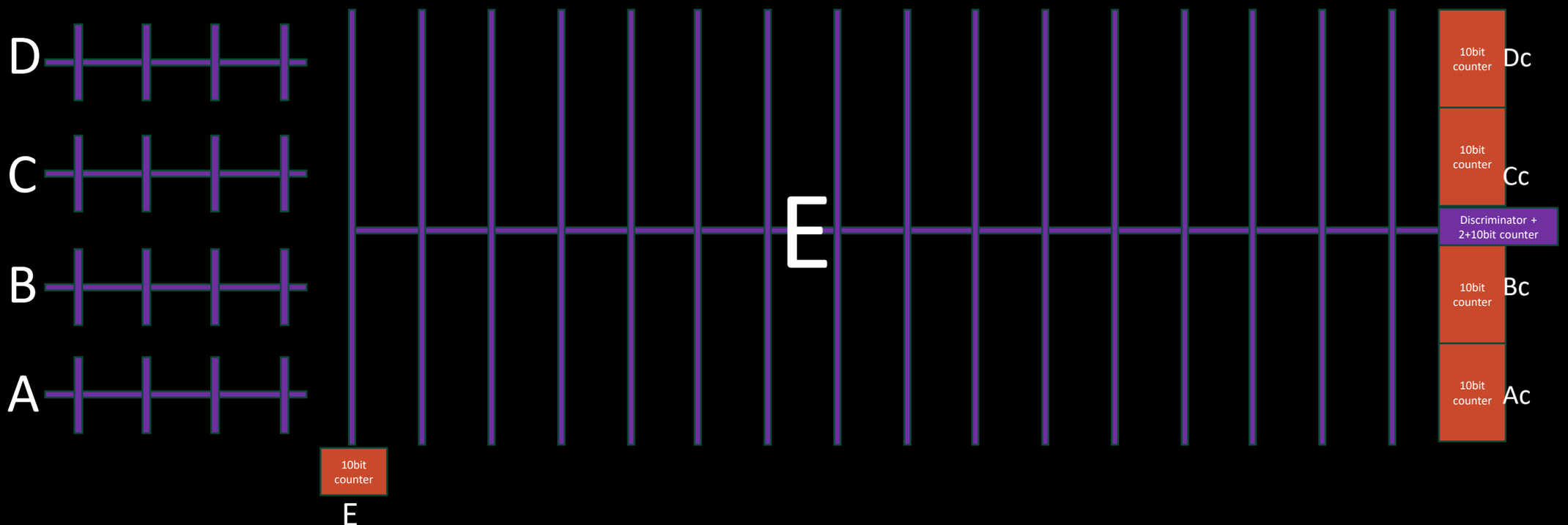
32x35fF capacitor load per fast bank buffer when the corresponding fast bank is running



Layer: M6. Trace width: 2u
Rs: 0.14 Ohm/Sq
C: 2e-2 fF per 1u trace length

Trigger Scheme

0: sampling and counting. 1: holding and not counting.



States and Trigger Scheme

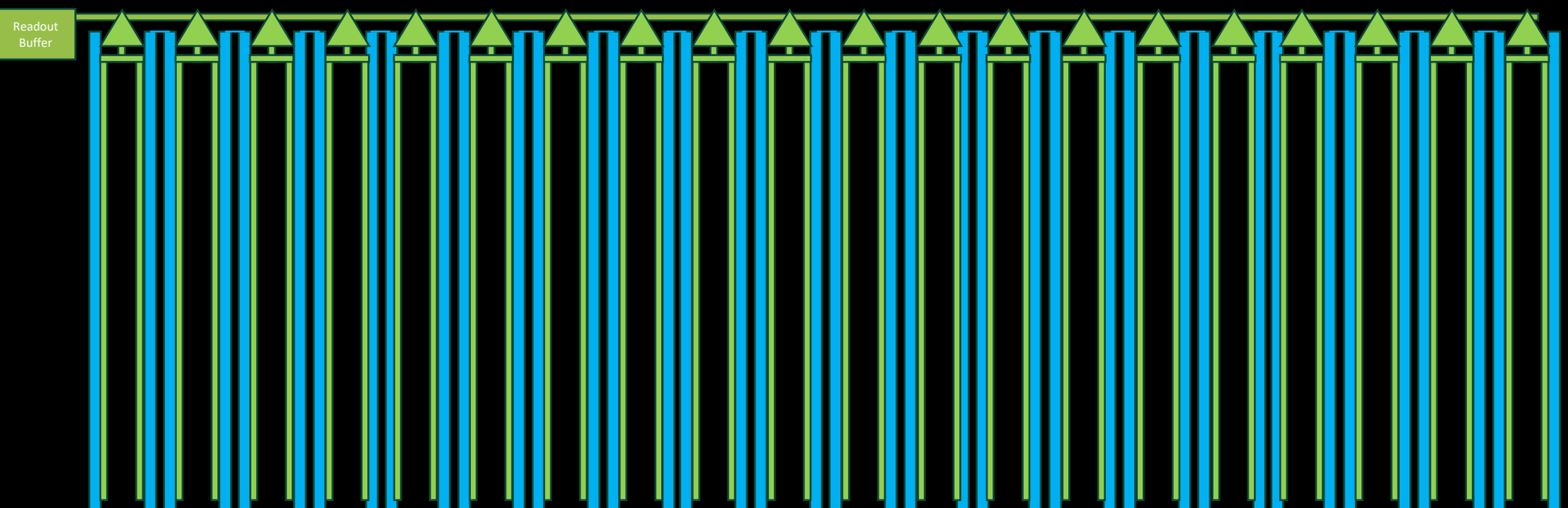
States	A	Ac	B	Bc	C	Cc	D	Dc	E
stopped	1	1	1	1	1	1	1	1	1
samplingA	0	0	1	0	1	0	1	0	0
samplingB	1	1	0	0	1	0	1	0	0
samplingC	1	1	1	1	0	0	1	0	0
samplingD	1	1	1	1	1	1	0	0	0
samplingE	1	1	1	1	1	1	1	1	0
samplingA+B	0	0	0	0	1	0	1	0	0
samplingC+D	1	1	1	1	0	0	0	0	0
samplingA+B+C+D	0	0	0	0	0	0	0	0	0

Transitions	Conditions
stopped→samplingA	Start command from FPGA
samplingA→samplingB	Discri. Fired for the 1st time
samplingB→samplingC	Discri. Fired for the 2nd time
samplingC→samplingD	Discri. Fired for the 3rd time
samplingD→samplingE	Discri. Fired for the 4th time
samplingB,C,D,E→stopped	Stop command from FPGA

After roughly 800 5GHz clock cycles or 180ns since the discriminator fired for the 1st time, notify the FPGA so that it can issue the stop command

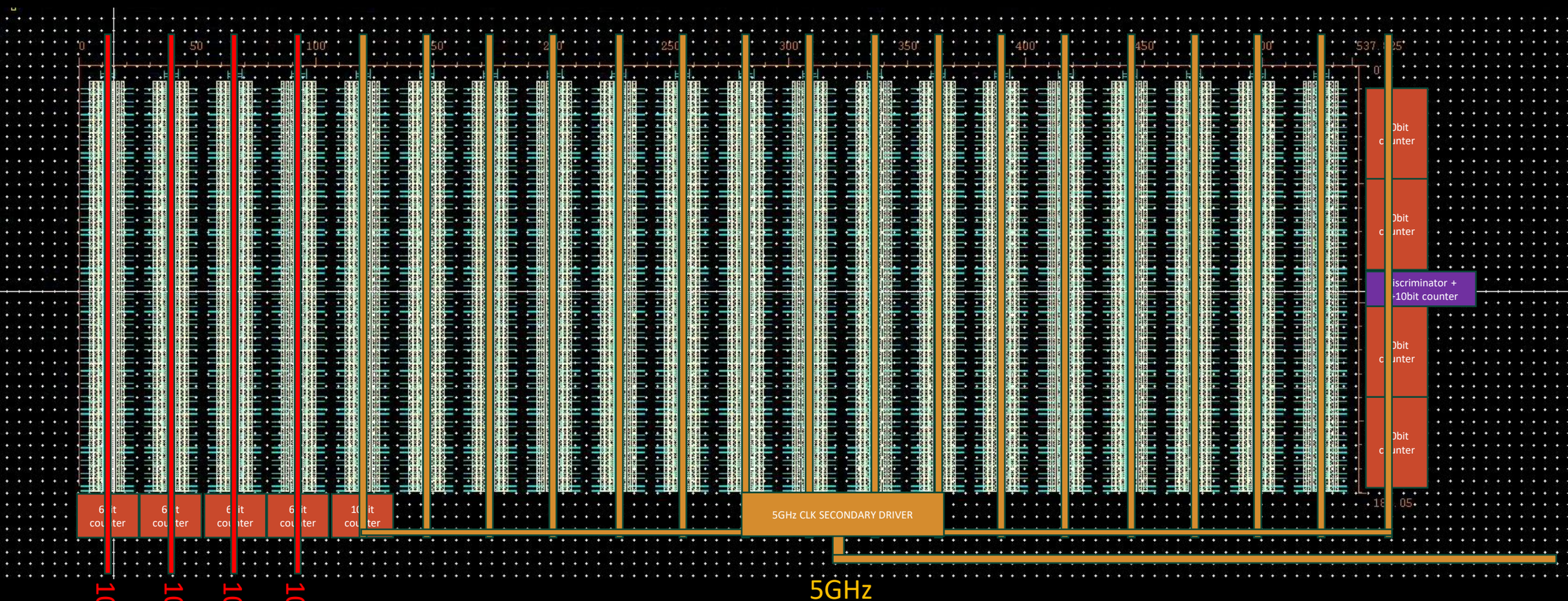
Readout Scheme

There is a voltage follower at each column, 20 in total.



Each thick blue line represents 64 flip-flops running at 50MHz.
Only one flip-flop is high at any given time.

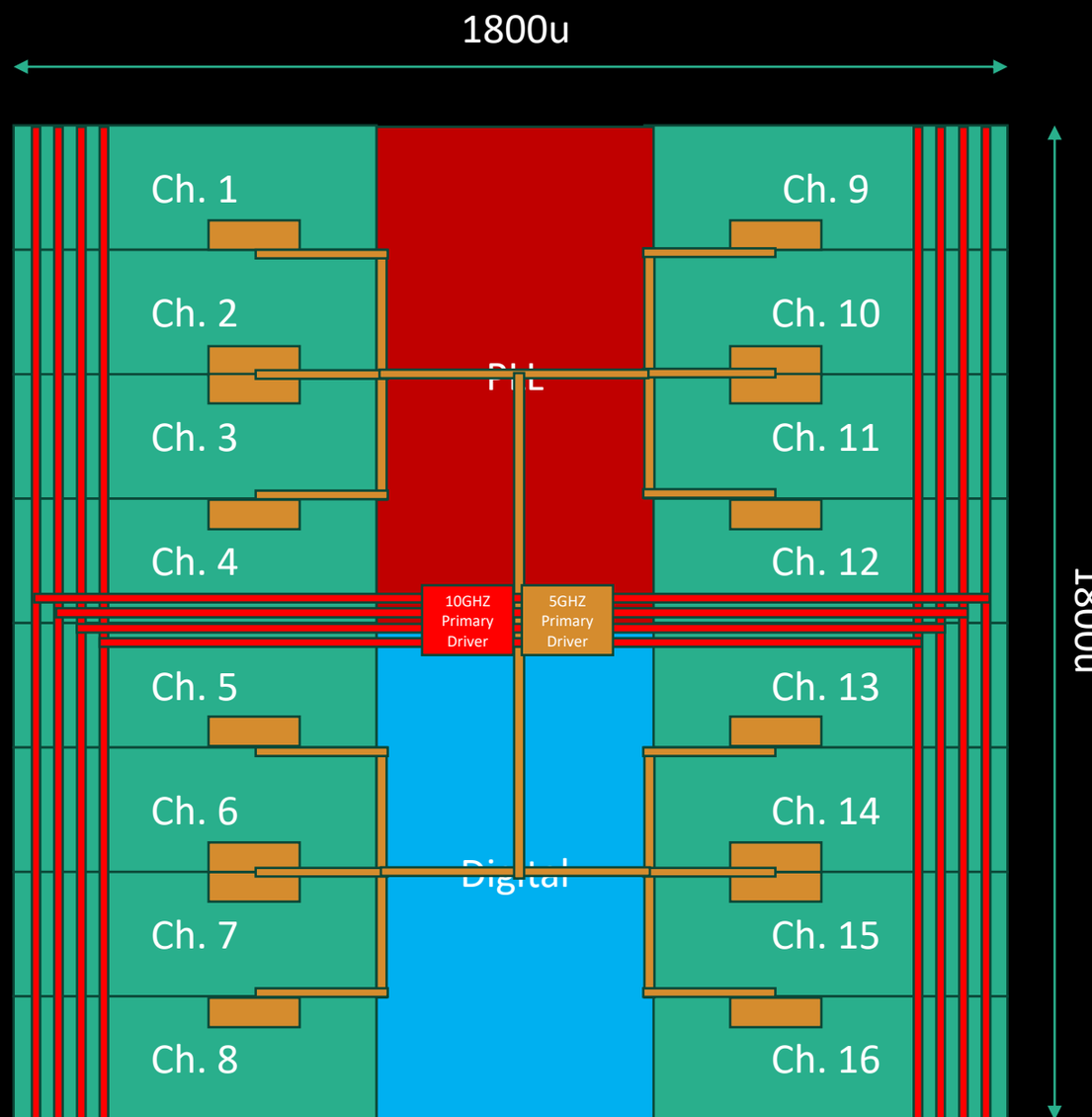
Clock distribution



10GHz CLK does not have a secondary driver in the current design!

25ps ~ 7500u

6ps ~ 1800u



Layer: M9. Trace width: 2u
Rs: 0.04 Ohm/Sq
C: 2e-2 fF per 1u trace length

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Chip Overview(88 pins)