

# Would Psec TOF Be Useful To LHCb?

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## OUTLINE

1. What would you do with it if you had it?
2. How does one get much better time resolution?
3. Some technical details
4. Plan for the future- 3yr development

Apologies for sloppy talk- I finished the big DOE proposal today

# What would TOF<10psec do for you?

■ (disclaimer- I know next to nothing about LHCb, b-physics, or the Collab. goals..- I'm making this up....needs work- would be delighted to see someone pick this up.)

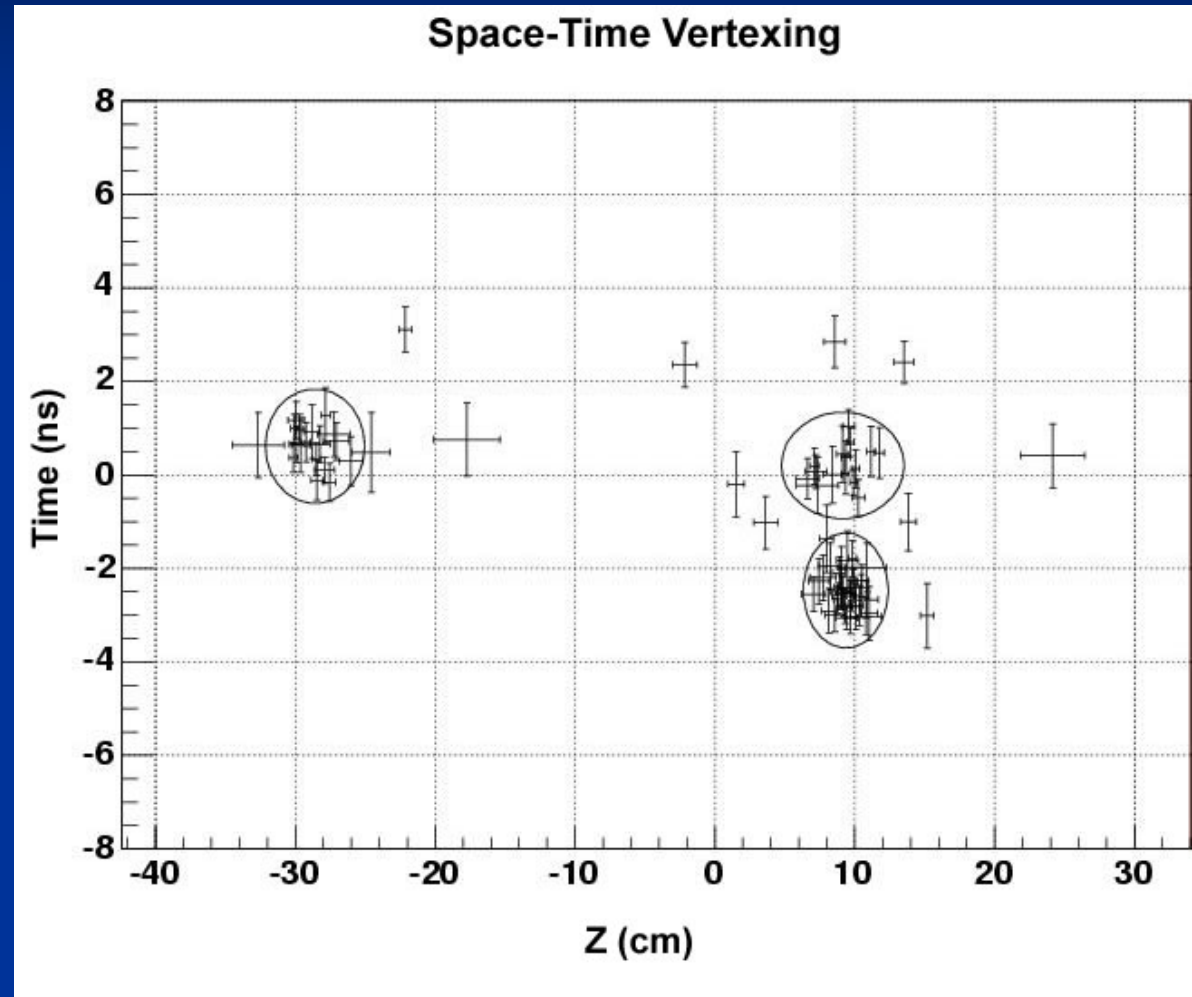
1. If you can stand a little active material in front of your em calorimeter, convert photons- 10 psec is 3mm IN THE DIRECTION of the photon flight path- can vertex photons. **Do pizeros, etas,  $K_L$  and  $K_S$ , ...**
2. This allows **all neutral signature mass reconstruction**- new channels. e.g. **the CP asymmetry in  $BS \rightarrow \pi K^0$**  (J.Rosner suggestion)
3. Eta's in general are nice: e.g.  **$BS \rightarrow J/\psi \eta$**  (again, J.R.)
4. With two planes and time maybe get to 1 psec, =300 microns along flight path- **can one vertex from timing?**
5. Searches for **rare heavy long-lived things** (other than b's)- need redundancy.
6. May help with pileup- **sorting out vertices.**

# Performance Goals

Quantity	Present	Baseline	HJF
Time resolution-charged particles (psec)	12 (6)(2.3*	10	<1
Time resolution-photons (psec)	---	10	1-3
Space resolution- charged (mm)	0.1*	1	0.1
Space resolution- neutrals (mm)	--	5	1-3
Thickness (inches)/plane	1*	2	2
Cost (\$/30 sq-meters/plane)	60M\$	3.0M\$	1.2M\$
Schedule for development (from $t_0$ - i.e. funding of MCP project)	---	3 yrs	5 yrs
* With a 2" square Burle MCP in beam- 6 psec on bench,2.3 expected			
4/16/2009	LHCb Upgrade Meeting		50

# Example of vertexing from CDF

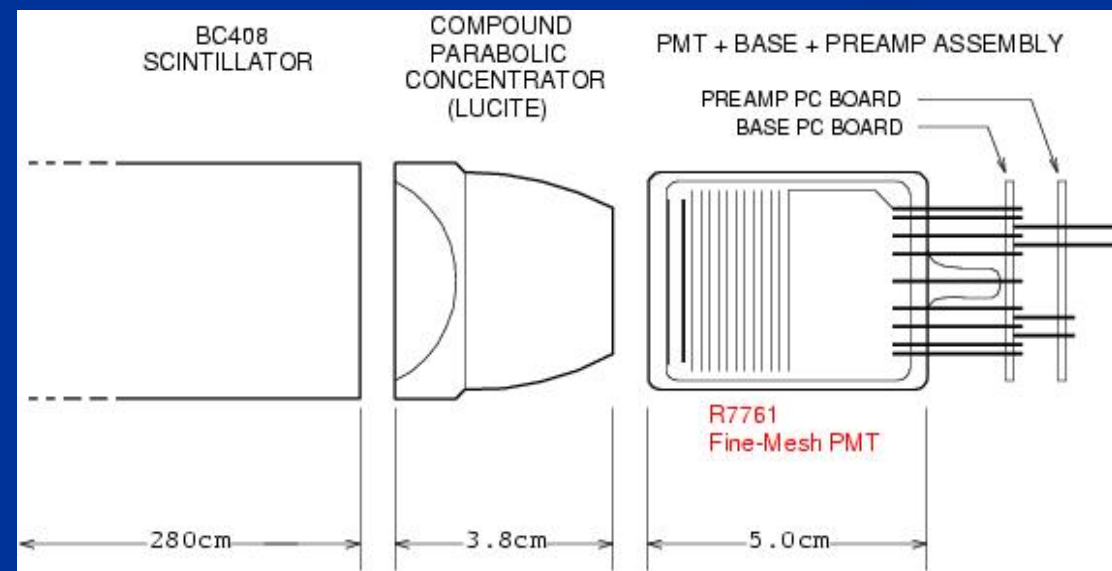
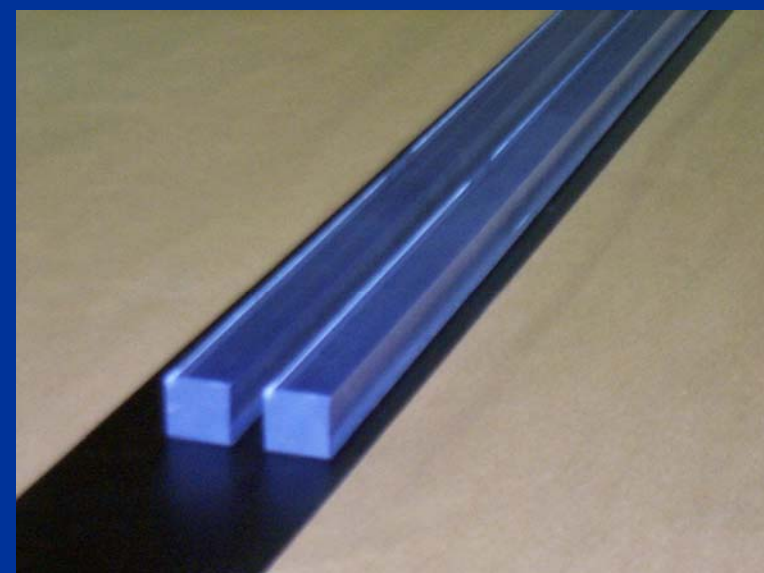
- EM timing (Dave Toback, HJF, et al)
- Vertices overlap in time, and in space, but usually not both
- Resolution is good wrt 7 cm



# Why has 100 psec been the # for 60 yrs?

Typical path lengths for light and electrons are set by physical dimensions of the light collection and amplifying device.

These are now on the order of an inch. One inch is 100 psec  
That's what we measure- no surprise! (pictures from T. Credo)



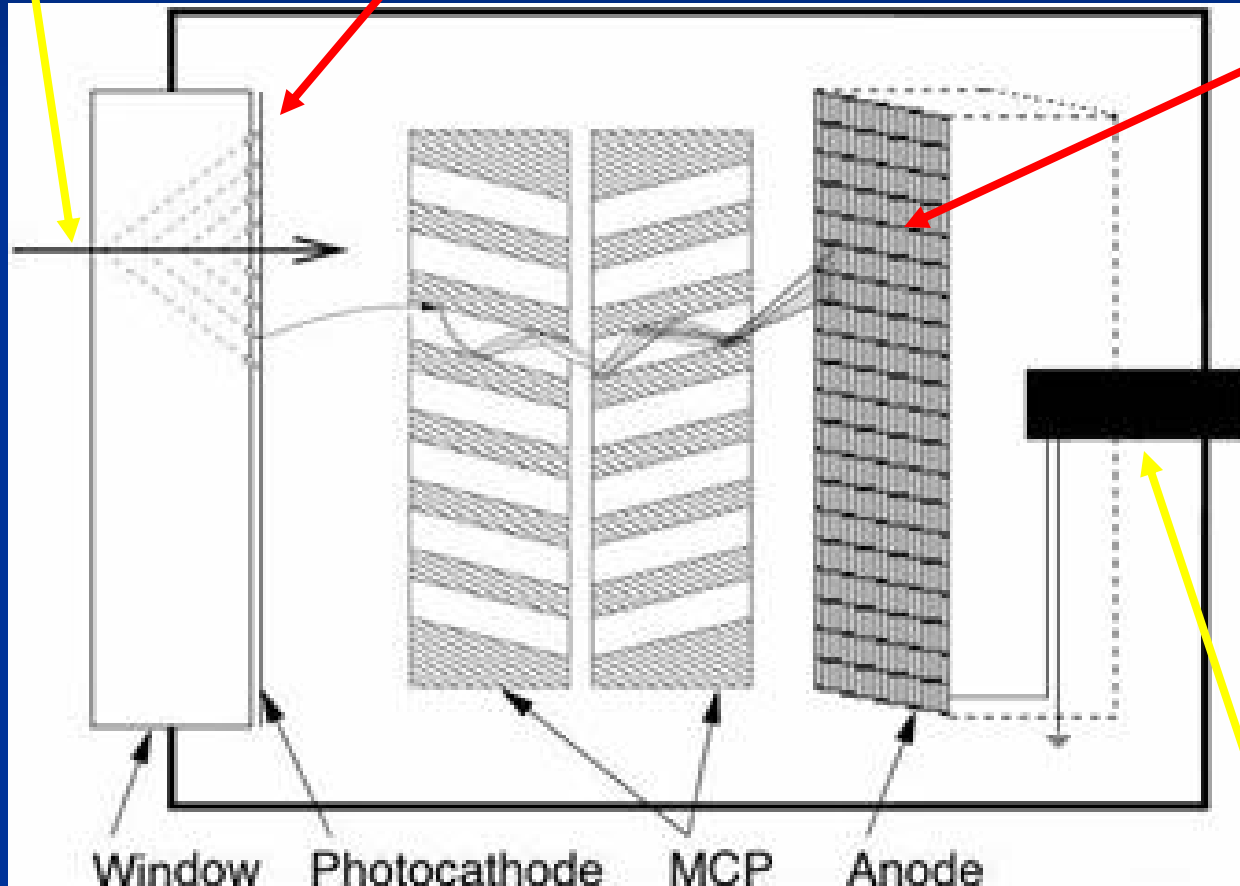
Typical Light Source (With Bounces)

Typical Detection Device (With Long Path Lengths)

# Solutions: Generating the signal

**Use Cherenkov light - fast**

Incoming rel. particle



Custom Anode with  
Equal-Time Transmission  
Lines + Capacitive. Return

A 2" x 2" MCP-  
actual thickness  
~3/4"

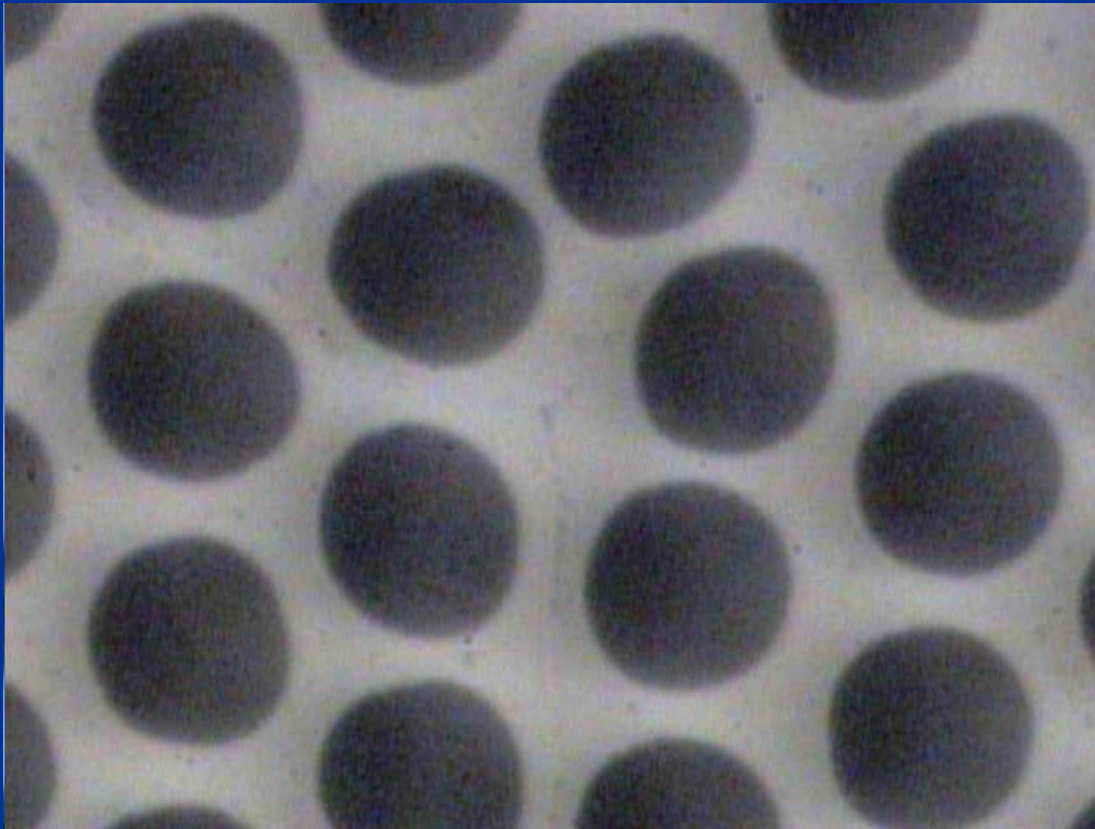
e.g. Burle  
(Photonis) 85022-  
with mods per  
our work



# Micro-channel Plates

Currently the glass substrate has a dual function-

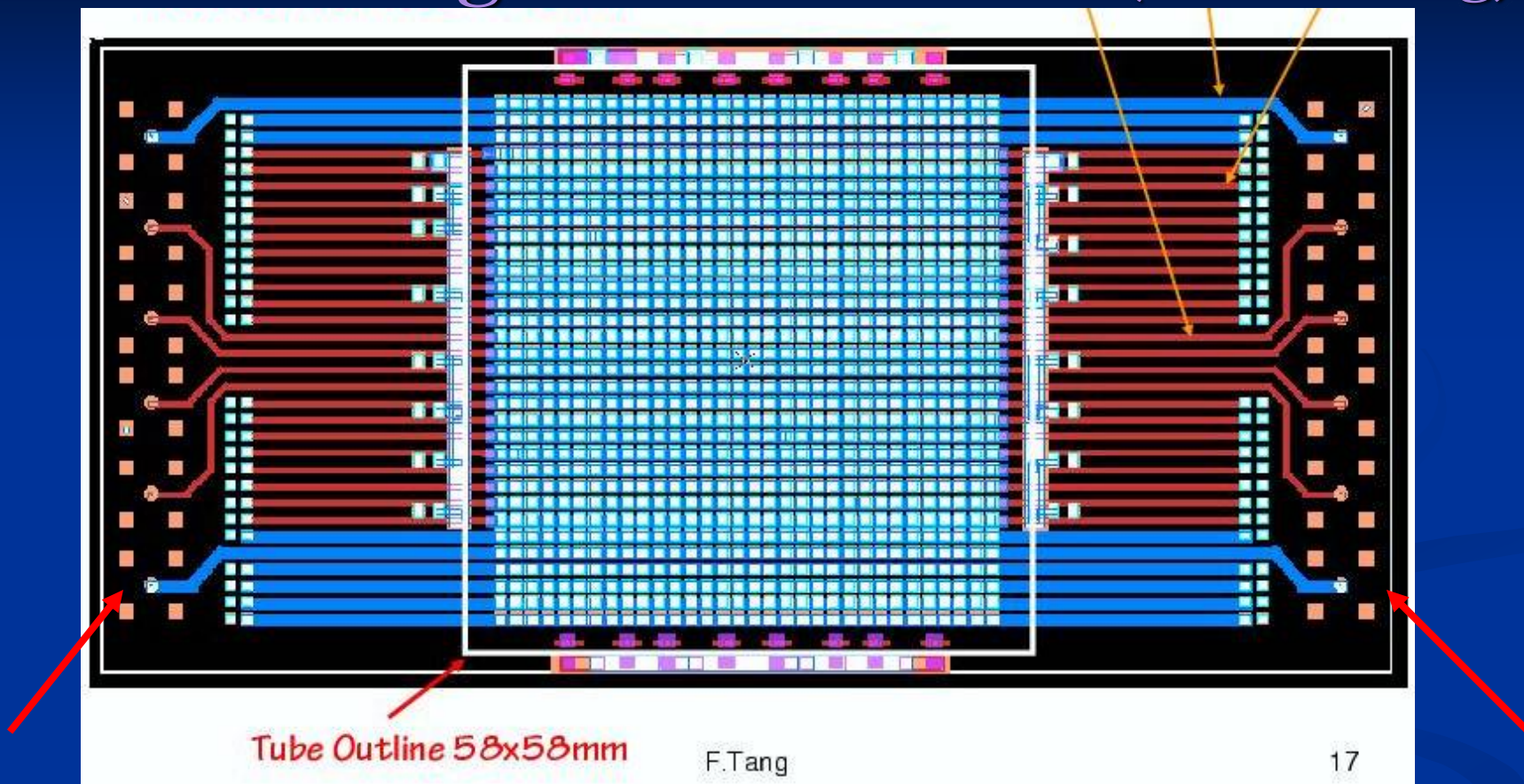
1. To provide the geometry and electric field like the dynode chain in a PMT, and
2. To use an intrinsic lead-oxide layer for secondary electron emission (SEE)



Micro-photograph of  
Burle 25 micron  
tube- Greg Sellberg  
(Fermilab)-  
~2M\$/m<sup>2</sup>- not  
including readout

# Get position AND time

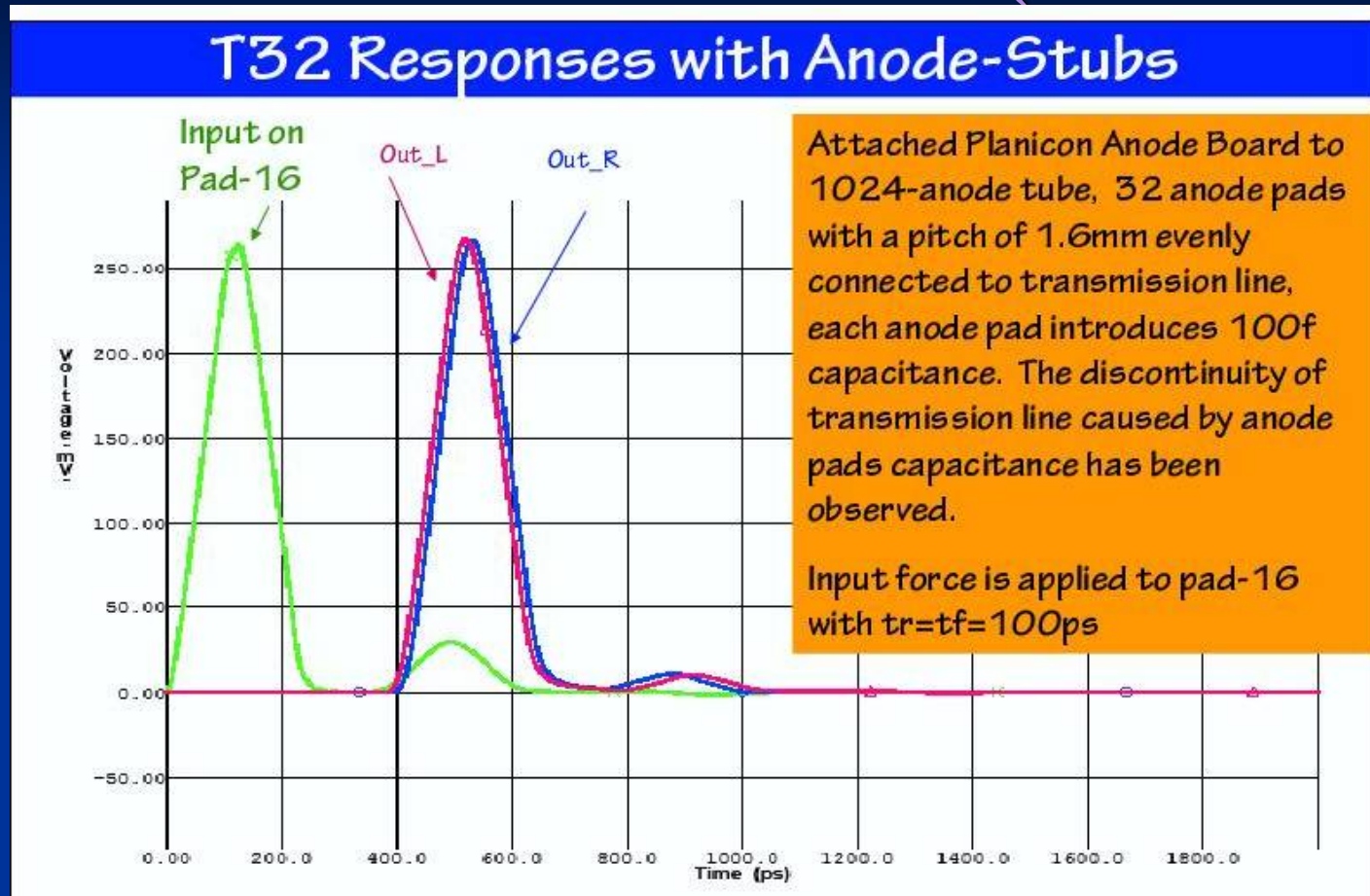
## Anode Design and Simulation(Fukun Tang)



- Transmission Line- readout both ends=> pos and time
- Cover large areas with much reduced channel account.

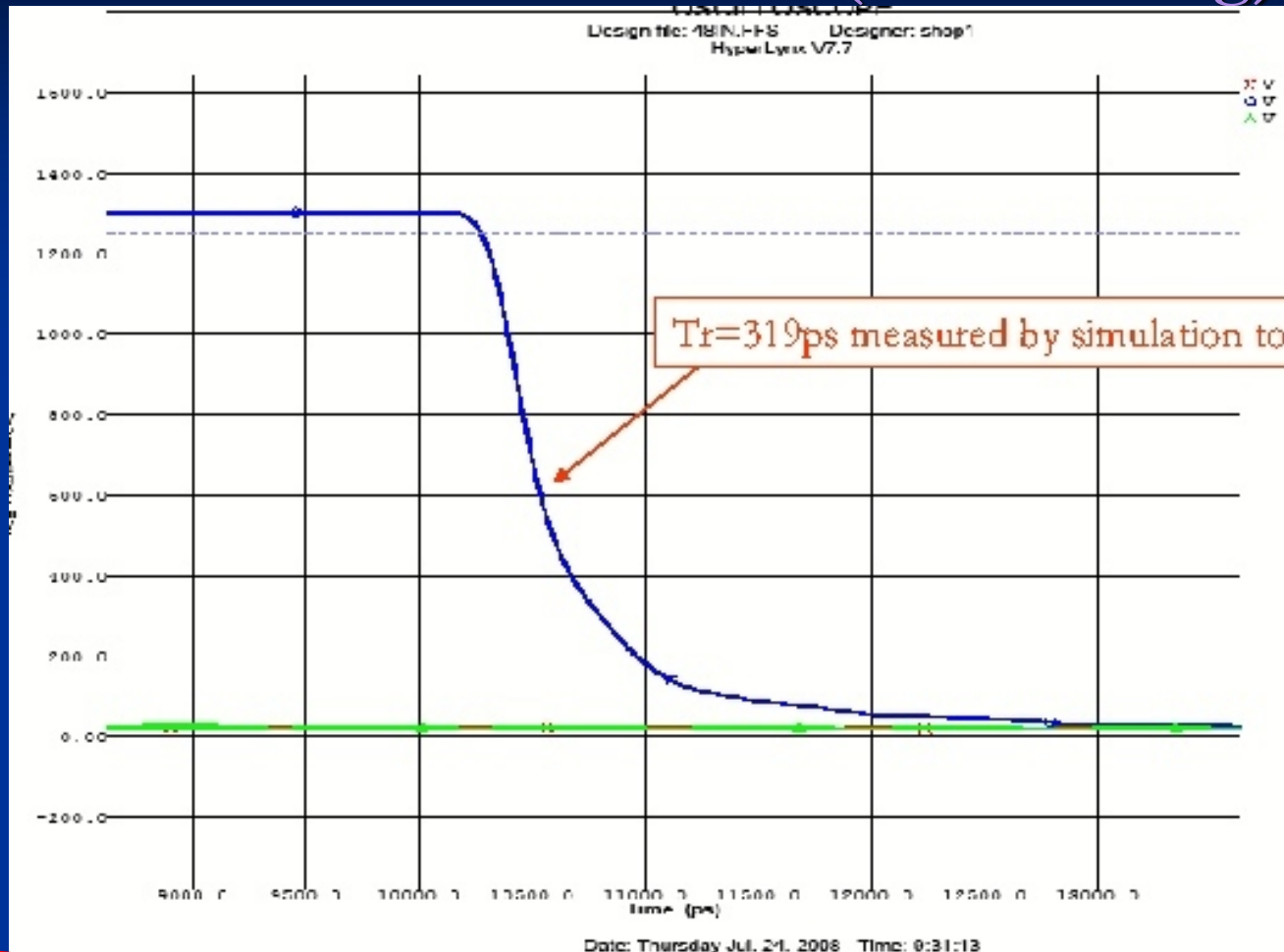


# Comparison of measurements (Ed May and Jean-Francois Genat and simulation (Fukun Tang)



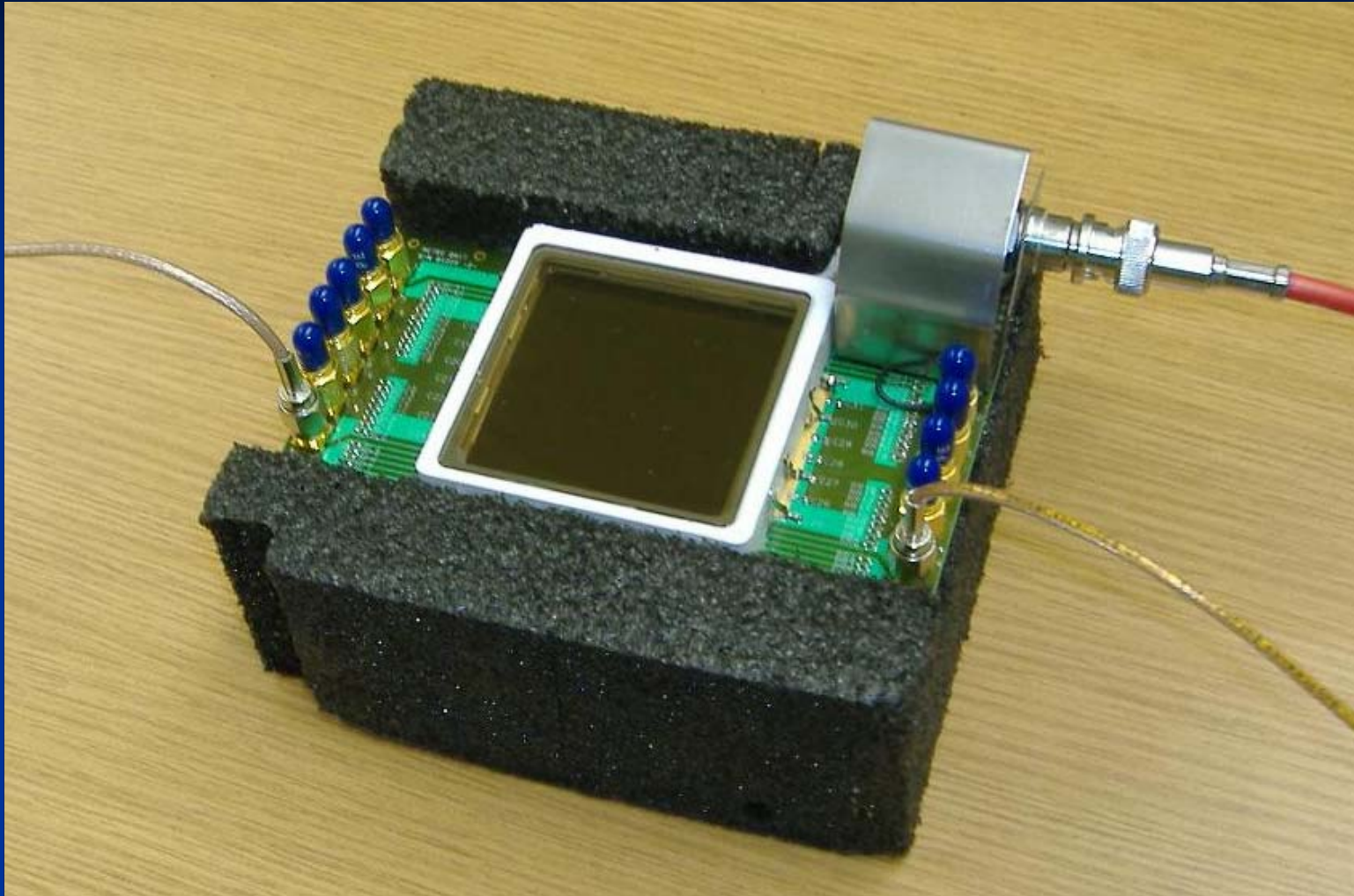
- Transmission Line- simulation shows 3.5GHz bandwidth- 100 psec rise (well-matched to MCP)
- The time difference yields a velocity of 64ps/cm against 68ps predicted

# Scaling Performance to Large Area Anode Simulation(Fukun Tang)



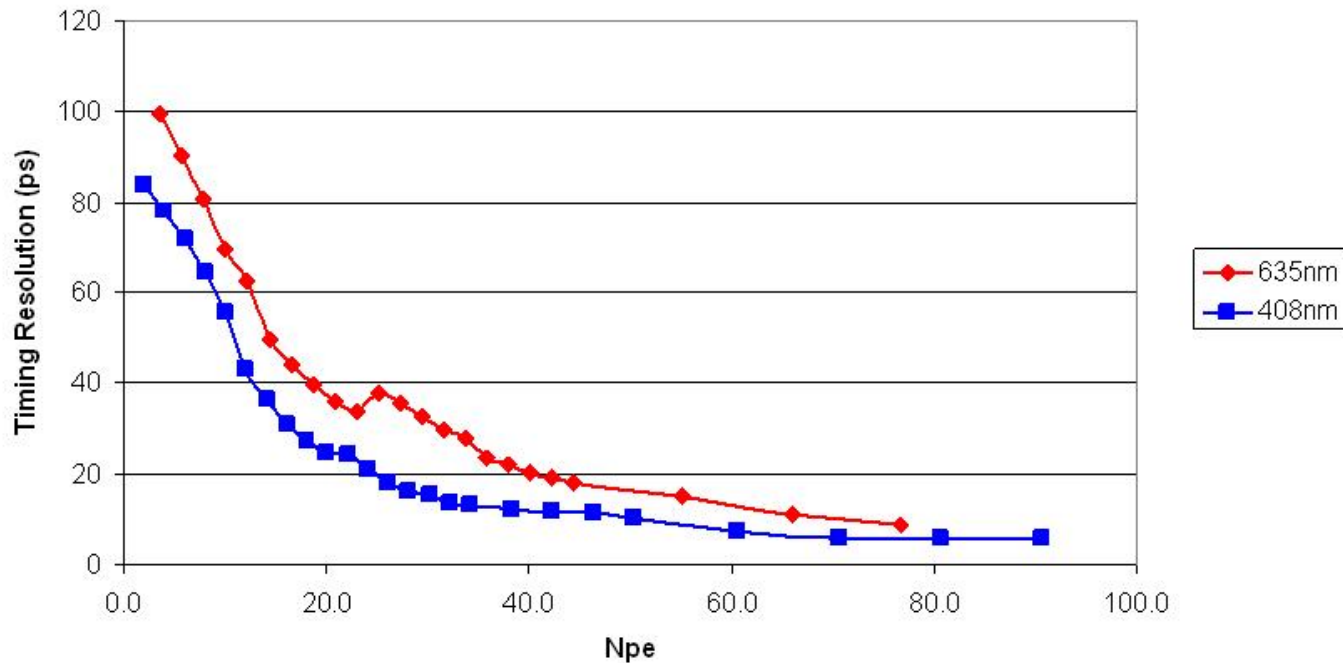
- 48-inch Transmission Line- simulation shows 1.1 GHz bandwidth- still better than present electronics.

# Photonis Planicon on Transmission Line Board



Couple 1024 pads to strip-lines with silver-loaded epoxy (Greg Sellberg, Fermilab).

## Timing Resolution of 408nm vs. 635nm Laser



Camden Ertley results using ANL laser-test stand and commercial Burle 25-micron tube- lots of photons  
(note- pore size may matter less than current path!- we can do better with ALD custom designs (transmission lines))



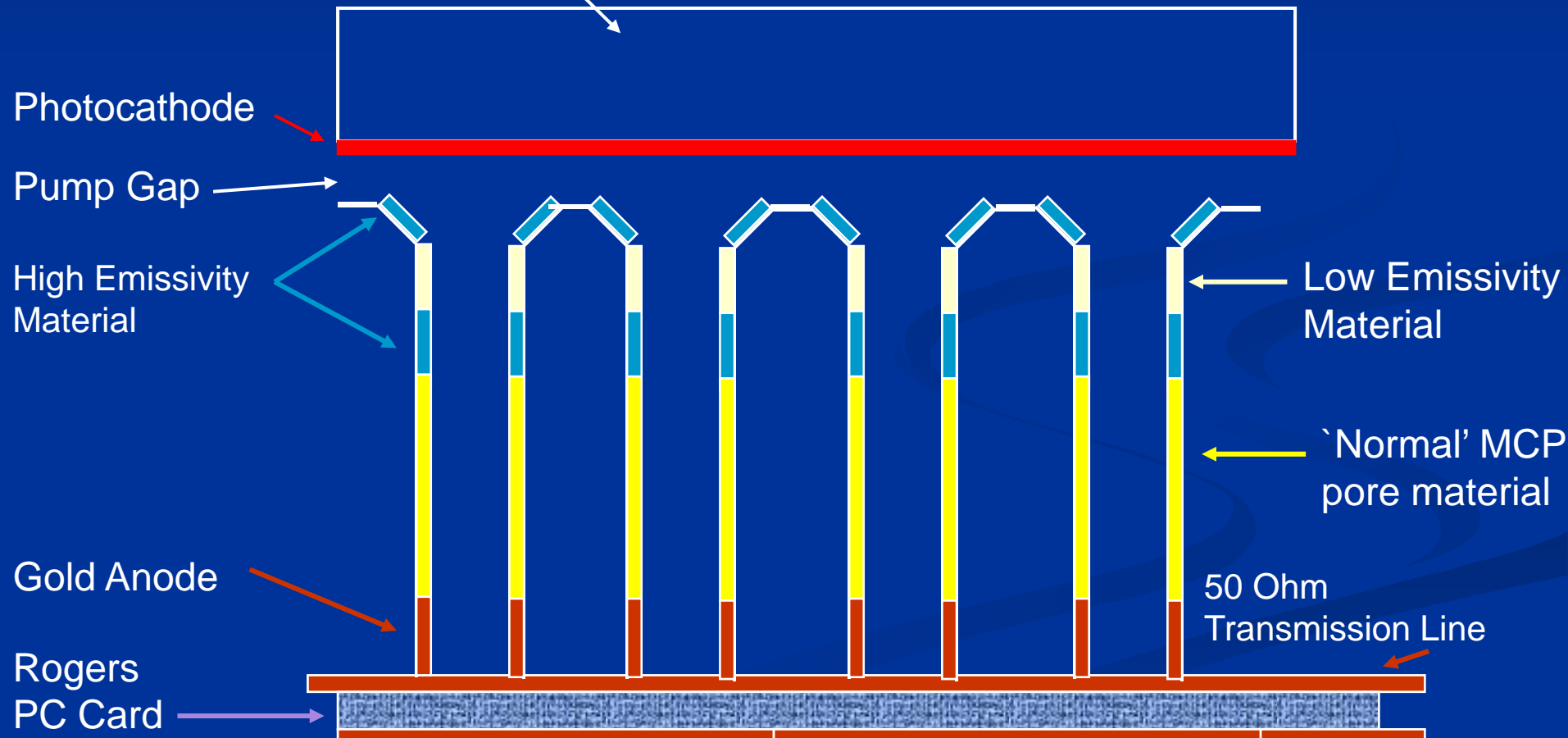
# Understanding the contributing factors to 6 psec resolutions with present Burle/Photonis/Ortec setups- Jerry Vavra's Numbers

1. TTS: 3.8 psec (from a TTS of 27 psec)
2. Cos(theta)\_cherenk 3.3 psec
3. Pad size 0.75 psec
4. Electronics 3.4 psec

# Large-area Micro-Channel Plate Panel "Cartoon"

N.B.- this is a 'cartoon'- working on workable designs-join us...

Front Window and Radiator



4/16/2009

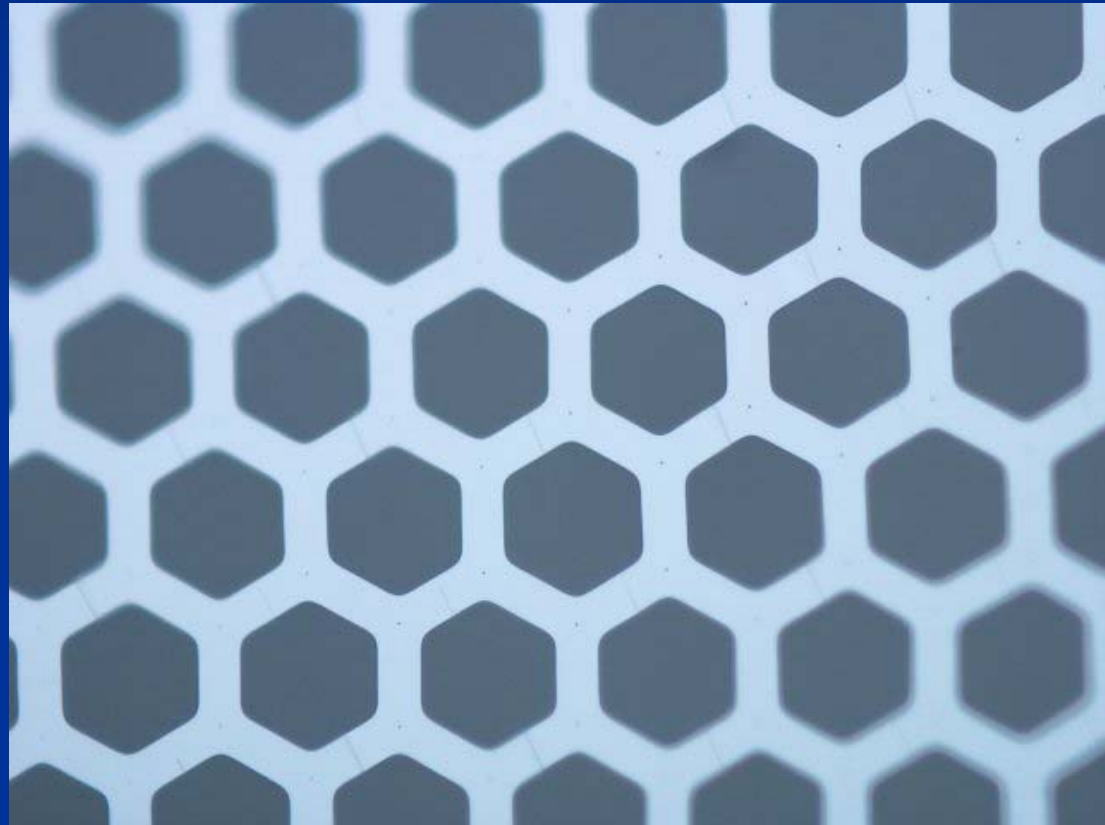
Capacitive Pickup to Sampling Readout

LHCb Upgrade Meeting

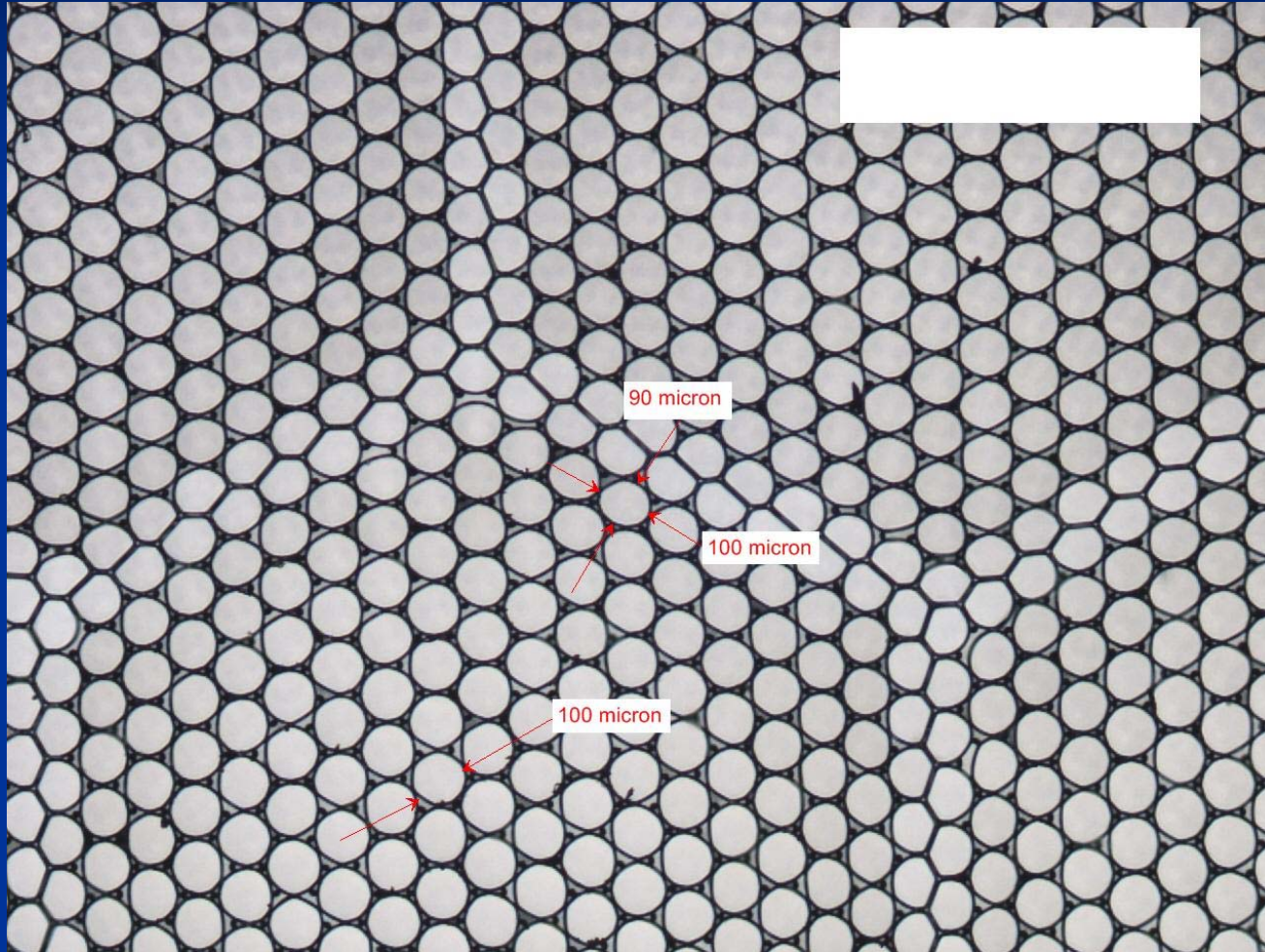
61

# Incom glass capillary substrate

- New technology-  
use Atomic  
Layer Deposition  
to `functionalize  
an inert  
substrate-  
cheaper, more  
robust, and can  
even stripe to  
make dynode  
structures (?)



# Another pore substrate (Incom)





# Front-end Electronics

## Critical path item- probably the reason psec detectors haven't been developed

- We had started with very fast BiCMOS designs- IBM 8HP- Tang designed two (really pretty) chips
- Realized that they are too power-hungry and too 'boutique for large-scale applications
- Have been taught by Gary Varner, Stefan Ritt, Eric DeLanges, and Dominique Breton that there's a more clever and elegant way- straight CMOS – sampling onto an array of capacitors
- Have formed a collaboration to do this- have all the expert groups involved (formal with Hawaii and France)- see talks by Tang and Jean-Francois at Lyon



## II STATE OF THE ART

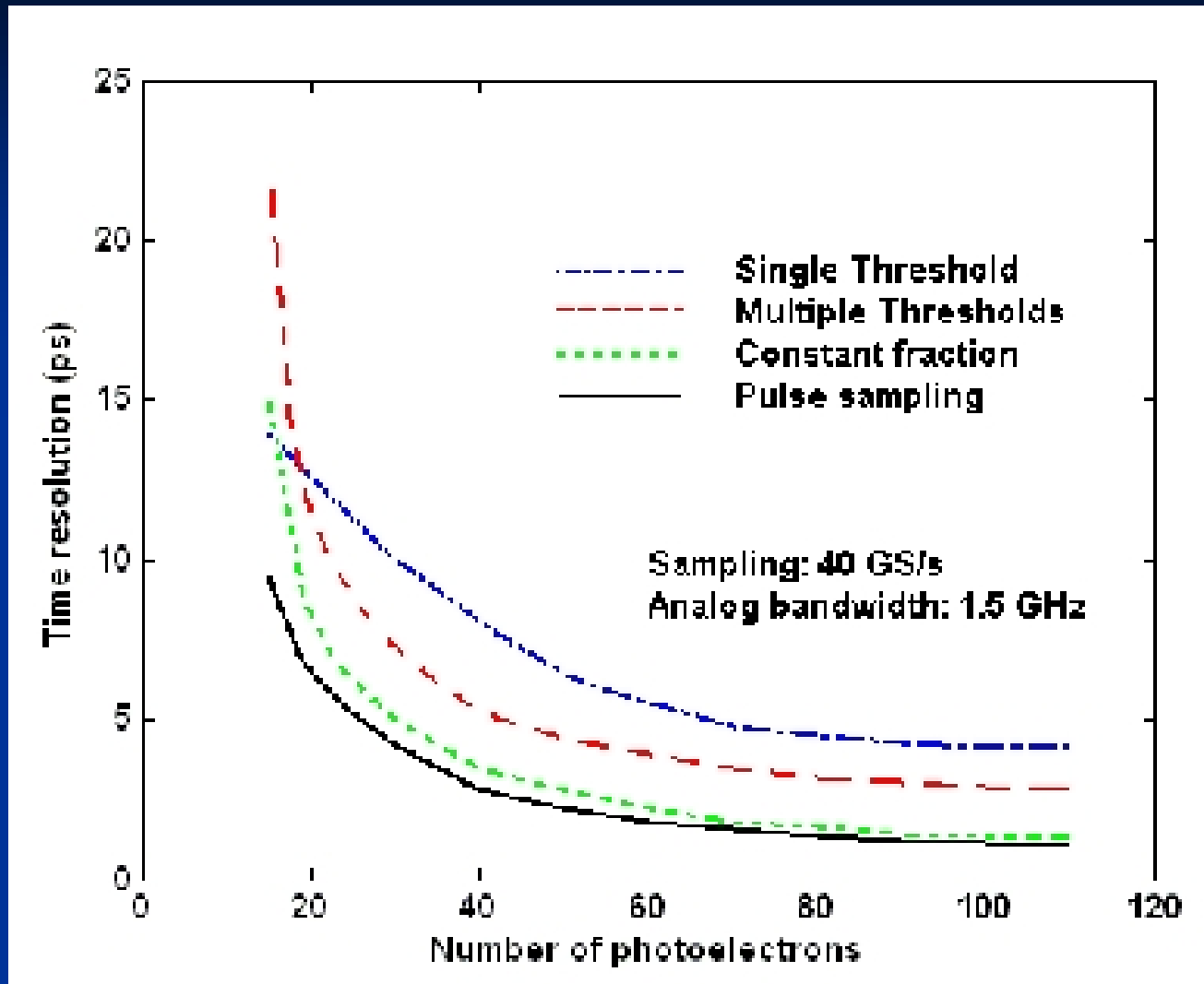
Several circuits have already been designed in the HEP community for fast pulse sampling, mainly to record photo-multipliers pulse shapes. As detailed in section I, fast timing requires higher sampling rates, but smaller dynamics ranges.



	Hawaii		Orsay/Saclay		PSI		PSEC
	Lab 3	Planned Elab2	Sam	Planned	DR S3	Planned DR S4	This proposal
Sampling frequency	20 MHz-3.7 GHz	1-10 GHz	0.7-2.5 GHz	10 GHz	10 MHz-5 GHz	5 GHz	40 GHz
Analog bandwidth	900 MHz	850 MHz	300 MHz	650 MHz	450 MHz	> DR S3	> 1 GHz
Number of Channels	9	16	2		12/62/1	8/4/2/1	16
Triggered mode	Common Stop	Channel trigger or stms	Common Stop		Common Stop	Common Stop	Channel trigger
Resolution		10 bit	11.6 bit		11.6 bit	11.5 bit	8-10 bit
Samples	256	48 rows of 512	256	2048	1024-12288	1024-8192	64
Clock	33 MHz	33 MHz	66 MHz		20 MHz	16amp/2048	60 MHz
Max latency			5ns		0.5 ns		
Input Buffers		TIA (500km gate)	Yes	No	No	No	Yes
Differential inputs	No	Pseudo-diff	Yes		Yes	Yes	Pseudo diff
Input impedance	500 kms Ext	30-700 kms adjustable	> 10 MΩ/km			7-1 pF	
Readout clock		1 GHz Wilkinson	16 MHz		33 MHz	33 MHz	60 MHz
Readout time	150µs	512µs	< 2 µs		30ns * 1, samples	30ns * 1, samples	< 1 µs
Locked delays	Ext DAC	Ext DLL	Ext DLL		Ext PLL	Ext PLL	
On-chip ADC	Yes	1 GHz Wilkinson	No		No	No	Yes
R/W's in channels		Yes	No		No	Yes	No
Power/clk	50mW	20mW/s ample 0.2W/read	150 mW		1-13mW	2-20mW	
Dynamic range		1mV/1V	0.65mV-2V		0.35mV/1.1V	0.35/1V	1V
Xtalk	Average <= 10%	< 0.1%	0.30%		<0.5%	<0.5%	
Sampling jitter		T&D	40ps		200ps (Ext PLL)	Ext PLL	10ps
Power supplies	2.5V	2.5V	0-3.3V		2.5V	2.5 V	1.8V
Process	TSMC 0.25	TSMC 0.25	AMS 0.35	AMS 0.18	UMC 0.25	UMC 0.25	CMOS 0.13
Chip area	2.5 mm <sup>2</sup>	12 mm <sup>2</sup>	10 mm <sup>2</sup>		25 mm <sup>2</sup>	25 mm <sup>2</sup>	1 mm <sup>2</sup>
Cost/channel		500\$/40 10\$/2k	15.7\$/12k			10-15\$	

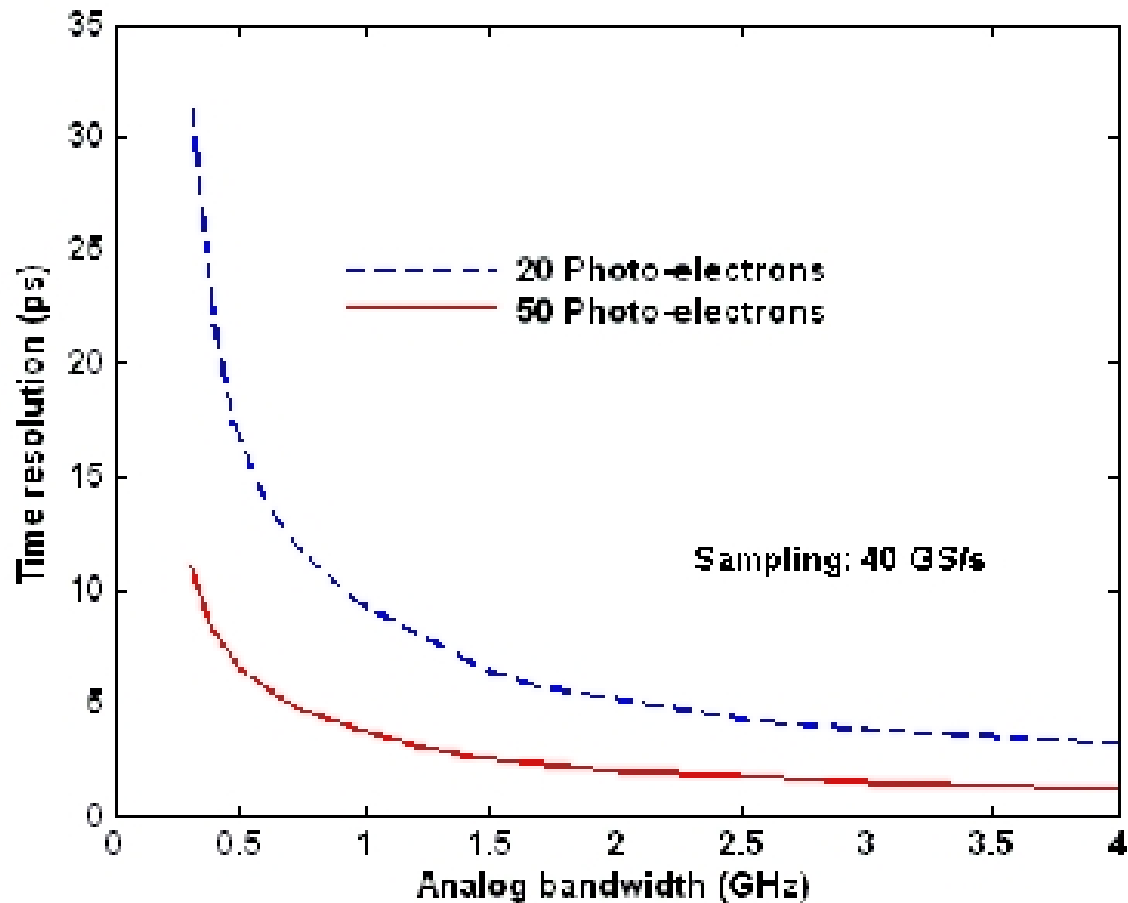
Table 1. State of the art, this proposal. The yellow column is from Gary Varner's group at the University of Hawaii (USA) [12], the light blue from Dominique Breton from the University of Paris-Sud (Orsay) [10] and Eric Delagnes from CEA (Saclay), (France) [11]. The orange column from Stefan Ritt at PSI (Switzerland) [13]. The dark blue is this proposal.

# Front-end Electronics



■ Wave-form sampling does well- CMOS (!)

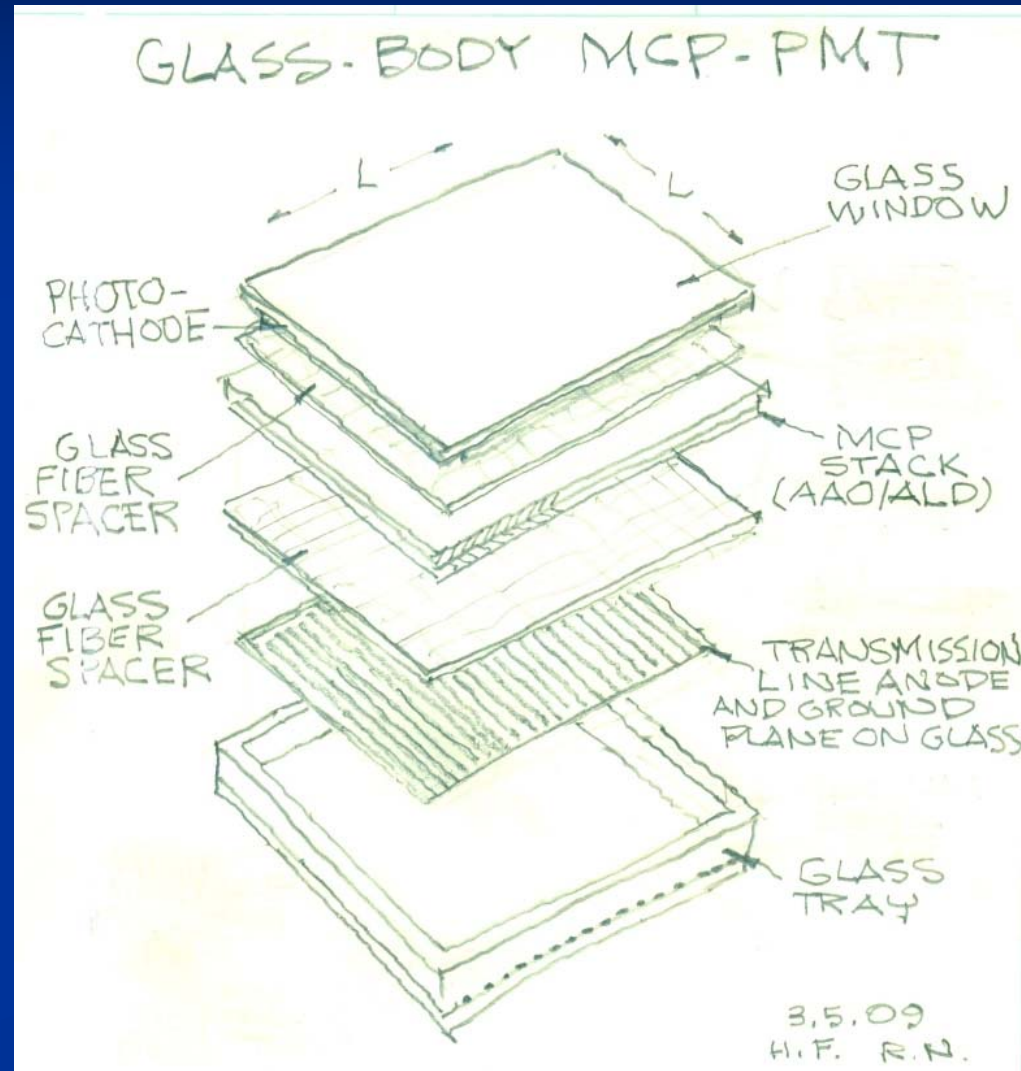
# Front-end Electronics-II



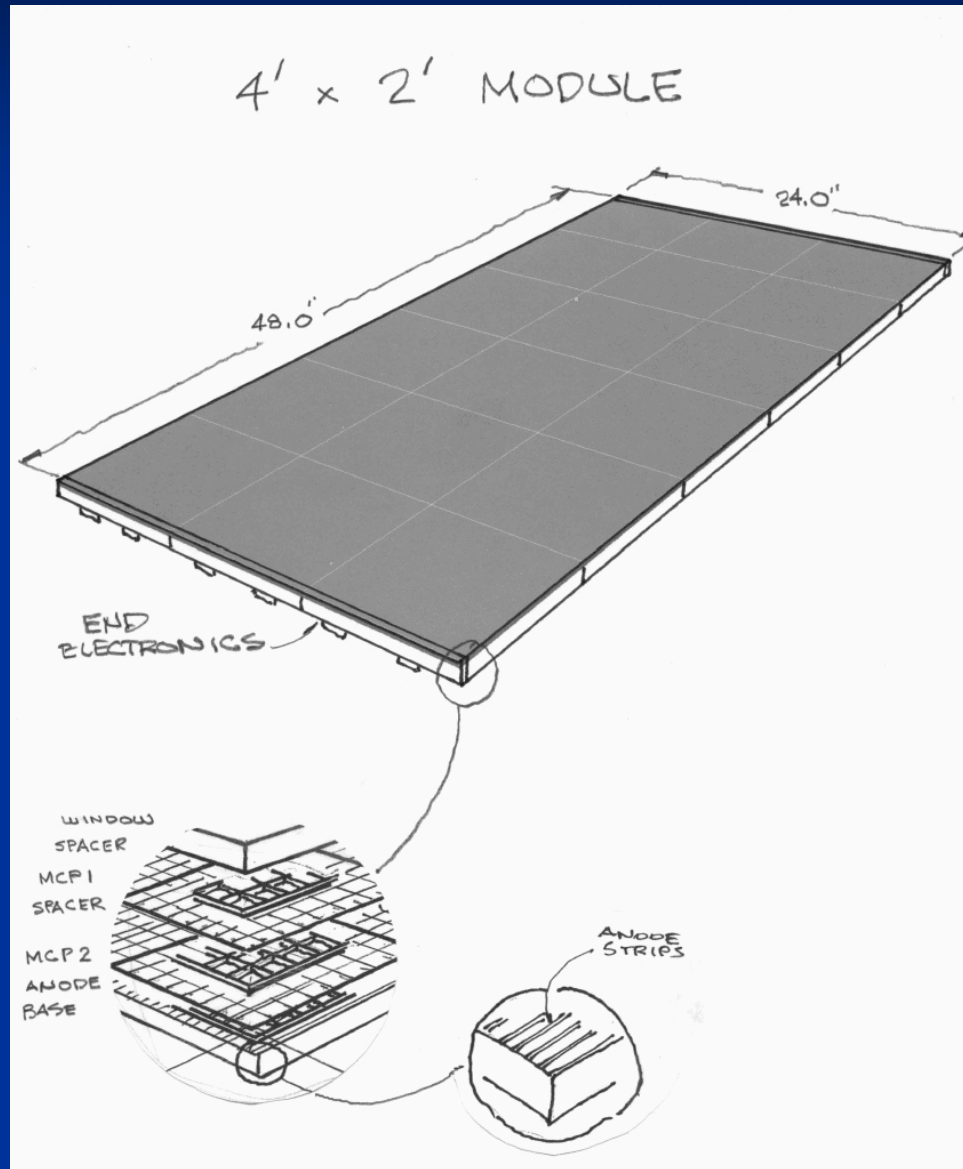


# Cartoon of a 'frugal' MCP

- Put all ingredients together- flat glass case (think TV's), capillary/AJD amplification, transmission line anodes, waveform sampling



# Can dial size for occupancy, resolution- e.g. neutrinos 4'by 2'



# Plans to Implement This

## The Development of Large-Area Fast Photo-detectors

April 15, 2009

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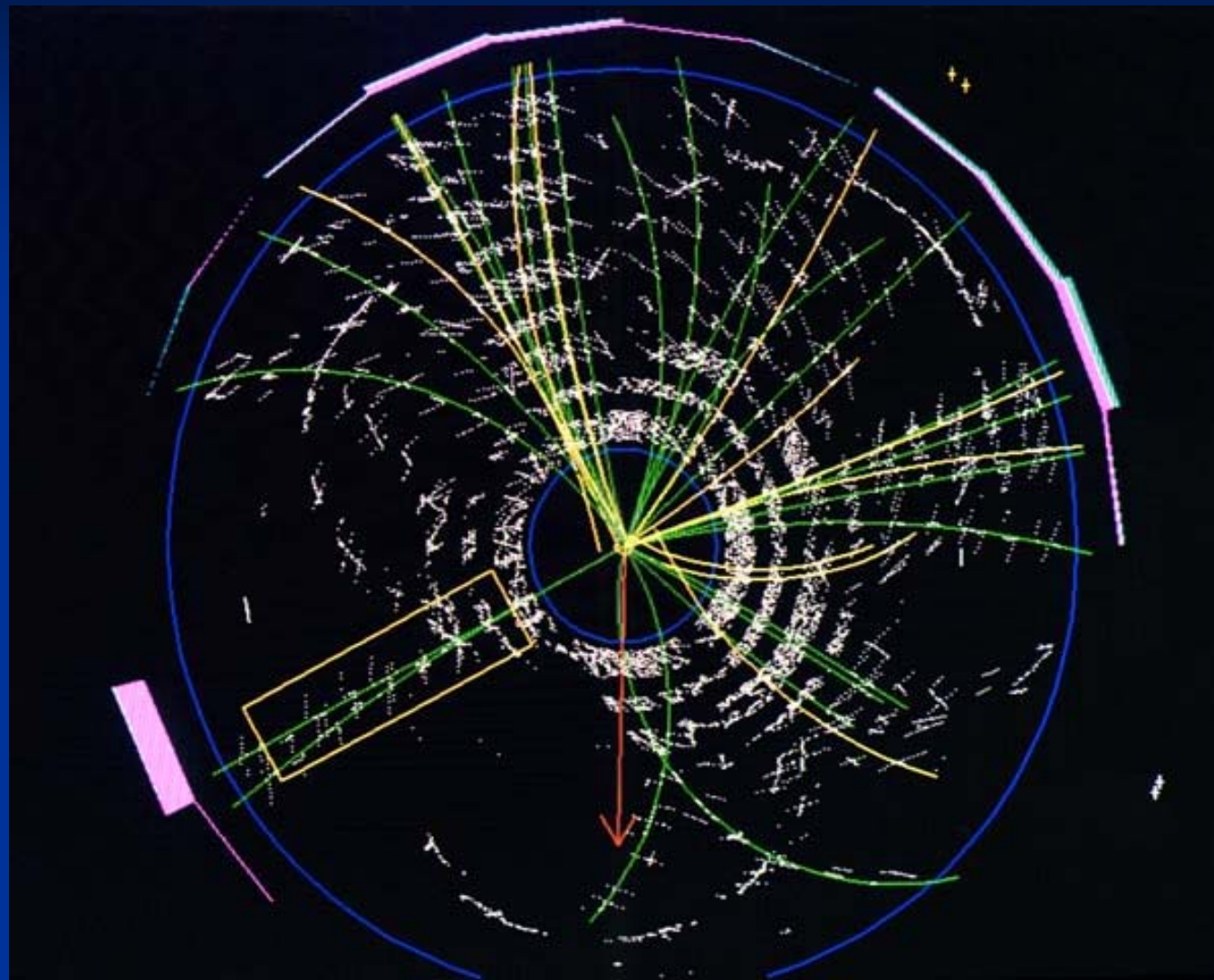
Have formed a  
collaboration to do this  
in 3 years. 4 National  
Labs, 5 Divisions at  
Argonne, 3 companies,  
electronics expertise at  
UC and Hawaii  
R&D- not for sure, but  
we see no show-stoppers

# What can LHCb do? Need Serious Simulation of 1-10psec TOF

- Need a list of physics drivers- (e.g J/Psi-eta, pizero-Kzero CP Asym.,...)
- What is required rate, occupancy vs radius?
- What resolution is necessary for each analysis?
- What is budget, schedule?
- So need a serious simulation effort.
- Are there folks who would work with us on this and vice versa?



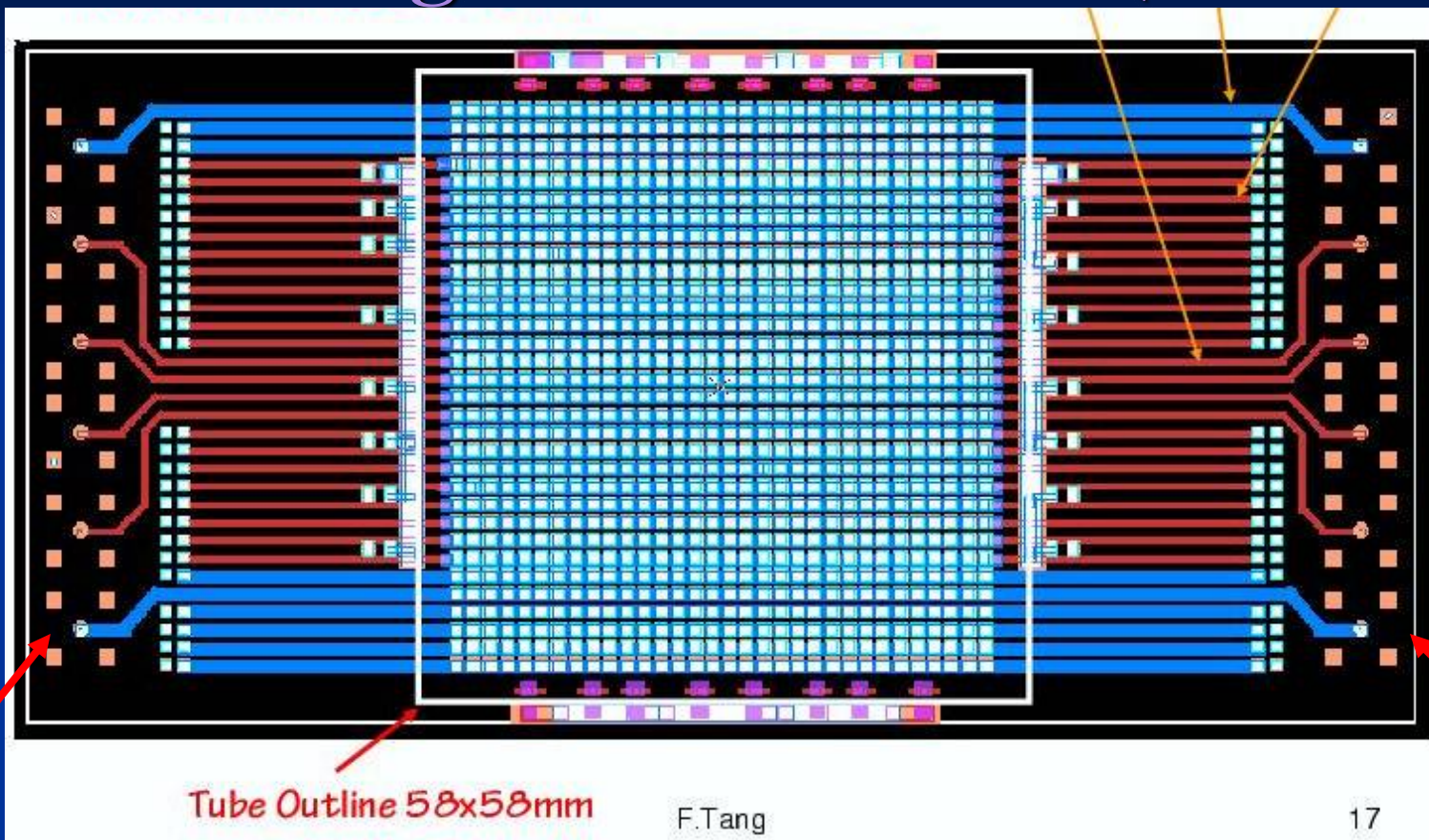
# The End-





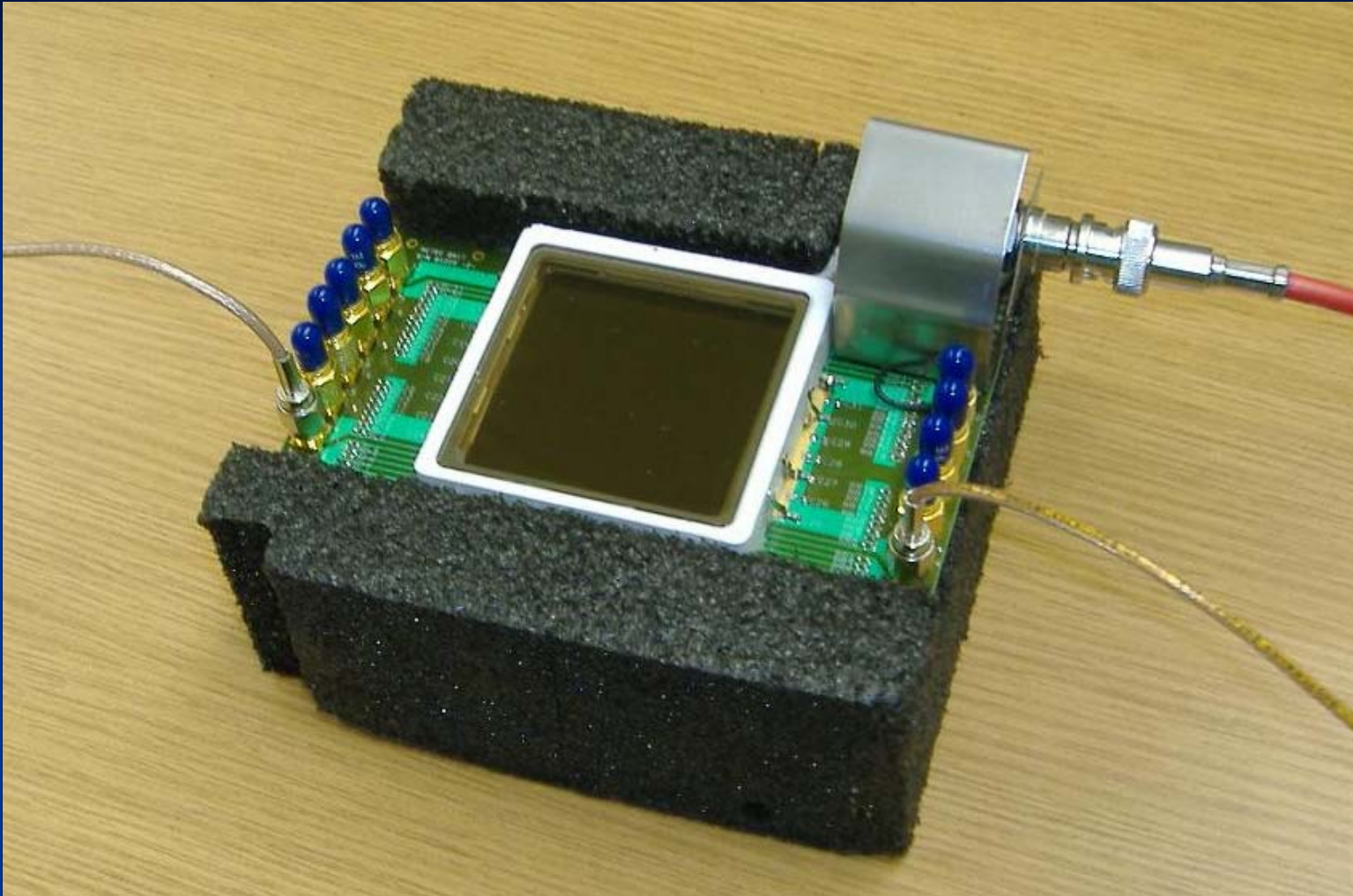
# Get position AND time

## Anode Design and Simulation(Fukun Tang)



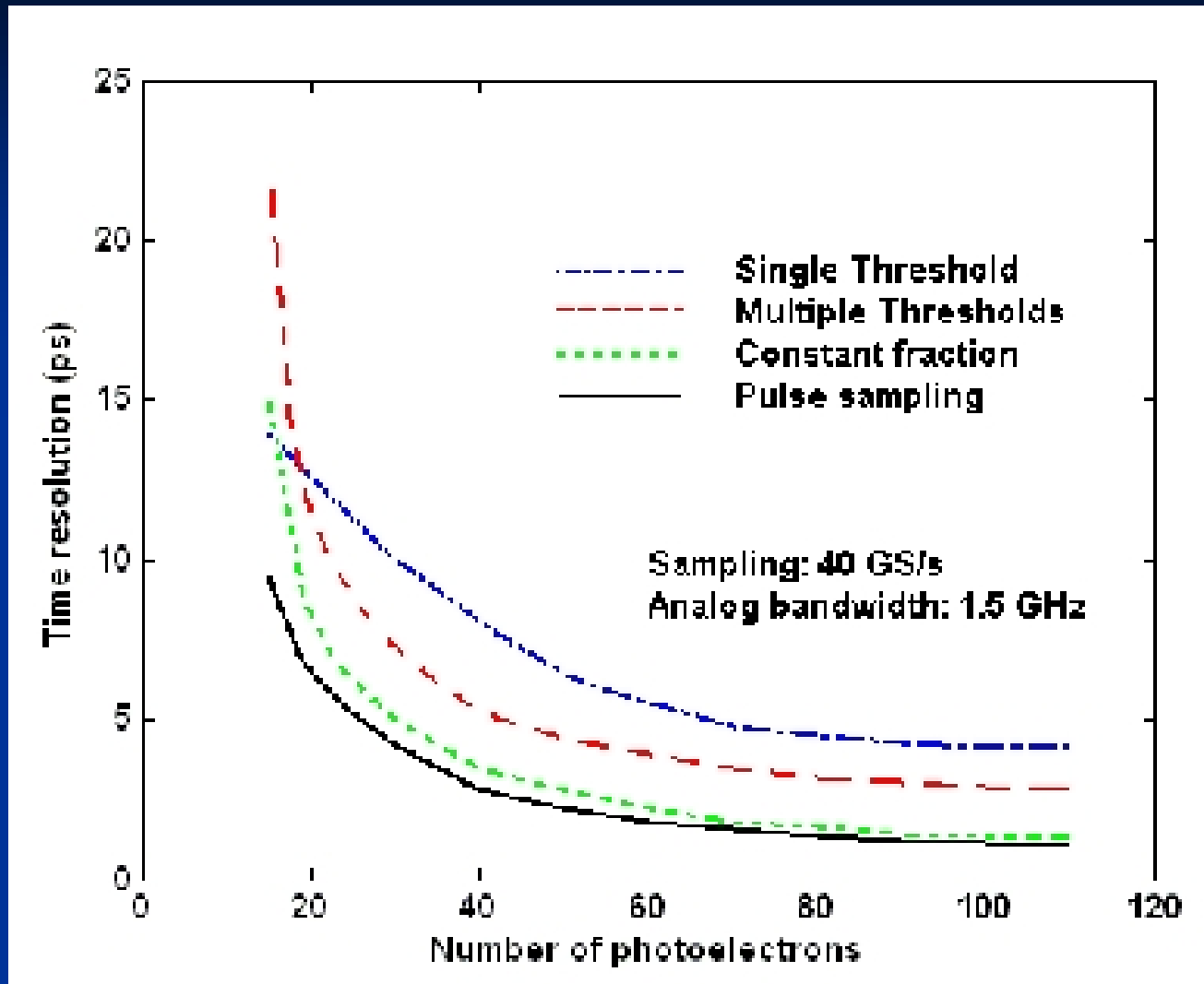
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# Photonis Planicon on Transmission Line Board



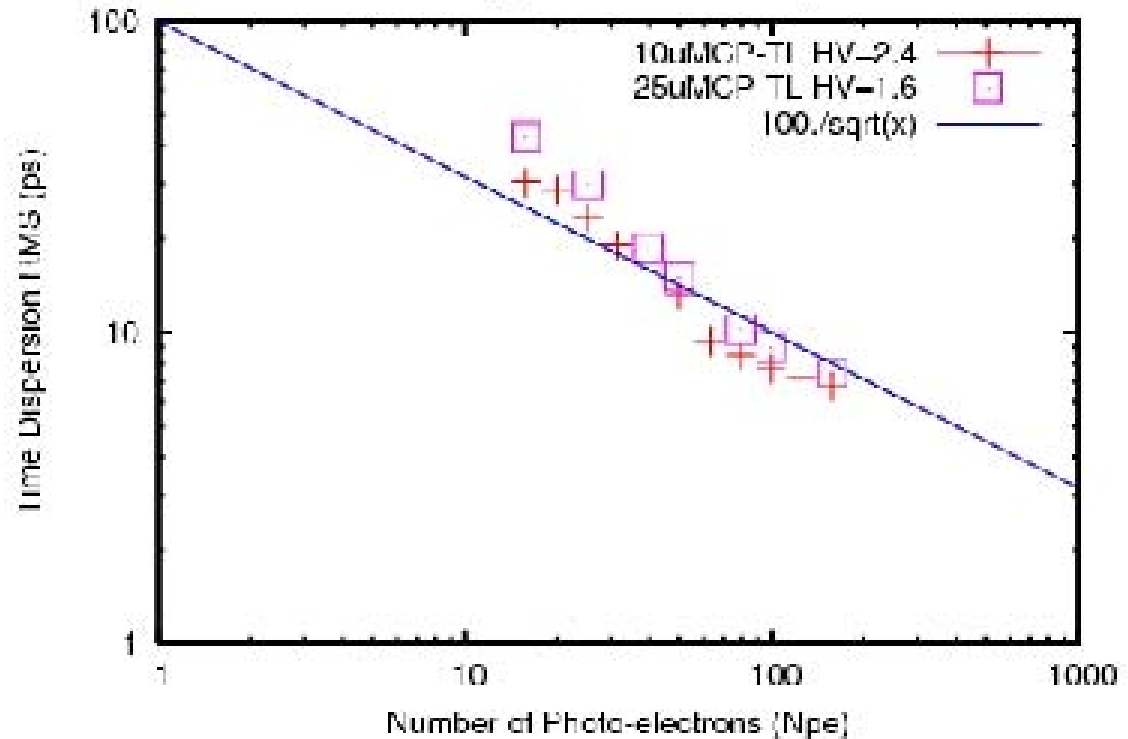
Couple 1024 pads to strip-lines with silver-loaded epoxy (Greg Sellberg, Fermilab).

# Front-end Electronics



- Wave-form sampling does well- CMOS (!)

Time resolution v. Light for MCP with Delay Line Readout





# Application to a water Cherenkov Counter- effect on the physics

