THE UNIVERSITY OF CHICAGO

CHARGED PARTICLE TRACKING IN AN OPTICAL TIME PROJECTION
CHAMBER

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ABSTRACT

A first experimental test of tracking relativistic charged particles with a water Cherenkov optical time projection chamber (OTPC) is described. Using planar micro-channel plate photo-multiplier tubes (MCP-PMT) coupled to an anode of 50Ω microstrips, we have demonstrated the ability to measure the time and 2D spatial coordinates of individual optical photons. With a single photon time resolution better than 100 ps and spatial resolutions of a few mm, it is feasible to use the relative timing and detected positions of Cherenkov photons to reconstruct the particle trajectory. The detector consists of a 77 cm long, 40 kg cylindrical water mass instrumented with a combination of commercial 27 cm^2 MCP-PMTs and 45 cm^2 mirrors in a stereo configuration. For each MCP-PMT, a mirror is mounted on the opposing side of the detector allowing an increase of the photo-detection efficiency by time resolving the direct and reflected Cherenkov light. A 180-channel data acquisition system digitizes the MCP-PMT signals using the PSEC4 waveform sampling chip operating at 10 Gigasamples-per-second. The detector was installed on the Fermilab MCenter test-beam in a location where the primary flux is multi-GeV muons. Muon tracks are reconstructed in 3D by fitting the time-projection of detected Cherenkov photons along the vertical and azimuth axes of the detector. Tracking resolutions of AAA cm and BBB 20 mrad are shown.

CHAPTER 1

INTRODUCTION

The concept of the time-projection chamber (TPC) was introduced in 1974 by Nygren as a novel tracking detector to study e^+e^- collisions. This technological advancement was a "new approach to the problems of track recognition and momentum measurements of high energy charged particles", particularly in environments with large magnetic fields and high track multiplicity [1]. The first TPCs were gaseous detectors in which a strong electric potential, which is applied between a central cathode and a segmented readout anode comprised of multi-wire proportional chambers, runs parallel to a solenoidal magnetic field. A high momentum charged particle traversing the volume ionizes the gas, enabling the freed electrons to drift in an ideally straight path to the anode. Serving as a proxy for the charged particle, these 'drifting' non-relativistic electrons are time-projected on the anode, allowing the particle's 3-D path and its ionization loss (dE/dx) to be measured with 100 μm precision and 3% resolution, respectively [2, 3, 4].

Since its original application the TPC has been adapted and applied to other areas of particle and astro-physics. In particular, the use of cryogenic liquid Argon TPCs for neutrino detection was proposed soon after the invention and is now a prevalent technology in contemporary and planned future detectors [5]. In these TPCs the neutrino flavor and interaction kinematics are inferred through calorimetry and tracking of the outgoing charged lepton (in the case of a charged current interaction) and/or recoil particles.

Water Cherenkov and liquid scintillator detectors are among non-cyrogenic technologies for neutrino oscillation physics experiments. Due to their directionality, the prompt Cherenkov photons generated along a particle trajectory are uniquely suited to track charged particles [6]. The photosensors used in these experiments are conventional photo-multipliers (PMTs), which are one-pixel devices with single photon time resolutions > 1 ns [7, 8]. In an event window of several nanoseconds, the PMTs are capable of discerning the total number and the aggregate time of the prompt photons. High granularity particle tracking is not

[28] possible in these primarily ring-imaging detectors, though event and vertex reconstruction

[29] techniques are sophisticated [9].

1.1   The Optical TPC

[31] In this thesis, we investigate a new type of charged particle tracking TPC using Cherenkov

[32] radiation in a water detector. Applying photo-detection technology developed by the Large-

[33] Area Picosecond Photo-Detector (LAPPD) collaboration [10], it is possible to tag individual

[34] photons with spatial and timing resolutions of ≤ 3 mm and ≤ 100 ps, respectively, while in-

[35] strumenting relatively large areas [11, 12]. Each photon can now be resolved in 3-dimensions

[36] (2 space + 1 time) permitting the concept of a 'photon-' or 'optical-' time-projection chamber

[37] (OTPC) using Cherenkov light generated along a particle track.

1.1.1   Enabling Technology: LAPPD MCP-PMT
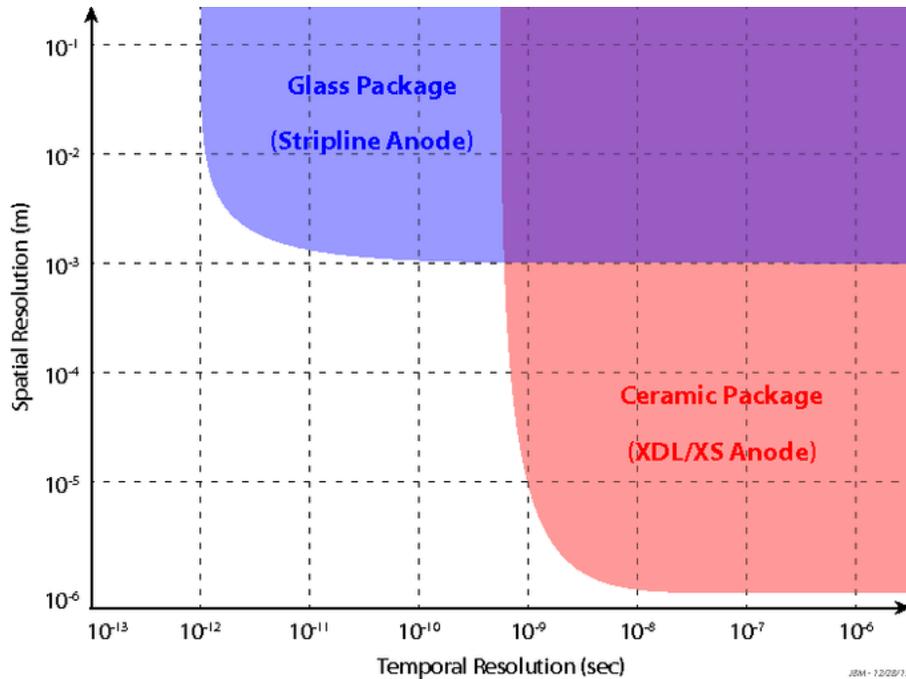
Figure 1.1: LAPPD MCP-PMT spatial vs. timing resolutions for different anode architectures. With the economical glass-package, the single photon resolutions are ≤ 3 mm and ≤ 100 ps. Figure courtesy of J. McPhate, SSL.

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To realize an optical-TPC, a low time-jitter and high granularity photosensor is needed to augment conventional single-pixel PMTs in a water Cherenkov detector. Micro-channel plate photomultiplier tubes (MCP-PMT) are inherently low-jitter amplifying devices due to the relatively small variation in electron path lengths in the dynode. Measured single photon jitter can be better than 50 ps with signal rise times <100 ps [13, 14]. Through novel fabrication techniques and low-cost materials, the LAPPD project is developing 20×20 cm^2 active-area MCP-PMTs that are intended to be economically scalable to instrumenting large detectors [11, 12, 15, 16].

The spatial resolution in an MCP-PMT is largely determined by the anode design that sets the number of MCP pores, and hence the effective pixel size, which will be coupled together in readout. The spatial vs. timing resolution for the full signal range of LAPPD MCP-PMTs is shown in Figure 1.1 for different anode geometries. For the glass hermetic package, an array of parallel of microstrip lines allows an economical readout scheme while preserving good time resolution [17]. To have a precise, ∼micron-level imaging detector, a more expensive cross-strip anode can be implemented in a ceramic package at a cost in timing resolution.

1.1.2   A prototype OTPC

To demonstrate this technique, we have built a 40 kg water Cherenkov detector using a combination of commercial MCP-PMTs and optical mirrors. A concept drawing of the optical setup of for this detector is shown in Figure 1.2. For each planar MCP-PMT mounted on the water volume, a mirror is mounted on the opposing side creating an image of the Cherenkov light hitting the opposing wall. For a given charged particle track, the mirror adds a discrete set of reflected photons that are time-resolved, thus economically doubling the photodetection efficiency over the angular acceptance of the detector.

As the LAPPD MCP-PMTs are not yet available, this prototype relies on commercial MCP-PMTs that exhibit the same detection resolutions, but with 1/16 the photo-active area
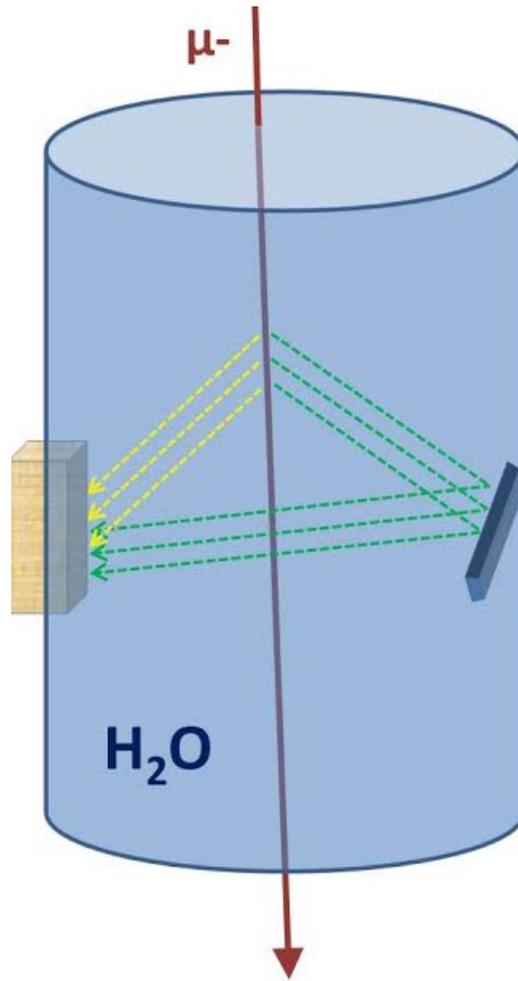
Figure 1.2: The concept of the prototype water-based OTPC. A charged particle emits Cherenkov light in the water volume. For each time and spatial-resolving MCP-PMT (left), a mirror is mounted on the opposing side. The mirror adds a discrete reflected set of photons (green) that can be time resolved from the direct Cherenkov light (yellow).

⁶⁵ per unit. The commercial photo-detector used is Planacon XP85022 MCP-PMT device from

⁶⁶ PHOTONIS [18]. The total photo-coverage in the prototype OTPC is only 125 cm^2 over

⁶⁷ the surface $\sim$1700 cm^2 enclosing the fiducial volume.

⁶⁸ 1.2   Cherenkov Radiation

⁶⁹ A charged particle exceeding the speed-of-light in a dielectric medium will emit coherent

⁷⁰ Cherenkov radiation in a thin conical volume symmetric about the particle trajectory at a

⁷¹ polar angle of θ_c given by

$$\cos\theta_c = \frac{1}{n\,\beta} \tag{1.1}$$

⁷² where n is the phase index of refraction of the medium. In a realistic detector the medium

⁷³ will be dispersive, such that $n = n(\omega)$, giving rise to a distribution of θ_c's. In a dispersive

⁷⁴ medium the Cherenkov wavefront does not travel perpendicular to the photon propagation

⁷⁵ direction. Rather, the opening angle of the wavefront with respect to the particle direction,

⁷⁶ η, is derived by Tamm

$$\cot(\eta) = \frac{d}{d\omega}(\omega\,\tan\theta_c)|_{\omega_o} =$$
$$(\tan\theta_c\,+\,\beta^2\omega\,n(\omega)\,\frac{dn}{d\omega}\cot\theta_c)|_{\omega_o} \tag{1.2}$$

⁷⁷ in which ω_o is the center frequency over the limited optical wavelength range of interest [19,

⁷⁸ 20]. The first term in Eqn. 1.2 is the θ_c complement angle and the second term contributes

⁷⁹ a dispersion dependent factor that will be positive within a normally dispersive wavelength

⁸⁰ range ($\frac{dn}{d\lambda} < 0$) in a medium. The Cherenkov emittance and opening angles are shown in

⁸¹ Figure 1.3 in the context of the OTPC

⁸²   The condition that $\eta + \theta_c < 90°$ in dispersive media is explained by the fact that the

⁸³ Cherenkov photons, which are generated at an angle specified by the phase velocity of the

⁸⁴ dielectric medium, propagate at the speed at which energy is transported in the dielectric:

<div align="center">5</div>

the group velocity. As shown in Ref. [21], the group velocity is expressed as

$$v_g(\omega) = \frac{c}{n_g(\omega)} = \frac{c}{n(\omega) \,+\, \omega \,(dn/d\omega)} \qquad (1.3)$$

where the group index, n_g, is both greater in magnitude and more dispersive than n [22, 23].

1.3   Outline

The implementation of LAPPD MCP-PMTs neutrino physics experiments has been proposed in several applications [24, 25, 26, 27]. These applications share a common goal of using precision timing and digital 3D photon tagging to significantly enhance the reconstruction of neutrino interactions in non-cryogenic liquid detectors [28]. By building an MCP-PMT-equipped 40 kg water Cherenkov detector, this thesis presents a proof-of-principle of reconstructing charged particle tracks in an OTPC.

A realistic experiment will face similar challenges as it will likely be economically impossible to instrument 100% of a water Cherenkov detector with MCP-PMTs. It will then be necessary to use a limited coverage of fast timing and high spatial granularity photodetectors to reconstruct OTPC-generated track segments. These track segments, in combination with additional conventional PMT coverage, can be stitched together to complete the time-sliced picture of the event.

In the following chapters, the implementation and results from a prototype OTPC detector are described. The detector design, optical properties, photo-detection, and electronics readout is discussed in Chapter 2. Chapter 3 describes the the experimental setup and installation at the Fermilab National Laboratory test-beam facility. Chapter 4 presents the test-beam datasets and Chapter 5 follows with an analysis of these data and the detector performance. Finally, Chapter 6 concludes and discusses future considerations with this technology.
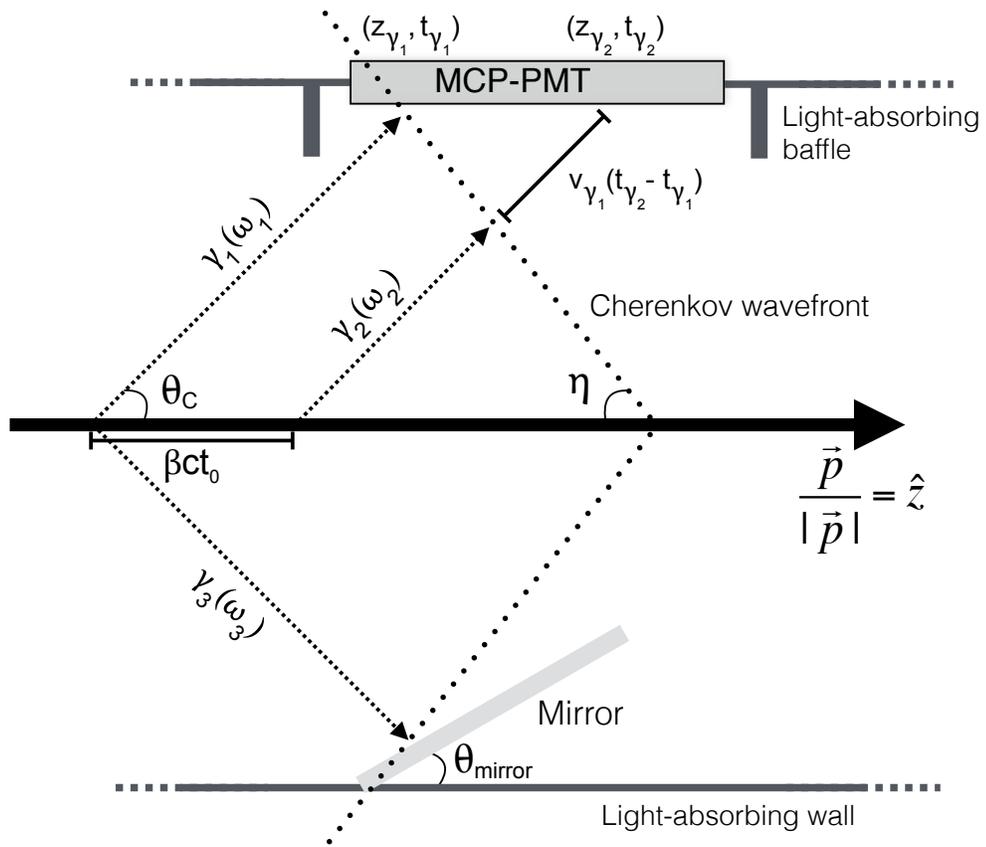
Figure 1.3: Two-dimensional projection of the Cherenkov light generated by a relativistic charged particle (heavy, black arrow) and the OTPC optics.

CHAPTER 2

DETECTOR

The OTPC is a small-scale, prototype detector that was constructed to demonstrate the principle of tracking high momentum charged particles through a water volume in a cosmic ray and test-beam setting. The following sections cover an overview of the detector: the OTPC design (§2.1), the detector optics (§2.2), and the photodetector module (§2.3).

2.1 Design

The detector is constructed from a 24 cm inner-diameter Poly-Vinyl Chloride (PVC) cylindrical pipe cut to a length of 77 cm. Six 11 cm diameter ports were machined in the tube arranged in 2 columns of three ports each along the cylindrical axis. These columns have an azimuthal separation of 65°. The photodetector modules (PMs), described in §2.3, are mounted on five of these ports. The column with 3 PMs installed is denoted the 'normal' view and the other the 'stereo' view. The dual views are shown in a rear-view drawing of the OTPC in Figure 2.1.

For each PM, a first-surface broadband optical mirror is mounted on the opposing wall facing the PM port. The 7.6 cm square mirrors are installed on the interior wall of the cylinder at an angle of 48°, which is denoted as θ_{mirror} in Figure 1.3. Consequently, the mirrors protrude somewhat into the detector volume giving a horizontal distance from the mirror center point to the PM port of ∼20 cm. A rendering of the OTPC detector is shown in Figure 2.2 as modeled in Chroma [29].

The remaining exposed PVC surfaces of the interior wall were painted with light absorbing paint [30]. An economical choice of outdoor rated black matte spray paint was used. Multiple coats were applied after lightly sanding in between.

The detector is filled with 40 L of deionized water for the target volume. Because of the detector angular acceptance, the Cherenkov light directionality, and since only the first
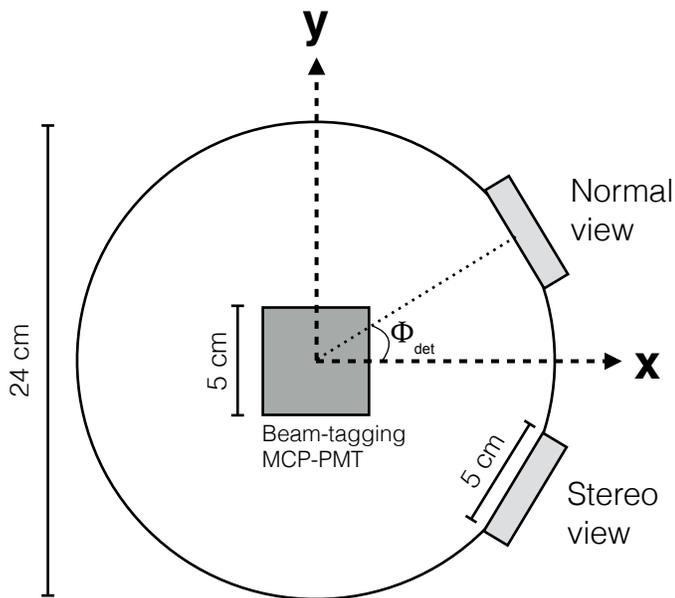
Figure 2.1: Rear-view scale drawing of OTPC detector showing the normal and stereo MCP-PMT mounting positions. The normal and stereo mounted PMs are bisected by the x-axis in the OTPC coordinate system by an angle Φ_{det} of 32.5°. The beam comes out of the page in the +z direction
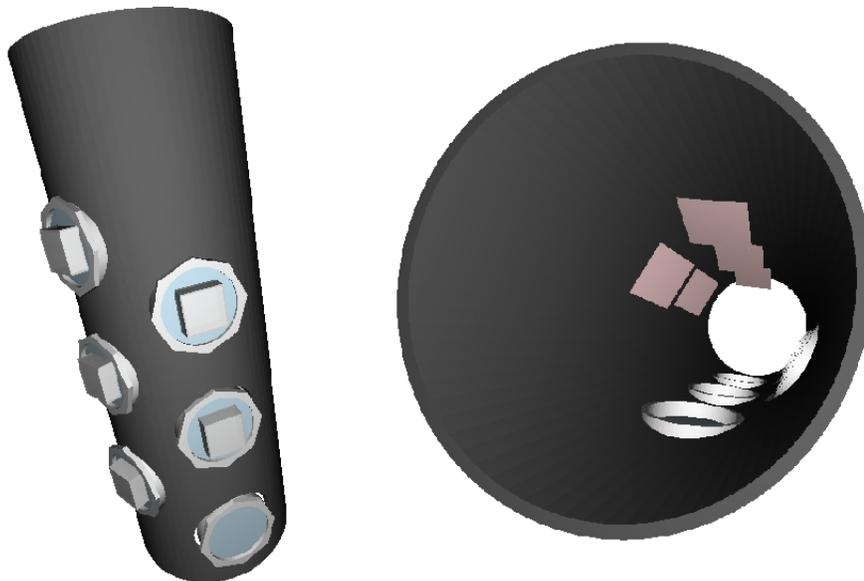
Figure 2.2: Two renders of the OTPC detector made using Chroma [29]. On the left is a side view that shows the water tank with the PM ports mounted in the normal and stereo views. The right is a view down the center of the detector tank and the mirrors (red) mounted in the inner volume.

9

132 five the ports are instrumented, the effective fiducial volume is limited to roughly the top
133 two-thirds of the total volume. This sets the OTPC fiducial mass of $\sim$27 kg.

2.2 Detector Optics

135 With low-timing jitter and high granularity MCP-PMTs, the water chromaticity and scatter-
136 ing properties become important as the distance from track to photo-detector increases. How-
137 ever, we can ignore these effects due to the prototype-OTPC short drift lengths ($<$30 cm),
138 we can assume $v_{\gamma_2} = v_{\gamma_1} = < v_{group} >$. The path length difference depends on the emittance
139 angle, $\theta_c(\omega)$ and the particle angle, θ_i. Again considering the dispersion effects negligible in
140 this application, $\theta_c(\omega) = cos^{-1}(\frac{1}{\beta<n>})$ and is constant.

141   Consider a particle traveling through the OTPC as shown in Figure 1.3, but further
142 generalizing the track by allowing a polar angle, θ_i, with respect to the z-axis in the plane.
143 Two Cherenkov photons generated along the particle path generated at $t = 0$ and $t = t_0$ are
144 detected with a relative time and position of $\Delta t_{\gamma 21} = t_{\gamma_2} - t_{\gamma_1}$ and $\Delta z_{\gamma 21} = z_{\gamma_2} - z_{\gamma_1}$. The
145 relative timing is given by

$$\Delta t_{\gamma 21} = t_o + (\frac{L_{\gamma_2}}{v_{\gamma_2}} - \frac{L_{\gamma_1}}{v_{\gamma_1}}) = t_o + \frac{\Delta L_{\gamma 21}}{< v_{group} >} \tag{2.1}$$

146 where $\Delta L_{\gamma 21}$ is the path length difference and $< v_{group} >$ is the weighted average of the
147 group velocity over the optical range of the detector. The experimentally measured time
148 projection and z-projection in terms of the track variables

$$\Delta t_{\gamma 21} = t_o \, (1 - \frac{\beta \, c}{< v_{group} >} \, \tan \theta_i) \tag{2.2a}$$

149

$$\Delta z_{\gamma 21} = \beta \, c \, t_o \, \cos \theta_i \tag{2.2b}$$

150 A useful relation is the ratio of the time-projection to the z-projection. The ratio over an

infinitesimal track length is

$$\frac{dt}{dz} \approx \frac{1}{\beta\,c} - \frac{\tan\theta_i}{<v_{group}>} \qquad (2.3)$$

for small angles along a path parallel to the detector plane.

The OTPC drift speed in Eqn. 2.3 is given by $<v_{group}>$. In a electron-drift TPC, the first term in Eqn. 2.3 is negligible due to the relatively slow drift speeds[1], and dispersion thereof, compared to that of the charged particle. In an OTPC, the photon velocity is comparable with the particle speed in the lab frame enabling the potential to measure β along the track. The first term, $1/\beta\,c$, in Eqn. 2.3 is equivalent to $\frac{\cos\theta_c}{<v_{phase}>}$.

An additional set of photons is detected at each MCP-PMT from a mirror mounted on the opposite side of the inner cylinder as shown by γ_3 in Figure 1.3. This not a specific feature of an OTPC, but is used to increase the the limited photocathode coverage.Each mirror is mounted at an angle, θ_{mirror} of 90°-θ_c. For a small range of particle angles, the mirror creates a time-delayed image of the Cherenkov light on the opposing wall at the MCP-PMT.

The discrete mirror positions offer a handle on the longitudinal track location across a single MCP-PMT by using the measured time difference between the direct and mirror-reflected Cherenkov light. The displacement, r, from the OTPC center-line is given by

$$r = \frac{\tan(\theta_c)}{2}\, \frac{\Delta t_{mirror} - D/<v_{group}>}{\frac{1}{<v_{group}>\cos\theta_c} - 1/\beta c} \qquad (2.4)$$

where Δt_{mirror} is the measured time difference at the MCP-PMT and D is the inner cylinder diameter.

2.2.1   Optical properties of detector components

The transmission, reflection, and spectral efficiency of the various OTPC components define the energy bandwidth and quantity of Cherenkov light photons detected. The indices of

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1. For a liquid argon TPC of the electron drift speed is on the order of a few $mm/\mu s$: $(v_{drift}/c \sim 10^{-5})$ [31]

Table 2.1: Indices of Refraction of the OTPC optical coupling from the water volume to the MCP-PMT photocathode.

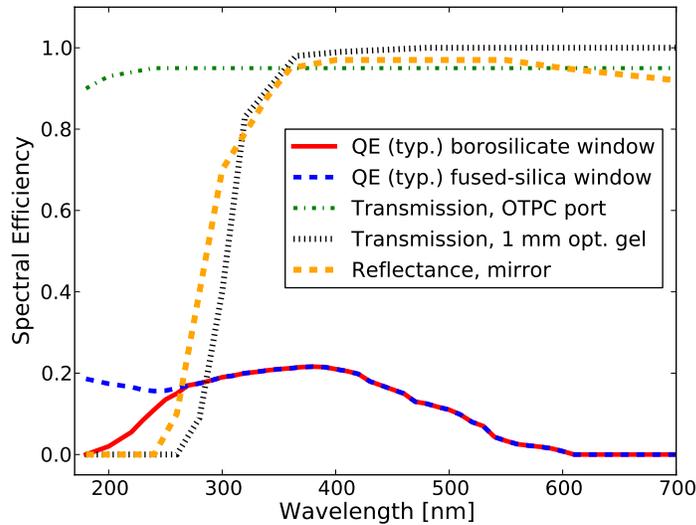| Volume	Thickness	n at 400 nm
DI H_2O	n/a	1.34
Fused silica port	3.175 mm	1.47
Optical coupling gel	$\sim$1 mm	1.47
MCP-PMT fused silica window	<2 mm	1.47
MCP-PMT borosilicate window	<2 mm	1.51

Figure 2.3: Optical properties of the OTPC optical components over wavelength range of 200 to 700 nm. These parameterizations are used to model the optical properties in the Chroma OTPC simulation.

refraction encountered by the light path from the water volume to the MCP-PMT photo-cathode are shown in Table 2.1. Losses from reflection due to polarization at the water-fused silica port interface are minimal. In fact, the direct in-plane polarized Cherenkov light hits the window near the Brewster angle for small-angled tracks. An optical coupling gel is used to prevent total internal reflection at the OTPC port and phototube window interface.

The properties of the detector components over the optical and near-UV range is shown in 2.3. The data are taken from the various manufacturers [18, 30]. Despite efforts to capture as much near-UV Cherenkov light as possible by using fused-silica components, the optical coupling gel cuts off these wavelengths. Not shown is the light absorbing paint, which was modeled with a broadband 95% absorbance and a 5% diffuse reflectance. These properties were used to parameterize the surfaces in the Chroma detector simulation.

2.2.2   Optical quality of water

The optical quality of the OTPC water volume is notably poor, but isn't too much of a limitation for short photon path lengths. Measuring 1-cm-deep samples with a spectrophotometer at various post-fill intervals, we measured the water attenuation length as shown in Figure 2.4. Compared to a pure water standard, the absolute absorbance at over the 300-500 nm range is 50 to 100 times worse[2].

This can be attributed to several factors. One, there is no filtration system to remove particulates in the volume. Second, in the 12 hr and 60 day measurements a noticeable degradation in the near-UV part of the spectrum was observed. This is likely attributed to UV stabilizers in the PVC enclosure leaching into the water [33]. In any case, data presented are from runs in which the optical quality was at or better than the 6 hr attenuation curve. With a $1/e$ attenuation length > 0.5 m at 300 nm, the longest path lengths in the OTPC are $\sim$0.3 m.

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2. Also compared with the Super-K experiment, which regularly measures attenuation lengths of 100 m in the 350-500 nm range [32]
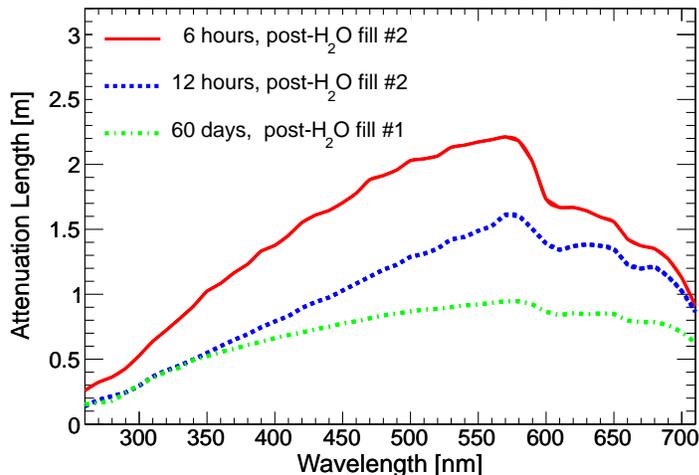
Figure 2.4: Calculated attenuation length of the OTPC water samples over a wavelength range of 250 to 720 nm using data obtained from dual-beam spectrophotometer measurements.

2.2.3   Detector Monte Carlo

A detector simulation was created for the OTPC using Chroma [29], In this simulation, the water volume, geometry, and optical properties of the OTPC components are fully modeled from data presented in previous sections. In the top frame in Figure 2.5, the ideal OTPC responses two 1 GeV muons entering the detector at the same point, but at different angles, are shown. The direct and mirror reflected hits at each of the 5 photo-detector modules are visible, separated by ~800 ps. The entire event occurs in about 2 ns.

The bottom frame shows the linear-fit residuals when fitting the direct Cherenkov light at each photo-detector from the straight-going ($\theta = 0°$) muon. Before fitting, the data were smeared with (optimistic) 20 ps timing errors.

2.3   Photodetector Module

The OTPC is instrumented with five Photodetector Modules (PM), which provide the photon detection, signal readout, analog-to-digital conversion, and send data packets to the upstream system. The PM components are discussed in detail in the following sections:

14
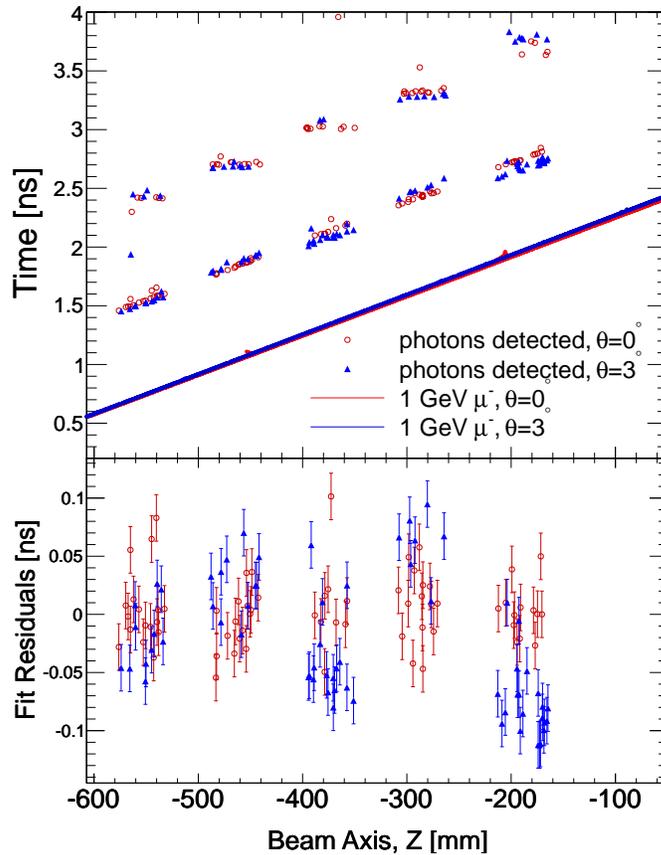
Figure 2.5: Two 1 GeV muons simulated in the fully modeled OTPC detector using Chroma. The muons enter the OTPC water volume at the same position, but with angles (θ, ϕ) of red: (0,0) and blue: (3,3) degrees. For clarity in demonstrating the operation principle, the OTPC detected photon response in the upper frame assumes a perfect resolution. Fitting the direct Cherenkov light for the (0,0) muon track after smearing the time response at 20 ps, the linear residuals are shown in the bottom frame.

210 Section 2.3.1 covers the commercial Planacon MCP-PMT and its transmission line anode 211 readout. Section 2.3.2 discusses the readout electronics system built around the PSEC4 212 waveform digitizing ASIC. Results from characterization tests with a single-photon laser are 213 presented in §2.4.

214 *2.3.1   MCP-PMT and Anode*

215 The photo-detector used on the OTPC is the commercial 'Planacon' XP85022 MCP-PMT 216 device from PHOTONIS [18]. These square devices have a 5×5 cm^2 photo-active area 217 and an anode comprised of a 32×32 square pad array with a 1.6 mm pad pitch. The 3 218 MCP-PMTs mounted in the normal view are 25 μm MCP-pore-size tubes with fused silica 219 front windows manufactured in 2014-15. On the stereo view are 2 MCP-PMTs: One from the 220 same manufacturing run and another considerably older MCP-PMT with a borosilicate front 221 window. The latter MCP-PMT exhibited relatively inferior gain and detection efficiency.

222 While reading out each of the Planacon's 1024 anodes might provide the best-case gran- 223 ularity and pileup per channel, it is not a scalable nor an economical option when instru- 224 menting a detector with many such photo-detectors. Instead, we adopt a similar microstrip 225 readout scheme as the first-generation glass package LAPPDs [17, 34]. A thirty-two channel 226 microstrip anode PCB board was designed such that a column of 32 anode pads is mapped 227 to a single 50 Ω line. The characteristic impedance is determined by the layout geometry 228 and the dielectric properties [35]. Each microstrip line serves as both the DC return and the 229 high fidelity signal path for $\frac{1}{32}$ of the MCP-PMT. The board-mounted photo-tube is shown 230 in Figure 2.6.

231 The accelerated electron shower from the MCP will induce a transverse electro-magnetic 232 wave between the microstrip's signal and reference plane [3]. Once created, this wave will

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3. More accurately the microstrip mode is 'quasi-TEM' for frequencies > 0. When a wave is induced in the microstrip, the fields are no longer static and the wave propagates in both the dielectric region between conductors and the air gap above the signal conductor. This introduces longitudinal field components, which remain considerably smaller than the transverse fields [36].
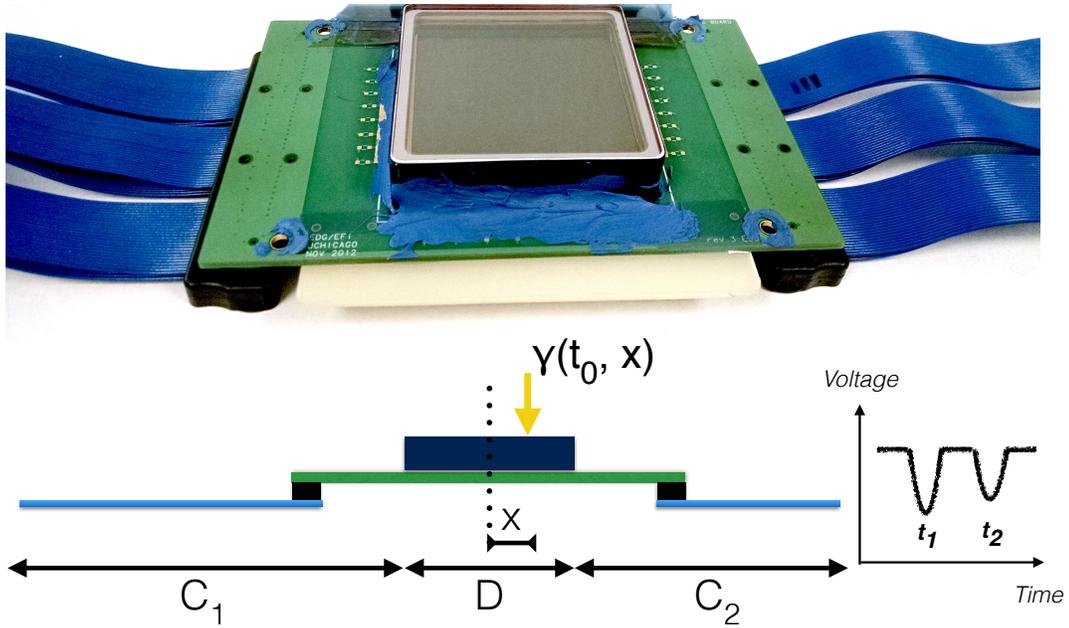
Figure 2.6: A PHOTONIS XP85022 Planacon MCP-PMT mounted on a custom thirty-two channel, 50 Ω transmission line anode board is shown in the top photograph. The Planacon has an anode of 1024 pads in a 32×32 array over the 5×5 cm^2 active area. These are mapped to the microstrip anode readout card in rows of 32. The bottom diagram outlines the technique for using the single-channel waveform timing to extract the incident photon (γ) position along the transmission line. The times of the direct and open-end reflected waves on the anode microstrip are denoted by t_1 and t_2.

propagate equally along both directions on the 1D microstrip. A set of 2 high-channel density coaxial cables bring these waveforms off the board. The readout strategy adopted for the OTPC is to digitize the waveform on the microstrip at only 1 anode terminal, leaving the other terminal open (high-Z). Thus, the wave that initially propagates toward the open-end will be reflected with the same polarity back along the transmission line towards the digitizer.

For a single photo-electron signal, the digitizer will record two transient waveforms along the microstrip. The times of the direct and open-end reflected waves, t_1 and t_2 can be extracted from these transients. Figure 2.7 diagrams this technique. Using the measured times we can solve for the incident photon position, x, and time-of-arrival, t_o. The measured times, t_1 and t_2 are expressed by

17

$$t_1 = t_0 + \frac{1}{v_{prop}} \left(\frac{D}{2} - x + C_2 \right) \tag{2.5a}$$

$$t_2 = t_0 + \frac{1}{v_{prop}} \left(\frac{3\,D}{2} + x + C_2 + 2\,C_1 \right) \tag{2.5b}$$

where D, C_1, and C_2 are the microstrip lengths of the MCP-PMT footprint, the reflected wave cable length, and the direct wave cable length respectively. The wave speed is v_{prop}. Solving these equations for x, the longitudinal position, and t_0, the photon hit time, yields:

$$x = v_{prop} \frac{t_2 - t_1}{2} - \frac{D + 2\,C_1}{2} \tag{2.6a}$$

$$t_0 = \frac{t_2 + t_1}{2} - \frac{1}{v_{prop}} (D + C_2 + C_1) \tag{2.6b}$$

The total length of the transmission line is $D + C_2 + C_1$. In many cases, the information of interest is the relative timing between photon hits allowing the constant term in Eqn. 2.6b to be dropped.

Practically, we use a 10" (25.4 cm) high density coaxial cable to provide delay for the reflected signal and an identical 6" (15.2 cm) cable to connect the microstrip card to the waveform digitizer board. The micro-coaxial cable has a a propagation delay of 4.265×10^{-3} ns/mm with corresponding per-unit length RC characteristics of 0.381 mΩ and 0.089 pF [37]. These lossy transmission line properties attenuate the further traveled reflected wave with respect to the direct waveform.

2.3.2   Front-end data acquisition

The waveforms on the anode microstrip of each PM are digitized at 10.24 Gigasamples-per-second (GSPS) using the ACquisition and Digitization with pseC4 (ACDC) card. This card

18

Figure 2.7: The OTPC front-end: the ACquisition and Digitization with pseC4 (ACDC) card. The ACDC card is a 30-channel waveform digitizing board using the waveform-recording PSEC4 ASICs running at a sampling rate of 10.24 GSPS. A 1 GHz 20 dB voltage amplifier card is plugged in the mezzanine slot and the MCP-PMT signal is plugged into the board-to-board slot furthest on the right.

uses 30 channels of the PSEC4 ASIC with an analog bandwidth $\geq$ 1 GHz [38][4]. The digitized waveforms from the PSEC4 chips are sent to an on-board FPGA, which buffers the digital data. Serial communication and data readout to the system DAQ is performed over a dual CAT6 LVDS link. The ACDC board is pictured in Figure 2.7.

The PSEC4 has a signal voltage range of 1.1 V digitized in 10.5 bits above noise. To fully exploit this dynamic range, a calibration look-up-table for each switched capacitor sample cell is required. However, for small signals that cover less then 50% of this range, the raw ADC count PSEC4 output deviates less then 1% from linearity. This error is acceptable since the typical single p.e. signals are less than 200 mV. A pedestal voltage of 0.8 V is set for the OTPC data runs, allowing ample headroom for negative polarity pulses.

The ACDC runs off a 40 MHz clock that is distributed to the 5 PSEC4 ASICs and

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4. This reference is included and supplemented in Appendix A

Table 2.2: Coarse DNL time-base calibrations for the PSEC4 ASIC. The wraparound is the PSEC4 time-step from sample 255→sample 0.

Time step Δt_n	Value [ps]
[0,254]	96.5
255	393.3

FPGA using an on-board jitter cleaning PLL chip[5], This clock is up-converted in PSEC4 ASIC using a voltage-controlled delay line (VCDL) to achieve a 10.24 GSa/s sampling rate over 256 sample cells. Though an enabling and power efficient means of garnering high sampling rates, the time-steps in a VCDL-controlled switch capacitor array are non-uniform due to process variations in the integrated circuit fabrication. Calibrations of the time-base in the PSEC4 and related CMOS chips are discussed in Refs:[38, 39, 40, 41].

There are two sources of error in the PSEC4 times-base: the differential non-linearity (DNL), the and the integral non-linearity (INL). The DNL is the cell-to-cell time-base variation from the nominal time-step and the INL is a measure of the aggregate deviation over many sampling cells. In this application, we apply a crude calibration that considers the average DNL over the PSEC4 time-base as shown in Table 2.2. The time-steps between sampling cells are defined as $\Delta t_n := t_{n+1}$ - t_n. In this inexact, but expeditious calibration the sampling step is assumed to be uniform over the first 255 cells. The PSEC4 'wraparound' is considered separately and has a much larger time-step.

The OTPC has 5 PM modules and a trigger module that are read out with an ACDC card, for a total of 180 PSEC4 channels. A mezzanine 20 dB pre-amp board is used on the 5 PM ACDC boards to bring the MCP-PMT single p.e. signals to a trigger-able amplitude. The front-end boards are plugged into 2 central system cards, which distribute the clock and buffer the data from the ACDC cards. Interfacing with a linux PC in the beam enclosure, the central cards communicate over a parallel USB 2.0 protocol.

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5. TI CDCE62005 clock generator/jitter cleaner
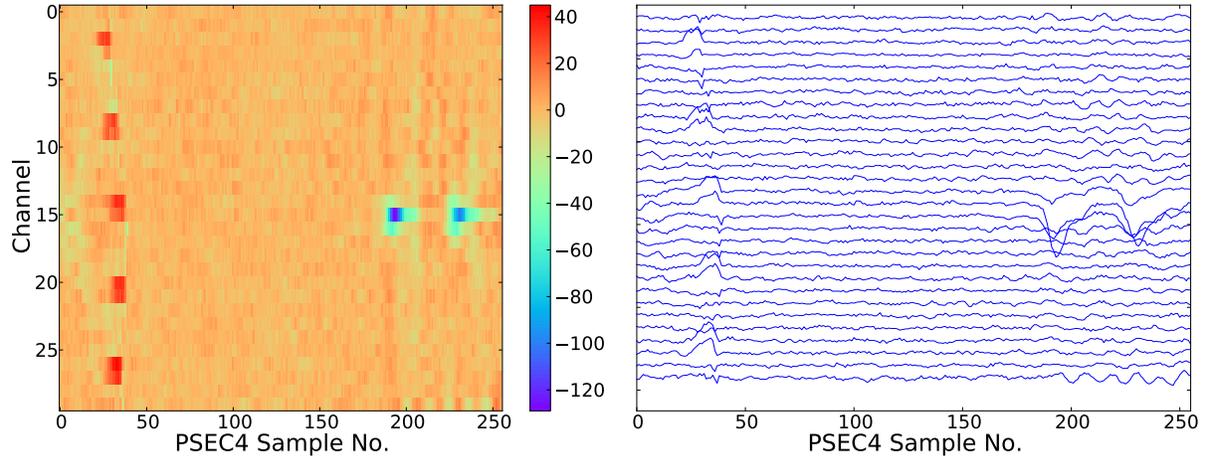
Figure 2.8: Single photo-electron recorded by the PM using a pulsed laser. The left figure shows the ACDC channel vs. PSEC4 sample number with the color indicative of the digitized value in PSEC4 ADC counts and the corresponding PSEC4 waveforms are shown on the right. This shows typical single p.e. system response, in which the 2 peaks are the direct and reflected pulses on the anode microstrip.

2.4   Single photo-electron response

A laser test-stand was built to characterize the single photo-electron (p.e.) response of the PMs. A 405 nm PiLas laser was used in pulsed mode, which can achieve pulse widths of 33 ps FWHM [42].

Single-photon

In the single photon mode, an iris is placed on the free-space output of the PiLas optical head, which picks off a 1 mm diameter portion of the beam. The iris is place a few mm off the incident beam axis in order to pick up a ∼0.5 attenuation fraction. Following the iris is an optically thick neutral density filter to attenuate the beam to the single-photon level. The single photon collection mode is corroborated by the data set statistics: ∼5% of the events recorded have a laser-correlated signal.

Figure 2.8 shows the PM response to a single p.e. Typical signals are on the order of 100 PSEC4-ADC counts (∼25 mV) for the first pulse and somewhat less for the time-lagged
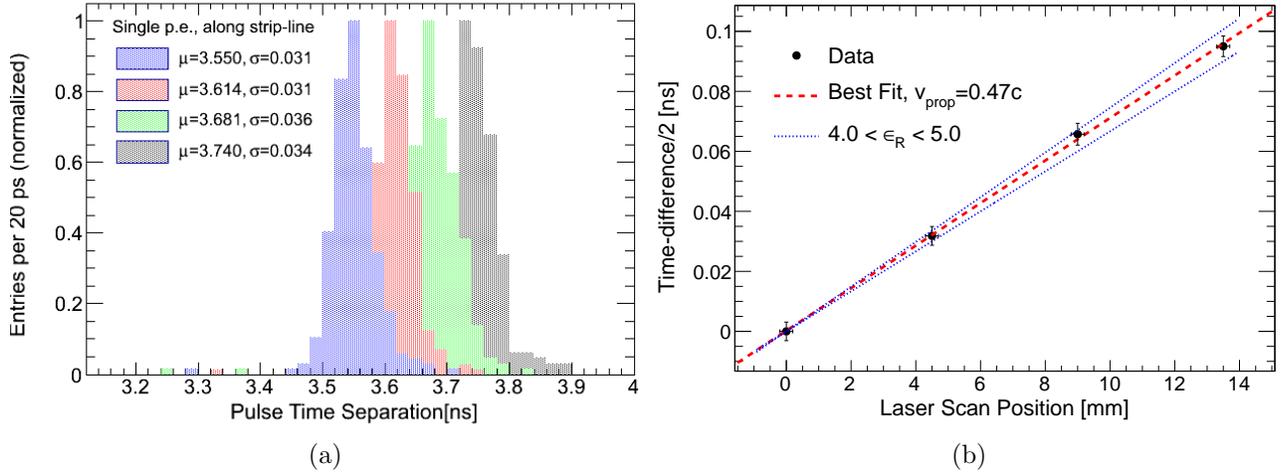
Figure 2.9: (a) Fitted time-difference along the MCP-PMT using the autocorrelation and waveform fits. The 1 mm diameter laser beam was scanned across the MCP-PMT surface, parallel to the microstrip direction, at 4 points separated by 4.5 mm. The resolution is ~35 ps. (b) Fitting for the propagation delay along the microstrip line, using data from (a). The error bars are multiplied by 2 for visibility. The data agree with the expected velocity given the typical relative permittivity of an FR4 printed-circuit board substrate (~4.3).
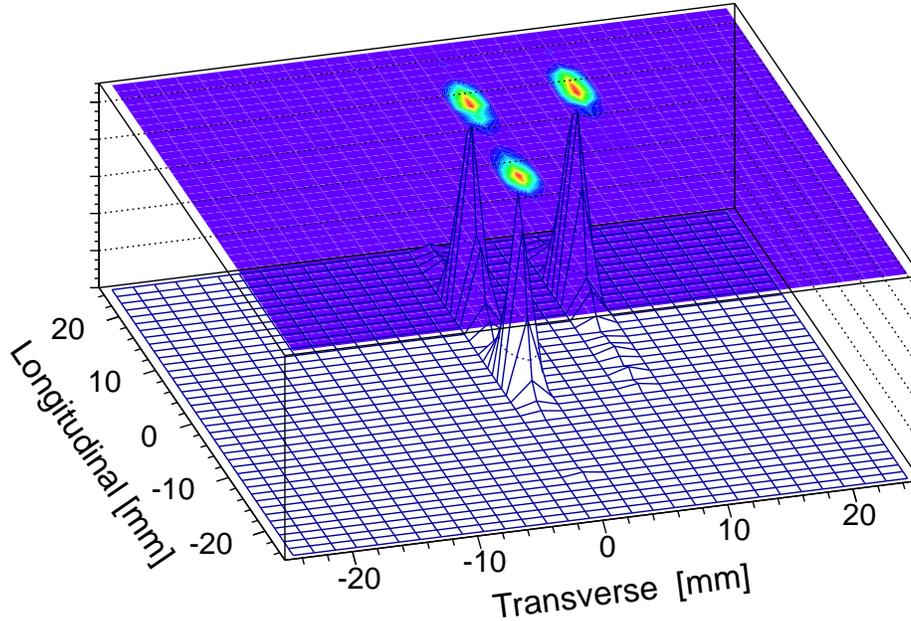
Figure 2.10: Reconstructed position of 3 single p.e. laser spots on the MCP-PMT active area of 5×5 cm^2. The longitudinal position is reconstructed by the time-difference along the microstrip line with a resolution of ~3 mm. The transverse position is reconstructed by taking the weighted average of the waveform autocovariance at zero-lag between 3 adjacent striplines. With this method, the transverse resolution is sub-mm

pulse due to the additional resistive attenuation. There is a 20 dB pre-amp board on the ACDC input so the unconditioned single p.e. MCP-PMT signals are typically between ∼2-5 mV.[6] Also visible in the figure is an apparent synchronous line in many channels near the beginning of the recording window. This is the time at which the PSEC4 is triggered.

The single p.e. position resolution is obtained by scanning the laser beam on the PM's active area both parallel and transverse to the microstrip direction. Results from a scan along the microstrip direction are shown in Figure 2.9. Four data points were taken at a spatial separation of 4.5 mm. The direct and reflected waveform time-difference is histogrammed for different points in Fig. 2.9a, which shows a resolution of ∼35 ps. This is the inherent electronics timing resolution for the single p.e. pulses and the resolution error is most likely dominated by the time-base INL, which is left uncalibrated.

Figure 2.9 shows the time difference along the microstrip vs. the laser beam position, allowing the signal propagation velocity in Eqn. 2.6 along the microstrip to be calculated. The best fit v_{prop} is found to be $0.47\,c$.

The spatial resolution transverse to the microstrip lines can be pushed to sub-mm levels using charge centroiding between channels [12]. In this application, we conservatively use the strip pitch for this value, ∼2 mm. Figure 2.10 shows the distinct separation and resolutions of 3 laser beam spots on the PM, demonstrating the principle of using the MCP-PMT as a multi-pixel photosensor.

Multi-photon

A similar test-stand setup is employed to measure the relative timing between single photons within the same laser pulse. In this setting, the iris is re-aligned with the laser beam axis, and a 10 mm focal length convex lens is put in the laser path. The MCP-PMT sits 30 cm behind the lens, which projects an elliptical laser beam spot over the MCP-PMT active area.

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6. Measurements with the LAPPD MCPs have demonstrated gains $\geq 10^7$, which give single p.e. signals ten-times as large into the same 50 Ω anode [43].

330 A neutral density filter is installed after the lens to attenuate to a ∼few photons per pulse.

331 Events are analyzed that have 2 recorded p.e.'s, in which the are clearly separated between

332 channels above and below the MCP-PMT center-line. ACDC recorded waveforms from one of

333 these events is shown in Figure 2.11a. Using waveform recording allows a range of algorithms

334 to best extract the timing information. It has been shown that full template fitting or cross-

335 correlation provides the best resolution [12, 41, 44]. In this test, the waveforms are fitted

336 using a Gaussian function covering the rising edge and the pulse peak.

337 The resultant relative timing between photons is shown in Figure 2.11b. A tail is seen

338 in the distribution, which is likely caused by optical reflections in the test setup that are

339 recorded late. The core resolution is shown to be 105 ps, which corresponds to a single p.e.

340 PM resolution of 75 ps. Again, a full calibration of the ACDC timebases across all channels

341 would certainly reduce the contribution from the electronics to this error.

342 From these measurements, we conclude that our 1-σ single p.e. time and space statistical

343 errors are $(\sigma_t, \sigma_x, \sigma_y) = (75$ ps, 2 mm, 3 mm$)$.
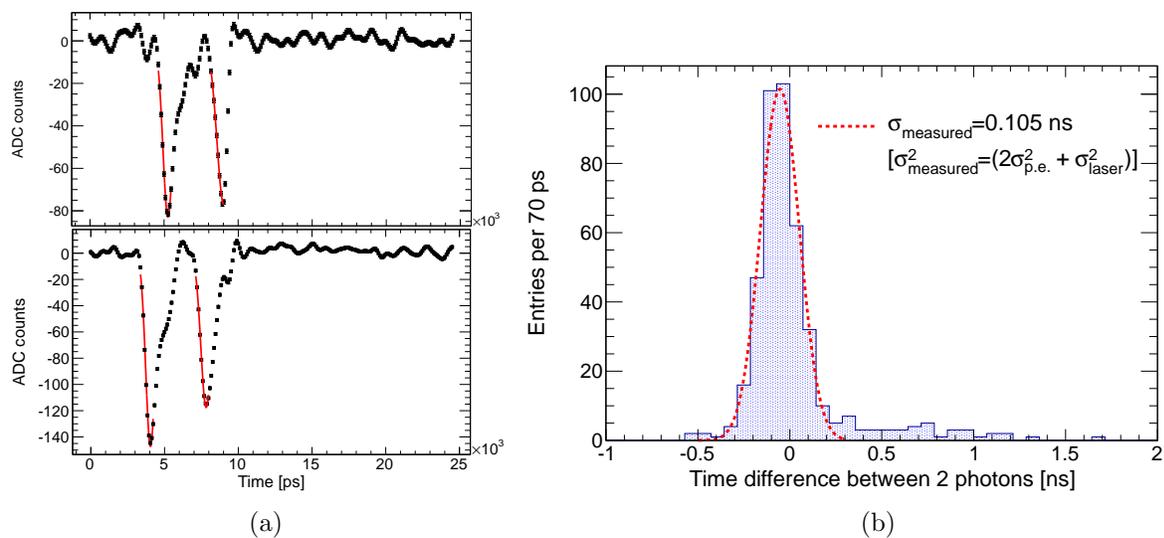
Figure 2.11: (a) The waveform fitting technique in the double-photon setup. This shows strip 10 (top) and strip 21, which were independently hit within the same laser pulse. The pulses are fit using a Gaussian function, from roughly 10% of the pulse amplitude on the leading edge to the 2nd sample point after the maximum pulse value. (b) The relative timing measurement between 2 photons on the PM. The underlying single p.e. electronics + MCP-PMT timing resolution for this measurement is 75 picoseconds.

CHAPTER 3

EXPERIMENTAL SETUP

In this chapter, we describe the experimental setup and beam-line simulations. The installation location and flux simulation of the Fermilab test beam are discussed in §3.1. Some of the OTPC operational configurations and related systematics are presented in §3.2. The OTPC trigger system is explained in §3.3.

3.1   MCenter Test Beam

The OTPC was installed ∼3 m behind a 1.09 m thick steel absorber that terminated the MCenter secondary beam line at the Fermilab National Laboratory Test-Beam Facility [45]. The absorber acts doubly as a collimator with a 13° off-axis slit and an anterior-mounted copper target oriented at the same angle. This generates the tertiary beam utilized by the LArIAT experiment, to which we operated parasitically [46].

A side view of the installed OTPC is shown in Figure 3.1 where the upstream absorber is out of the frame. The 5 OTPC PM modules are mounted facing inwards on the water volume. Each of the PMs are connected to the system central cards over 2 CAT6 network cables. The system cards interface to a remotely controlled linux PC on an adjacent rack that also houses the beam trigger coincidence and discrimination logic. High voltage (HV) is supplied to the detector from the counting room over ∼200 m SHV cables; the electronics' low voltage is supplied within the enclosure. The OTPC water volume is 2.1 radiation lengths along the cylindrical axis.

The beam is delivered to the Meson Lab during the 4.2-second slow-spill at the the beginning of the ∼60 second Fermilab Accelerator Complex 'super cycle'. The time structure is shown in Figure 3.2 as recorded during an acquisition run. During the OTPC test-beam runs, a secondary beam of positive pions was received on the MCenter target at momenta of 8, 16, or 32 GeV/c. Because of the OTPC location behind the secondary beam absorber,
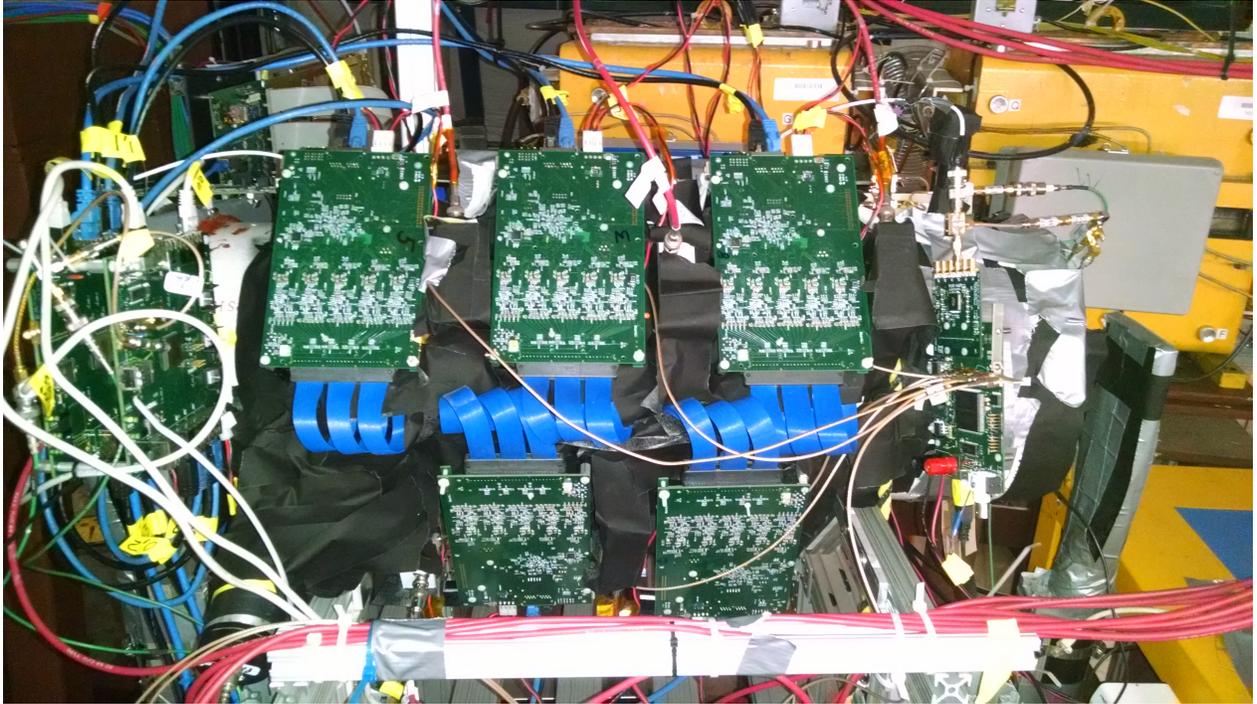
Figure 3.1: The OTPC mounted in the MC7 enclosure hall where the beam height is 208 cm. The upstream steel absorber block is out of the frame to the right. Mounted facing inwards, the 5 PMs connect to the system DAQ that is mounted on the left. The DAQ system connects to a remotely controlled laptop on an adjacent rack, which also houses the beam trigger coincidence and discrimination logic. The yellow dipole magnets on the adjacent tertiary beam-line are visible in the background.
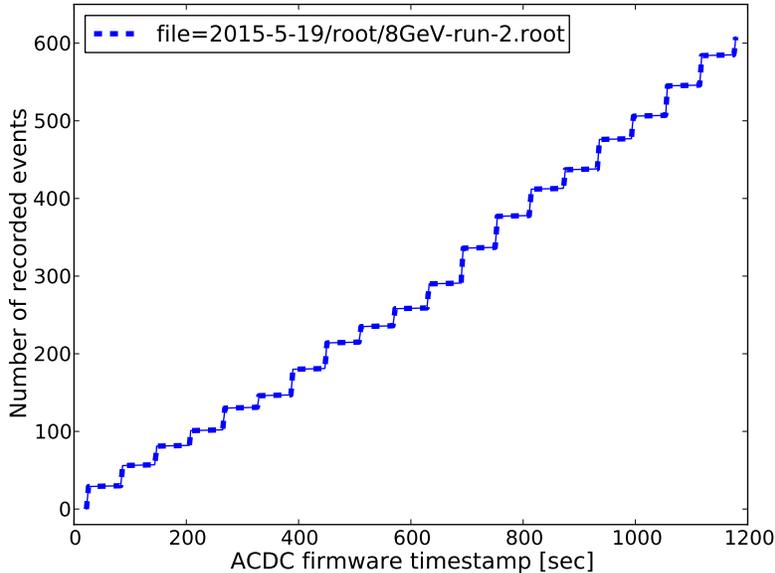
Figure 3.2: For a typical data acquisition, the number of events recorded to disk vs. the ACDC firmware timestamp from one of the front-end boards. The timestamp is registered with respect to the 40 MHz system clock. This acquisition was run for ∼20 min, which included 20 test-beam spills. The DAQ can acquire a maximum of 40-50 events per spill (<12 Hz). Saved in a compressed 'ROOT' format, each event is ∼70kB.

the flux and particle ID is not well defined.

A G4beamline simulation was written to understand the particle flux behind the absorber [47]. The copper target, steel block, and the OTPC water volume were included in the simulation. Two-million events were run, each starting with a 14 m long-π^+ beam to reproduce muons from pion decay-in-flight[1]. The results from the 16 GeV/c secondary momentum simulation are shown in Table 3.1, which represents particles whose trajectories would pass the OTPC beam trigger described in §3.3. Unsurprisingly, for a secondary beam of 16 GeV/c we expect primarily muons over a broad momenta range of:

∼[(16 - $dE/dx_{absorber}$)/2), 16 - $dE/dx_{absorber}$] GeV/c.

A variety of other particles, including multi-GeV pions, protons, with sub-GeV photons and $e^\pm$ are expected. At these momenta, pions will be indistinguishable by timing from muons over the OTPC length. Unless converting in the thin plastic scintillator that makes

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1. Supplemental details regarding the beamline simulation are included in Appendix B

Table 3.1: Simulated particle ID, count, and expectation value of total momentum, $<P_{tot}>$, at the OTPC location with a 16 GeV/c π^+ secondary beam. Particles with P_{tot} greater than 10 MeV/c were counted. (POT=π^+ on target)

PID	N/(10^6 POT)	$<P_{tot}>$	Note:
$\mu^\pm$	1200	10 GeV/c	broadband 7-14 GeV/c
$\pi^\pm$	150	8 GeV/c	peaked at 14GeV/c (16GeV/c - absorber dE/dx), otherwise scattered over 1-14 GeV/c
$e^\pm$	10	<1 GeV/c	
γ	60	<1 GeV/c	
p	<10	<4 GeV/c	

up the front coincidence trigger, the photons are not likely to pass the beam trigger. The opposite is true for showering $e^\pm$, which will may not toggle the back coincidence trigger. A limited TOF measurement ($\sigma \sim 100$ ps over 1 meter, discussed in §4.2) is possible with the trigger setup, which can potentially identify protons of several GeV/c or less.

During data taking, the MCenter count rate per test-beam spill varied between 4×10^4 and 1×10^5. Table 3.1 presents the expected the number of triggered events in a range of 20-50 test-beam spills.

Another aspect of the beam simulation was to provide an expectation on the number of simultaneous tracks within the OTPC. Assuming an RF bunch occupancy of either 0 or 1 particles, the track multiplicity expectation is shown in Figure 3.3. For each particle trajectory that passed the OTPC geometrical trigger cut, any other particle with momentum above 1 MeV/c that traverses the detector within the same simulated event was counted. We expect fewer than 1% of the events to have more than one track per trigger.

3.2   Operational Configuration and Timing Systematics

The MCP-PMT transit time from the photo-electric conversion at the photocathode to the signal generated on the anode varies with respect to the applied HV. Systematic timing differences between PMs will arise once the optimal HV conditions for each are set. This is particularly influenced by varying electron transit times in the MCP-PMT photocathode-to-
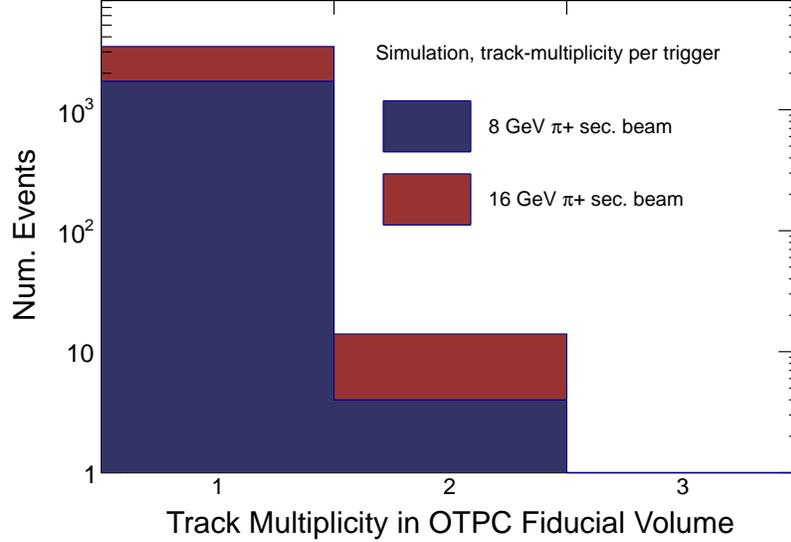
Figure 3.3: Simulated track multiplicity in the OTPC fiducial volume per triggered event. For both 8 and 16 GeV/c secondary π^+ beam, the number of tracks per pion-on-target was simulated.This was calculated by taking an event that passes the trigger cut and adding to it any additional tracks from that same event that passed through the OTPC.

top-MCP and bottom-MCP-to-anode gaps, in which electron(s) are accelerated in a uniform potential of 100's of volts from an kinetic energy of a few eV's over a distance of a several mm. In the Planacon MCP-PMTs used in this experiment, the photocathode gap ('K-gap') separation is 4.3 mm and the anode gap ('A-gap') is 3.0 mm [48].

A photo-electron produced in the photocathode is accelerated in a ∼straight path over a uniform K-gap potential. With this approximation, we ignore the photocathode emittance that contributes some angular dependence to the initial path condition. In the straight path case, the equation of motion of the non-relativistic photo-electron is given by

$$m_e \, \ddot{z} = q_e \, \vec{E} \cdot \hat{z} = q_e \, \frac{\Delta V}{d} \tag{3.1}$$

where m_e and q_e are the electron mass and charge, respectively. The K-gap electric potential and separation distance are represented by ΔV and d. Considering the initial photo-electron kinetic energy small enough to be negligible ($KE_i/KE_f \sim 0.01$), the transit time of the K-gap

30

Table 3.2: OTPC Photodetector Module (PM) operational voltages and corresponding MCP-PMT gap transit times. The photocathode gap (K-gap) and anode gap (A-gap) voltages are set using an external resistor divider circuit. The transit times for these gaps, T_{Kgap} and T_{Agap}, are calculated from Eqns. 3.2 and 3.3

PM No.	Total HV [V]	K-gap HV [V]	A-gap HV [V]	T_{Kgap} [ps]	T_{Agap} [ps]
0	2280	240±10	350±10	940±20	490±10
1	2910	395±20	410±20	730±20	450±10
2	2155	300±10	340±10	840±20	500±10
3	2190	310±10	340±10	820±20	500±10
4	2060	290±10	320±10	850±20	510±10

410 can be expressed as

$$T = d \sqrt{\frac{2\,m_e}{q_e\,\Delta V}} \tag{3.2}$$

411 An expression for the transit-time of the A-gap is not as straight-forward due to the physical

412 nature of the electron cloud showering from the bottom MCP. An expression for the time-

413 of-arrival, T_{max}, of an accelerated cloud of electrons across the A-gap arriving at the anode

414 has been solved using a ballistic (i.e. no interactions between electrons in the cloud) model

415 including non-zero initial radial and angular distributions [49]:

$$T_{max} = d\,\frac{\sqrt{2\,E_o\,m_e}}{q_e\,\Delta V}\,(\sqrt{1 + \frac{q_e\,\Delta V}{E_o}} - 1) \tag{3.3}$$

416 In this expression, d is the A-gap separation and E_o is the average initial electron kinetic

417 energy given by ∼3 eV, as specified by Ref. [49].

418   Using Eqns. 3.2 and 3.3, we can find the relative transit time differences between the

419 PMs as shown in Table 3.2. The systematic timing offsets between PMs are corrected by

420 subtracting from the ACDC digitized data the sum of transit times from both gaps. An

421 additional timing correction is applied by nulling relative trace lengths for different channels

422 on the ACDC and pre-amplifier board.

3.3 The Trigger

The OTPC trigger is created using 2 systems. The first is the beam trigger, which provides a coincidence signal of a thru-going particle. The second, level-0 (L0) trigger is done locally on each PM, which self-triggers on the detected Cherenkov photons on that particular MCP-PMT. This 2-level system is required when using the PSEC4 chip due to its relatively short analog memory. When running the PSEC4 at a sampling rate of 10.24 GSPS, the waveforms on the PSEC4 capacitor array are over-written in 25 ns intervals. The beam coincidence trigger decision requires a few hundred nanoseconds due to cable and electronic delays, which necessitates the fast L0 trigger to save these signals.

3.3.1 Beam trigger system

The beam trigger is a set of scintillator and Cherenkov detectors external to the OTPC water volume, as shown in Figure 3.4. A pair of $5 \times 5 \ in^2$ plastic scintillators are mounted fore (S_1) and aft (S_2) that provide good coverage over the OTPC cross-sectional area. A $1 \times 1 \ in^2$ active area, single-pixel MCP-PMT is mounted on the front cap of the OTPC and denoted as R_1. In the central region of R_1's active area is a small cylindrical (1 cm diameter) fused-silica radiator[2]. R_2 is a $2 \times 2 \ in^2$ MCP-PMT that is coupled to a matching 2 in square radiator[3]. It is mounted on the rear of the detector as also shown in Figure 2.1.

An additional set of PSEC4-based electronics is implemented on the OTPC to monitor the analog signals of S_1 and S_1, as well as to threshold discriminate R_1. This is done with a 6-channel PSEC4 evaluation card, which also serves to fan-out the R_1 trigger signal to the PMs as an unbiased L0 trigger signal. R_2 is read out and digitized in the same manner as the PMs, allowing spatial and time-tagging of the out-going particle. For each

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2. This was done in an attempt to use differences in pulse-height to distinguish particles that radiate in the MCP-PMT front window from those that traversed through the centrally-located cylindrical fused-silica radiator

3. R_2 is a borosilicate front-window PHOTONIS XP85022 MCP-PMT, which is same device used in the PMs. R_1 is a PHOTONIS XP85013 MCP-PMT, which has a different anode structure that is comprised of 64 pins. The R_1 signal is made by summing the central 32 pixels.
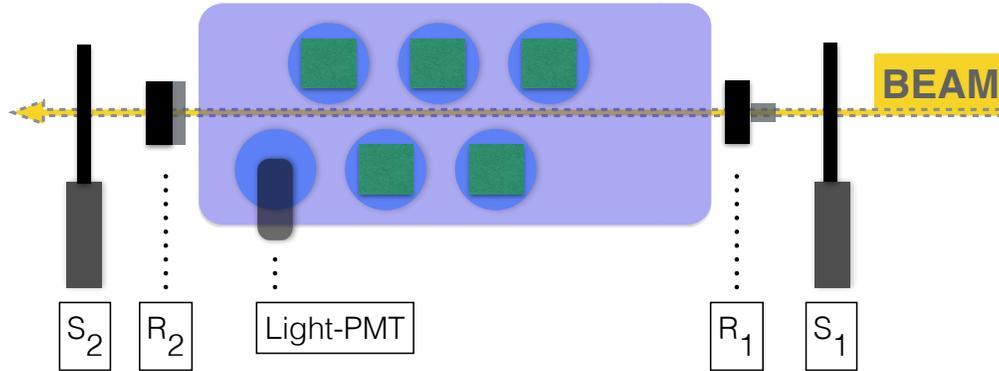
Figure 3.4: Diagram of the external trigger on the beam. The beam trigger coincidence can be made between four sub-detectors: the front and back scintillators+PMTs (S_1 and S_2), and the front and back fused-silica Cherenkov radiators+MCP-PMTs (R_F and R_B). An additional debug/trigger detector is generated by a 1" PMT mounted on the last OTPC port that can observe Cherenkov light in the water volume (*Light-PMT*).

event, the digitized signal from R_1 is recorded with those of R_2, allowing for a time-of-flight measurement as well.

The beam trigger signal is made with standard NIM rack electronics. S_1, S_2, and R_1 are discriminated and and fed to a coincidence unit. Two configurations were used during data runs: (1) $S_1+S_2+R_1$, and (2) S_1+R_1. Trigger configuration (1) is the default thru-going particle trigger. Configuration (2) allowed the recording of particles that may scatter, stop, or shower out within the water volume. Both digital trigger signals are sent to the OTPC DAQ.

3.3.2   Fast level-0 trigger

CHAPTER 4

DATASETS

The OTPC was installed on the MCenter test-beam for several months in the spring of 2015. Data was taken at secondary beam momenta of 8, 16, and 32 GeV/c during that time. The dataset properties presented here are from data runs triggering on thru-going particles (trigger configuration 1 as described in §3.3.1).

Section 4.1 presents the OTPC detection efficiency compared to simulation and channel-by-channel occupancies. Particle information from the beam trigger is shown in §4.2. Methods of waveform feature extraction are described in §4.3.

4.1 Efficiency, Occupancies, and Gain

The data presented are taken from 16 GeV/c secondary beam runs in which the optical water quality was at or better than the 6 hour curve in Figure 2.4.

4.1.1 Forming an event

An OTPC event is recorded using 180 channels 10.24 GSPS data in a time window of 25 ns. The first 150 channels are from the OTPC photodetector modules (PM) and the remaining 30 channels comprise the trigger information of R_1 and R_2, which are described in §3.3. The following procedures are run on these data before analyzing an event:

1. A pedestal calibration is performed for each sample cell in each PSEC4 channel as described in Ref [38][1].

2. The firmware time-stamps are checked on the front-end ACDC boards. If the time-stamps are not synced, the event is discarded.

---

1. Also described in the Appendix: A.4

Table 4.1: Signal selection thresholds for channels within each PM.

PM No.	Min. pulse (ADC counts)	Int. charge (pC)
0	50	0.30
1	35	0.22
2	55	0.32
3	50	0.30
4	50	0.30

3. Channel 179 is the digitized signal from R_1 and is used as a zero-time (t_0) reference. The data on all channels are shifted such that t_0 at sample cell 90. With this shift, the hits from the Cherenkov photons are now located in the first one-third of the 256 sample PSEC4 buffer.

4. A reference baseline level, created using median value of sample cells 200-255, is subtracted from each channel.

5. A time-base is constructed from the sample-steps using the coarse calibration shown in Table 2.2 using 97 ps time-steps per sample. The wraparound region is interpolated at the same 97 ps interval in order to have an evenly spaced time-base

6. The particle output position is extracted by fitting the R_2 data in channels 150-179, as described in §4.2. The data are then reduced to the 150 channels of the PMs.Tthe event is discarded if the trigger is poorly fit.

7. An event window is defined over the first 110 sample cells. The event is shrunk down to these data points, which encompasses a time window of ∼11 ns.

8. The data are digitally low-pass filtered using a 4th order butter filter at a -3 dB point of 800 MHz.

9. Channels below the signal thresholds defined in Table 4.1 are cut.

The signal threshold criteria are 2-fold. The first is a minimum pulse height given by the peak digitized PSEC4 value in the event time window. Second, there is a minimum
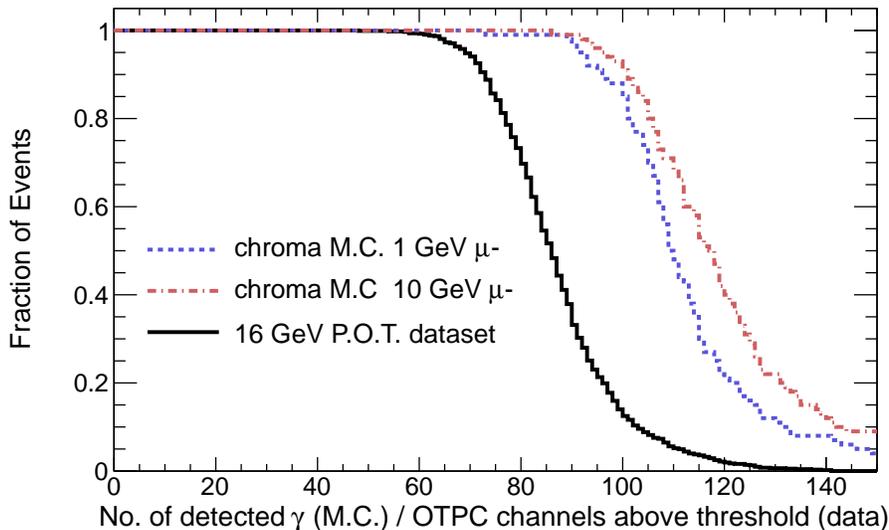
Figure 4.1: Fraction of events in which number of OTPC channels is above a defined single p.e. threshold. The threshold is a combination of minimum pulse height, integrated charge over a 11 ns waveform region.

requirement for integrated charge within the event window. The combination of the two aid in removing channels that are primarily cross-talk. A cross-talk signal may have a large amplitude, but a minimal deposited charge.

4.1.2   Photo-detection efficiency

The number of channels that passed the signal thresholds over a dataset of 1600 events is shown in Figure 4.1. Roughly 50% of the events have 80 or more channels above threshold per event. This is not a direct indication of the number of individual photons detected per event, but should be a decent proxy. Effects not included are over estimation due to charge-sharing between channels and under estimation from channels that may have 2 or more photon hits.

A comparison between data and the expectation from simulation shows a 20-30% detection ineffeciency compared to the Monte Carlo.
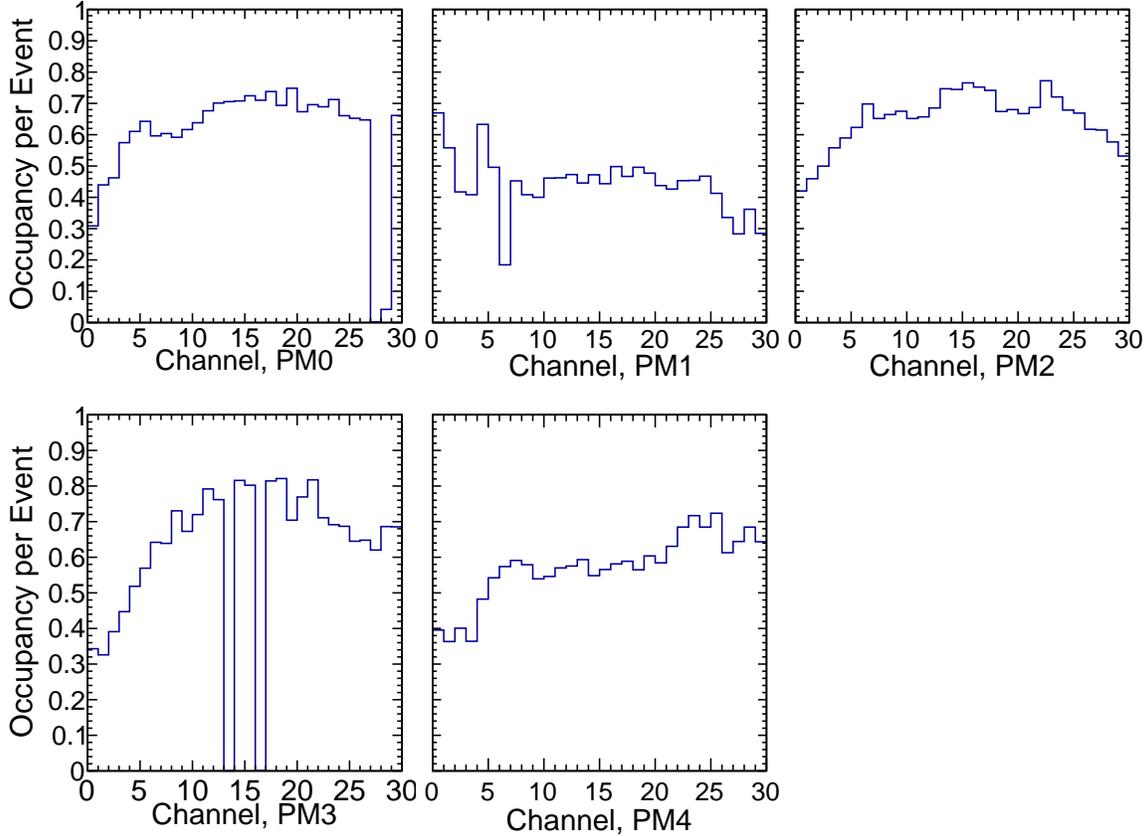
Figure 4.2: Per-event single p.e. OTPC channel occupancy.

4.1.3 Occupancy and Gain

Using the same dataset, we measure the occupancy and gain per OTPC channel. The number of signals above threshold per-event per-channel is shown in Figure 4.2. PMs 0 and 2-4 are the newer MCP-PMTs and PM 1 is an older model that shows a relatively less overall occupancy. A number of poorly coupled channels are visible in Fig. 4.2, which are cut from the dataset.

The gain per channel is shown in Figure 4.3, which is the multiplicative gain of the MCP-PMT and the 20 dB pre-amplifier board. This is measured by taking the median integrated charge for signals above threshold over the dataset. Error bars are taken to be the RMS of the integrated charge distribution per channel. MCP-PMT gains of about 10^6 are found for PMs 0 and 2-4, which is measured to be about twice the gain of PM 1. The gain on each
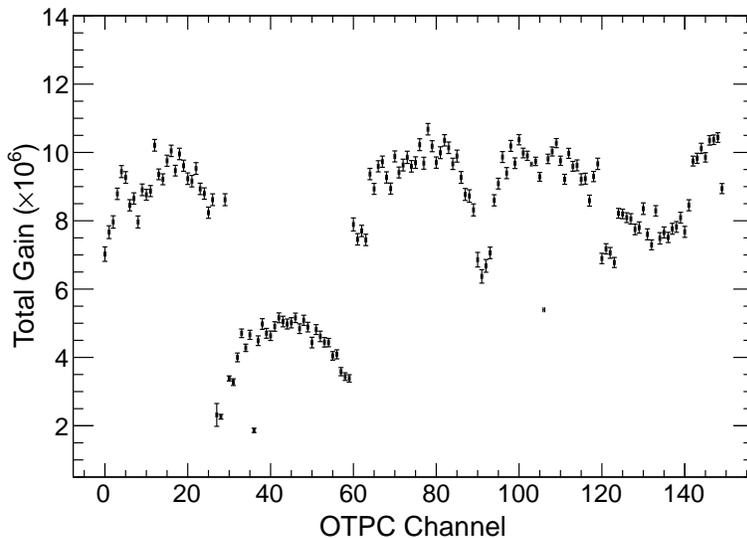
Figure 4.3: OTPC channel gain: MCP-PMT × electronics pre-amp gain.

channel is used to calibrate the number of detected photo-electrons per event.

4.2 Trigger Information

When triggering on thru-going particles, it is possible to reconstruct the position in which they leave the OTPC using the R_2 detector in the beam trigger (§3.3.1). The particle output position is extracted by fitting the R_2 signal on a 30 channel microstrip anode. A more detailed explanation of fitting the trigger signals is outlined in Appendix **??**. Figure 4.4 shows the reconstructed particle positions at the output of the OTPC for 8 and 16 GeV/c datasets.

A limited time-of-flight (TOF) measurement is also possible using the beam trigger. The relative timing between R_1 and R_2 for the 16 GeV/c dataset is shown in Figure 4.5. A resolution of 110 ps over a distance 0.9 m is measured for muons, pions, and possibly electrons passing through the detector. The front trigger detector, R_1, is the primary limitation of the TOF measurement due to the low-fidelity signal when wiring together the 32 anode-pads into a single pixel.
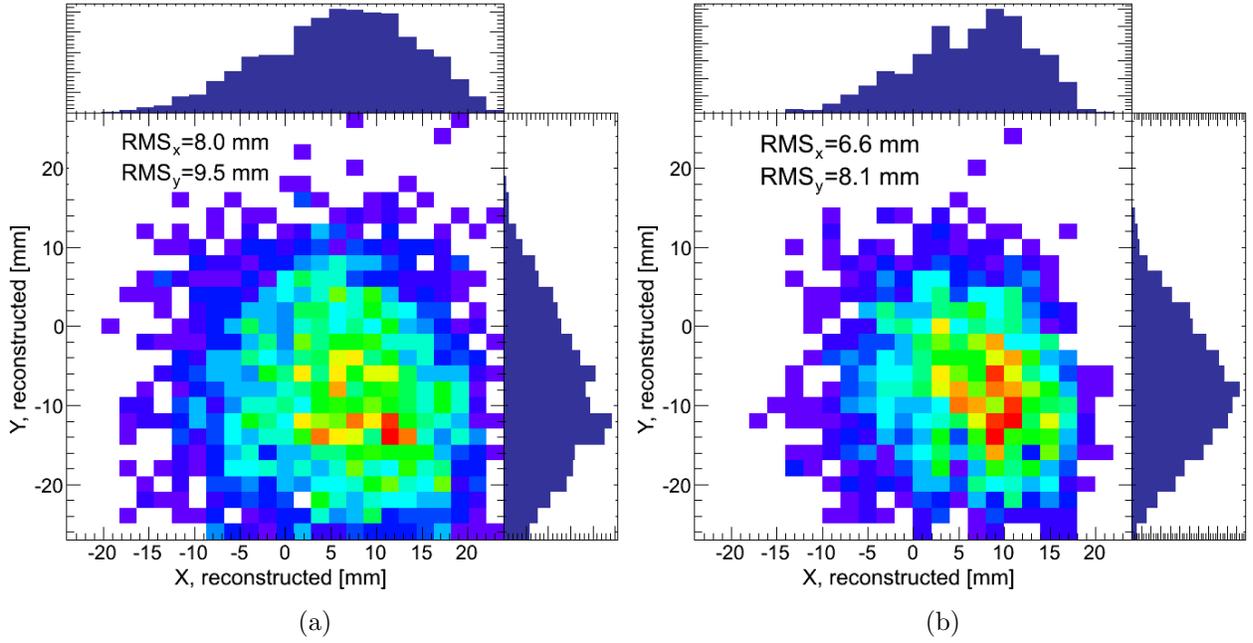
38

Figure 4.4: Reconstructed output particle position through the rear MCP-PMT+Cherenkov radiator for an (a) 8 GeV dataset and a (b) 16 GeV dataset. This MCP-PMT is part of the beam trigger system and is denoted as R_2 in Fig. 3.4 in the coordinate system defined in Fig. 2.1. The data is histogrammed in 2×2 mm^2 bins, where the Y direction is taken from the time difference along the anode transmission line and the X position is reconstructed using charge centroiding between microstrips.
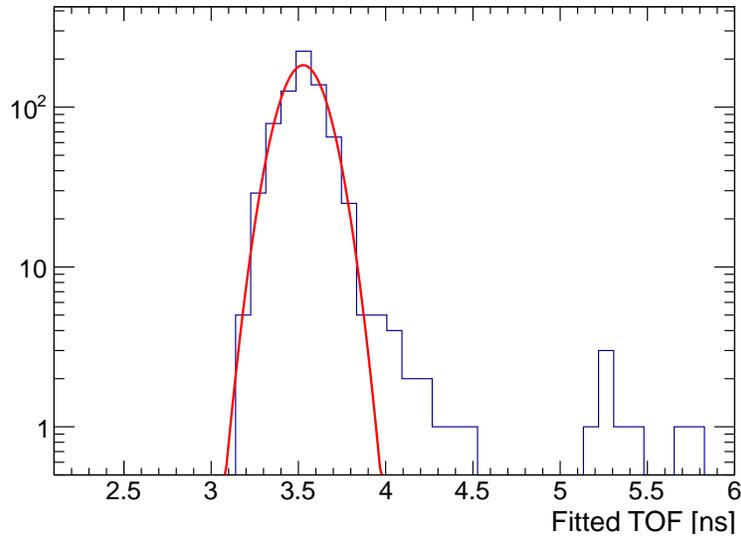

Figure 4.5: Measured time-of-flight using the beam trigger over 1k events in a 16 GeV/c dataset. The core resolution is 110 ps from the normal fit. Accidentals, or perhaps a few candidate protons (p < 2 GeV/c), are measured ∼1.5-2 ns slower.
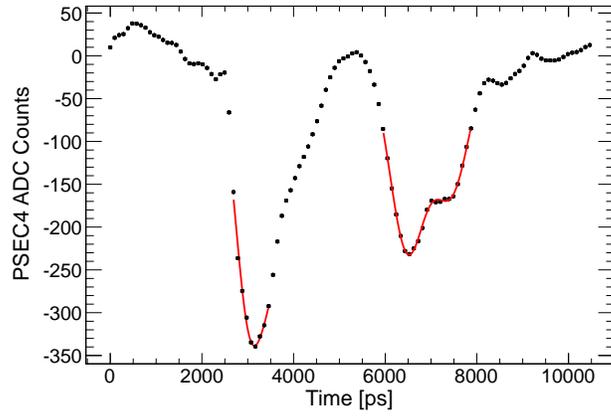
Figure 4.6: OTPC microstrip channel hit by two photons with 2 double-gaussian fits

4.3 Feature Extraction

40

Appendices

APPENDIX A

WAVEFORM SAMPLING & THE PSEC4 ASIC

The detection of discrete photons and high-energy particles is the basis of a wide range of commercial and scientific applications. In many of these applications, the relative arrival time of an incident photon or particle is best measured by extracting features from the full waveform at the detector output [44, 50]. Additional benefits of front-end waveform sampling include the detection of pile-up events and the ability to filter noise or poorly formed pulses.

For recording 'snapshots' of transient waveforms, switched capacitor array (SCA) analog memories can be used to sample a limited time-window at a relatively high rate, but with a latency-cost of a slower readout speed [51, 52]. These devices are well suited for triggered-event applications, as in many high energy physics experiments, in which some dead-time on each channel is acceptable. With modern CMOS integrated circuit design, these SCA sampling chips can be compact, low power, and have a relatively low cost per channel [52].

Over the last decade, sampling rates in SCA waveform sampling ASICs have been pushed to several GSa/s with analog bandwidths of several hundred MHz up to $\sim$1 GHz [39]. As a scalable front-end readout option coupled with the advantages of waveform sampling, these ASICs have been used in a wide range of experiments; such as high-energy physics colliders [39], gamma-ray astronomy [53, 54], high-energy neutrino detection [55, 56], and rare decay searches [57, 58].

A.1   Motivation for a new chip design

A natural extension to the existing waveform sampling ASICs is to push design parameters that are inherently fabrication-technology limited. Parameters such as sampling rate and analog bandwidth are of particular interest considering the fast risetimes ($\tau_r \sim$ 60 - 500 ps) and pulse widths (FWHM $\sim$ 200 ps - 1 ns) of commercially available and novel technologies of micro-channel plate (MCP) and silicon photomultipliers [43, 59, 60]. These and other fast

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photo-optical or RF devices require electronics matched to the speed of the signals.

The timing resolution of discrete waveform sampling is intuitively dependent on three primary factors as described by Ritt[1] [41]:

$$\sigma_t \;\propto\; \frac{\tau_r}{(SNR)\sqrt{N_{samples}}} \;=\; \frac{1}{(SNR)\,\sqrt{3 f_{sample}\, f_{3dB}}} \tag{A.1}$$

where SNR is the signal-to-noise ratio of the pulse, τ_r is the 10-90% rise-time of the pulse, and $N_{samples}$ is the number of independent samples on the rising edge within time τ_r. The sampling frequency and half-power bandwith are given by f_{sample} and f_{3dB}, respectively. The motivation for oversampling above the Nyquist limit is that errors due to uncorrelated noise, caused both by random time jitter and charge fluctuations, are reduced by increasing the rising-edge sample size. Accordingly, in order to preserve the timing properties of analog signals from a fast detector, the waveform recording electronics should 1) be low-noise, 2) match the signal bandwidth, and 3) have a fast sampling rate relative to the signal rise-time.

A.2   Introduction to PSEC4

We describe the design and performance of the PicoSECond-4 (PSEC4), a $\geq$10 Gigasample/second [GSa/s] waveform sampling and digitizing Application Specific Integrated Circuit (ASIC) fabricated in the IBM-8RF 0.13 μm complementary metal-oxide-semiconductor (CMOS) technology. This compact 'oscilloscope-on-a-chip' is designed for the recording of radio-frequency (RF) transient waveforms with signal bandwidths between 100 MHz and 1.5 GHz.

A.2.1   Towards 0.13 μm CMOS

The well-known advantages of reduced transistor feature size include higher clock speeds, greater circuit density, lower parasitic capacitances, and lower power dissipation per cir-

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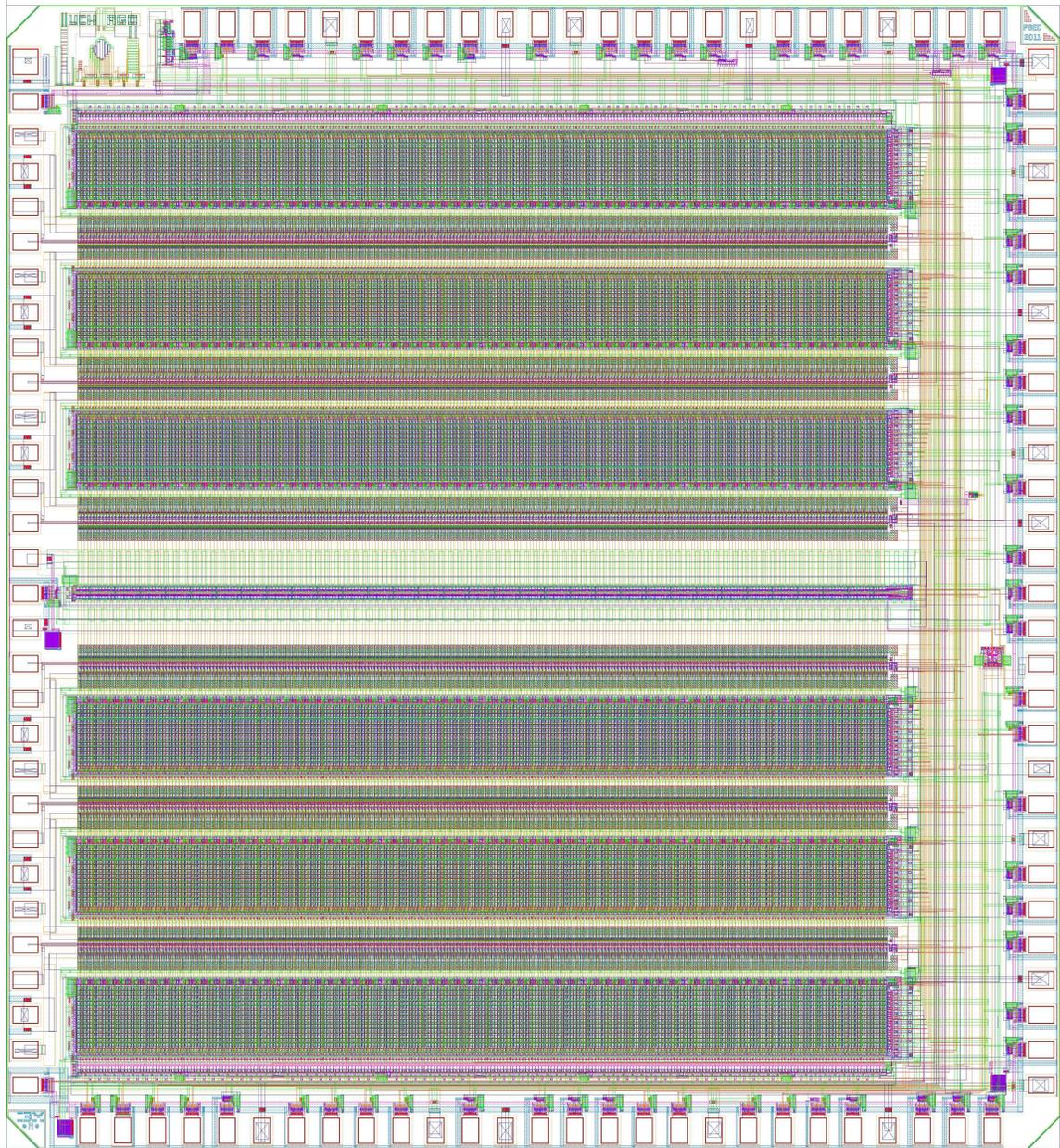1. Assuming Shannon-Nyquist is fulfilled

Figure A.1: The PSEC4 layout, as captured in the computer-aided design software. The layout is symmetric about the horizontal center-line, with 3 channels above and below. Along the center-line is the PSEC4 sampling and timing generator circuit. The chip dimensions are 4×4.2 mm^2. The 3 top, thick metal layers are not shown to allow a good view of the middle and lower metal layers, where the bulk of the circuitry is routed.

cuit [61]. The sampling rate and analog bandwidth of waveform sampling ASICs, which depend on clock speeds, parasitic capacitances, and interconnect lengths, are directly enhanced by moving to a smaller CMOS technology. Designing in a smaller technology also allows clocking of an on-chip analog-to-digital converter (ADC) at a faster rate, reducing the chip dead-time.

With the advantages of reduced transistor feature sizes also comes increasingly challenging analog design issues. One issue is the increase of leakage current. Leakage is enhanced by decreased source-drain channel lengths, causing subthreshold leakage ($V_{GS} < V_{TH}$), and decreased gate-oxide thickness, which promotes gate-oxide tunneling [62]. Effects of leakage include increased quiescent power dissipation and potential non-linear effects when storing analog voltages.

Another design issue of deeper sub-micron technologies is the reduced dynamic range [62]. The available voltage range is given by (V_{DD}-V_{TH}), where V_{DD} is the supply voltage and V_{TH} is the threshold, or 'turn-on', voltage for a given transistor. For technologies above 0.1 μm, the (V_{DD}-V_{TH}) range is decreased with downscaled feature sizes to reduce high-field effects in the gate-oxide [62]. In the 0.13 μm CMOS process, the supply voltage V_{DD} is 1.2 V and the values of V_{TH} range from $\sim$0.4 V for a minimum-size transistor (gate length 120 nm) to 0.2 V for a large-size transistor (5 μm) [63, 64].

The potential of waveform sampling design in 0.13 μm CMOS was shown with two previous ASICs. A waveform sampling prototype, PSEC3, achieved a sampling rate of 15 GSa/s and showed the possibility of analog bandwidths above 1 GHz [65]. Leakage and dynamic range studies were also performed with this chip. In a separate 0.13 μm ASIC, fabricated as a test-structure chip called CHAMP, a 25 GSa/s sampling rate rate was achieved using low V_{TH} transistors [66]. The performance and limitations of these chips led to the optimized design of the PSEC4 waveform digitizing ASIC. The fabricated PSEC4 die is shown in Figre A.1.

In this chapter, we describe the PSEC4 architecture (§A.3), and experimental perfor-

mance (§A.5).

A.3 PSEC4 Architecture

An overview of the PSEC4 architecture and functionality is shown in Figure A.2. A PSEC4 channel is a linear array of 256 sample points and a threshold-level trigger discriminator. Each sample point in the array is made from a switched capacitor sampling cell and an integrated ADC circuit as shown in Figure A.3.

To operate the chip, a field-programmable gate array (FPGA) is used to provide timing control, clock generation, readout addressing, data management, and general configurations to the ASIC. Several analog voltage controls are also required for operation, and are provided by commercial digital-to-analog converter (DAC) chips.

Further details of the chip architecture, including timing generation (§A.3.1) sampling and triggering (§A.3.2), analog-to-digital conversion (§A.3.3) , and data readout (§A.3.4), are outlined in the following sections.

A.3.1 Timing Generation

The sampling signals are generated with a 256-stage Voltage-Controlled Delay Line (VCDL), in which the individual stage time delay is adjustable by two complementary voltage controls. There is a single VCDL that distributes the timing signals to the entire chip. Each stage in the VCDL is an RC delay element made from a CMOS current-starved inverter. The inverse of the time delay between stages sets the sampling rate. Rates of up to 17.5 GSa/s are possible with PSEC4 as shown in Figure A.4. When operating the VCDL without feedback, the control voltage is explicitly set and the sampling rate is approximately given by

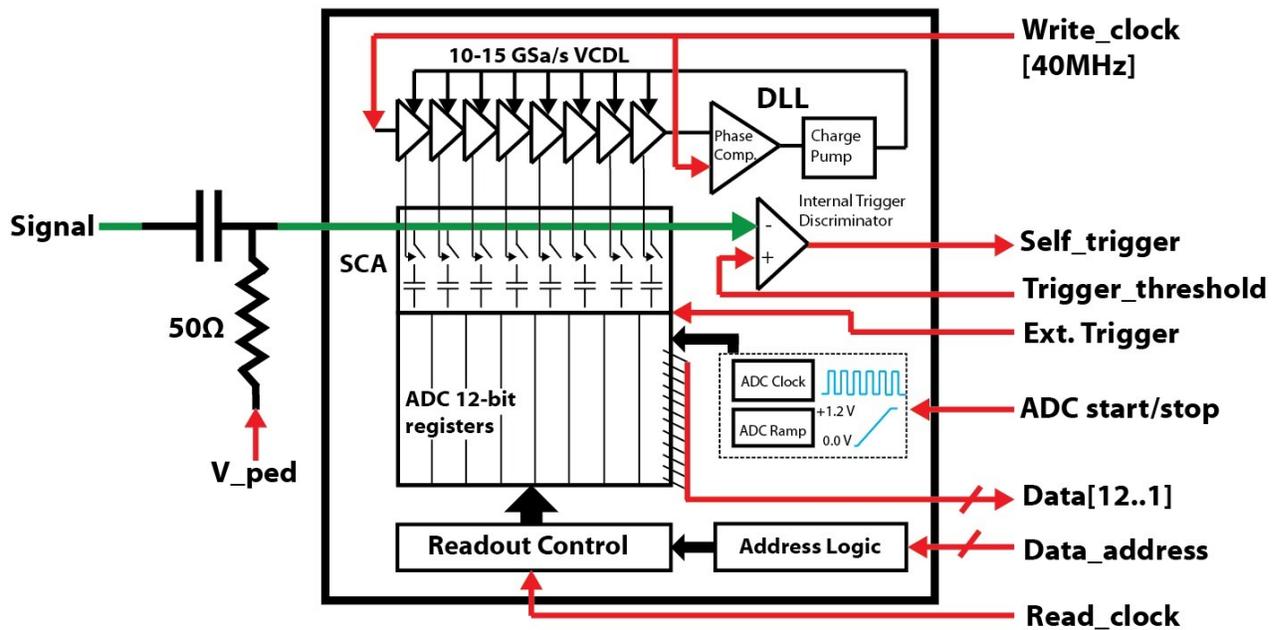$$18 - 0.3 \, e^{6 \cdot V_{control}} \ [GSa/s]. \tag{A.2}$$

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Figure A.2: A block diagram of PSEC4 functionality. The RF-input signal is AC coupled and terminated in 50Ω off-chip. The digital signals (listed on right) are interfaced with an FPGA for PSEC4 control. A 40 MHz write clock is fed to the chip and up-converted to ~10 GSa/s with a 256-stage voltage-controlled delay line (VCDL). (For clarity, only 8 of the 256 cells and 1 of the 6 channels are illustrated). A 'write strobe' signal is sent from each stage of the VCDL to the corresponding sampling cell in each channel. The write strobe passes the VCDL-generated sampling rate to the sample-and-hold switches of each SCA cell. Each cell is made from a switched capacitor sampling cell and integrated ADC counter, as shown in Figure A.3. The trigger signal ultimately comes from the FPGA, in which sampling on every channel is halted and all analog samples are digitized. The on-chip ramp-compare ADC is run with a global analog ramp generator and 1 GHz clock that are distributed to each cell. Once digitized, the addressed data are serially sent off-chip on a 12-bit bus clocked at up to 80 MHz.
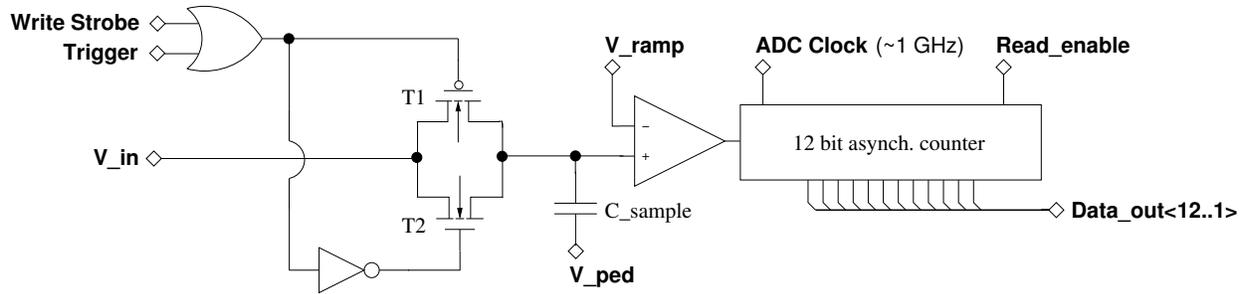
Figure A.3: Simplified schematic of the 'vertically integrated' PSEC4 cell structure. The sampling cell input, V_{in}, is tied to the on-chip 50Ω input microstrip line. Transistors T1 and T2 form a dual-CMOS write switch that facilitates the sample-and-hold of V_{in} on C_{sample}, a 20 fF capacitance referenced to *V_ped*. The switch is toggled by the VCDL write strobe while sampling (Figure A.2) or an ASIC-global trigger signal when an event is to be digitized. When the ADC is initiated, a global 0.0-1.2 V analog voltage ramp is sent to all comparators, which digitizes the voltage on C_{sample} using a fast ADC clock and 12-bit counter. To send the digital data off-chip, the register is addressed using *Read_enable*.
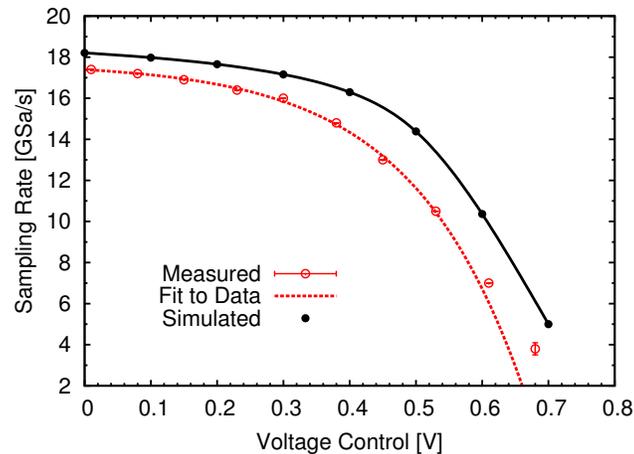

Figure A.4: Sampling rate as a function of VCDL voltage control. Good agreement is shown between post layout simulation and actual values. Rates up to 17.5 GSa/s are achieved with the free-running PSEC4 VCDL.

627 Typically, the servo-locking will be enabled and the VCDL is run as a delay-locked loop

628 (DLL). In this case, the sampling rate is automatically set by the input write clock frequency.

629 The stability of the sampling rate is negatively correlated with the slope magnitude as the

630 VCDL becomes increasingly sensitive to noise. The slowest stable sampling rate is ~4 GSa/s.

631 A 'write strobe' signal is sent from each stage of the VCDL to the corresponding sampling

cell in each channel. The write strobe passes the VCDL-generated sampling rate to the sample-and-hold switch of the cell as shown in Figure A.3. To allow the sample cell enough time to fully charge or discharge when sampling, the write strobe is extended to a fixed duration of 8× the individual VCDL delay stage. In sampling mode, a 'sampling block' made of 8 adjacent SCA sampling cells continuously tracks the input signal.

To servo-control the VCDL at a specified sampling rate and to compensate for temperature effects and power supply variations, the VCDL can be delay-locked on chip. The VCDL forms a delay-locked loop (DLL) when this servo-controlled feedback is enabled. The servo-control circuit is made of a dual phase comparator and charge pump circuit to lock both the rising and falling edges of the write clock at a fixed one-cycle latency [67]. A loop-filter capacitor is installed externally to tune the DLL stability.

With this DLL architecture, a write clock with frequency f_{in} is provided to the chip, and the sampling is started automatically after a locking time of several seconds. The nominal sampling rate in GSa/s is set by $0.256 \cdot f_{in}$ [MHz], and the sampling buffer depth in nanoseconds is given by $10^3/f_{in}$ [MHz^{-1}]. A limitation of the PSEC4 design is the relatively small recording depth at high sampling rates due to the buffer size of 256 samples.

A.3.2   Sampling and Triggering

A single-ended, 256-cell SCA was designed and implemented on each channel of PSEC4. Each sampling cell circuit is made from a dual CMOS write switch and a metal-insulator-metal sampling capacitor as shown in Figure A.3. With layout parasitics, this capacitance is effectively 20 fF. During sampling, the write switch is toggled by the write strobe from the VCDL. To record an event, an external trigger, typically from an FPGA, overrides the sampling and opens all write switches, holding the analog voltages on the capacitor for the ADC duration ($\leq 4\,\mu$s). Triggering interrupts the sampling on every channel, and is held until the selected data are digitized and read out. When triggered, the sampling is asynchronously halted. This corrupts the voltage on the 7 sample cells that were in the process of sampling,

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658 reducing the effective number of PSEC4 samples to 249.

659   The PSEC4 has the capability to output a threshold-level trigger bit on each channel.
660 The internal trigger is made from a fast comparator, which is referenced to an external
661 threshold level, and digital logic to latch and reset the trigger circuit. To form a PSEC4
662 trigger, the self-trigger bits are sent to the FPGA, which returns a global trigger signal back
663 to the chip. In the internal trigger mode, the trigger round-trip time is 15-20 ns (depending
664 on FPGA algorithm), which allows for the recording of a waveform before it is overwritten
665 at 10 GSa/s.

A.3.3   Analog-to-Digital Conversion

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667 Digital conversion of the sampled waveforms is done on-chip with a single ramp-compare
668 ADC that is parallelized over the entire ASIC[2]. Each sample cell has a dedicated comparator
669 and 12 bit counter as shown in Figure A.3. In this architecture, the comparison between
670 each sampled voltage (V_{sample}) and a global ramping voltage (V_{ramp}), controls the clock
671 enable of a 12-bit counter. When $V_{ramp} > V_{sample}$, the counter clocking is disabled, and
672 the 12-bit word, which has been encoded by the ADC clock frequency and the ramp duration
673 below V_{sample}, is latched and ready for readout.

674   Embedded in each channel is a 5-stage ring oscillator that generates a fast digital ADC
675 clock, adjustable between 200 MHz and 1.4 GHz. The ADC conversion time, power con-
676 sumption, and resolution may be configured by adjusting the ramp slope or by tuning the
677 ring oscillator frequency.

A.3.4   Readout

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679 The serial data readout of the latched counter bits is performed using a shift register 'token'
680 architecture, in which a *read_enable* pulse is passed sequentually along the ADC counter
681 array. To reduce the chip readout latency, a limited selection of the 1536 counters in PSEC4

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2. An overview of this ADC architecture can be found in reference [68].

can be read out. Readout addressing is done by selecting the channel number and a block of

64 cells. While not completely random access, this scheme permits a considerable reduction

in dead time. At a maximum rate of 80 MHz, the readout time is 0.8 μs per 64-cell block.

The readout latency is typically the largest contributor to the dead-time of the chip. The

ADC conversion time also adds up to 4 μs of latency per triggered event. These two factors

limit the sustained trigger rate to $\sim$200 kHz/channel or $\sim$50 kHz/chip.

A.4   Calibration

A.4.1   Linearity and Dynamic Range

The signal voltage range is limited by the 1.2 V core voltage of the 0.13 μm CMOS pro-

cess [63]. To enable the recording of signals with pedestal levels that exceed this range, the

input is AC coupled and a DC offset is added to the 50 Ω termination. This is shown in the

Figure A.2 block diagram, in which the DC offset is designated by *V_ped*. The offset level is

tuned to match the input signal voltage range to that of PSEC4.

The PSEC4-channel response to a linear pedestal scan is shown in Figure A.5. This is

the average DC response over all 256 cells in a channel. A signal voltage range of 1 V is

shown, as input signals between 100 mV and 1.1 V are fully coded with 12 bits. An integral

non-linearity (INL) of better than 0.15% is shown for most of that range. The non-linearity

and limited DC signal range near the voltage rails are due to transistor threshold issues in

the comparator circuit.

The DNL of this response, shown by the linear fit residuals in Figure A.5, can be corrected

by creating an ADC count-to-voltage look-up-table (LUT) that maps the input voltage to

the PSEC4 output code. The raw PSEC4 data is converted to voltage and 'linearized' with

a channel-averaged LUT.

Further linearity calibrations can be implemented to correct for cell-to-cell gain variations.

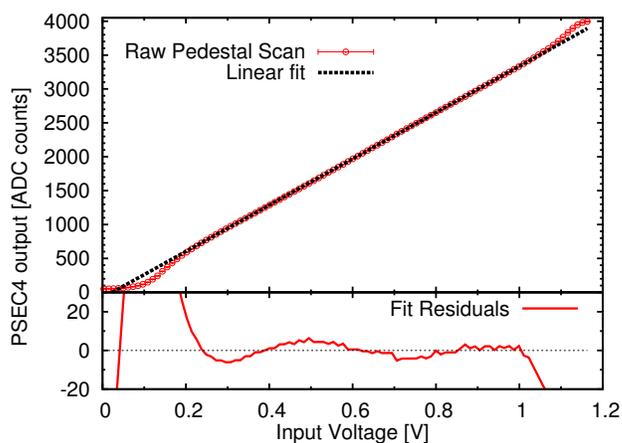A display of raw linearity scans over cells in a single channel is shown in Figure A.6. After

Figure A.5: DC response of the device running in 12 bit mode. The data are an average response of all 256 cells from a single channel. The upper plot shows raw data (red points) and a linear fit over the the same dynamic range (dotted black line, slope of 4 counts/mV). The fit residuals are shown in the lower plot.
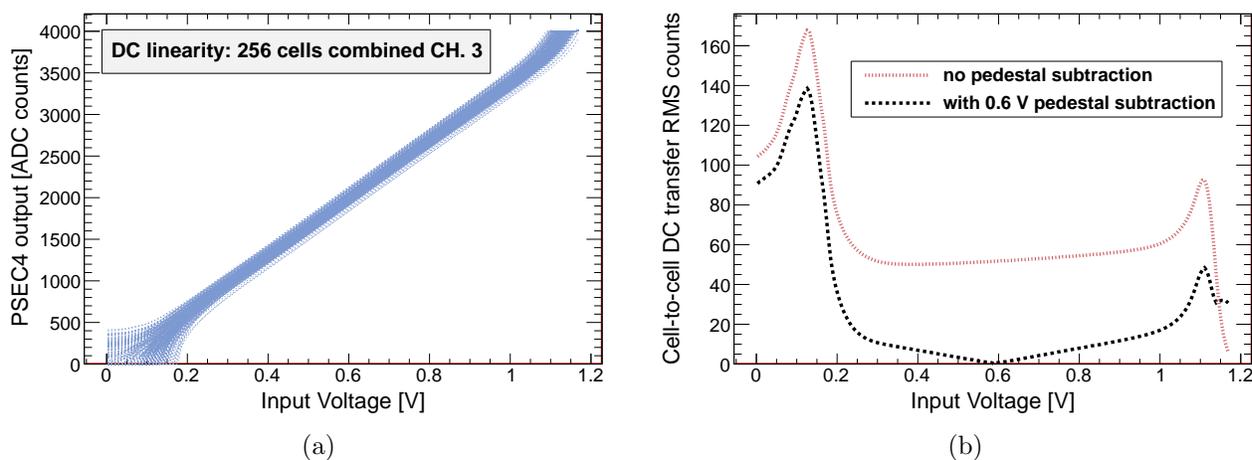

Figure A.6: (a) Raw DC scans for all 256 PSEC4 cells on a single channel. (b) RMS spread in ADC counts scanned over input voltage on a PSEC4 channel. A mid-range pedestal subtraction on each cell reduces the RMS/mean spread to ~1% over an 0.8 V range

a cell pedestal subtraction, the RMS cell-to-cell gain dispersion is ~1% over an 0.8 V range. Over this range, a single count-to-voltage LUT per channel may be sufficient. To effectively use the entire PSEC4 DC dynamic range, a count-to-voltage conversion LUT should be implemented for each individual cell.
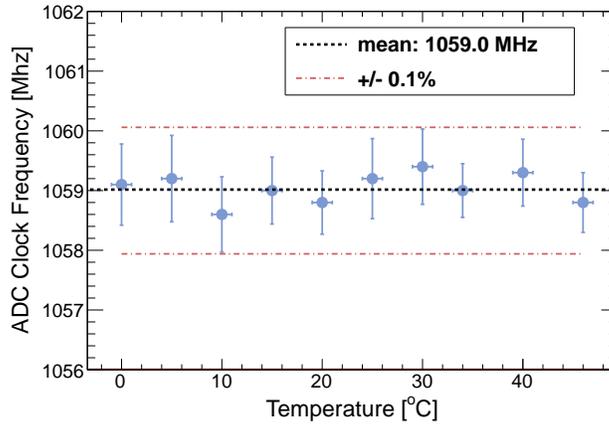
Figure A.7: Ring oscillator clock stability over temperature. This clock is stabilized with a servo-control algorithm in the FPGA that adjusts the DAC oscillator voltage controls. With this feedback, the ring oscillator frequency is held within 0.1% of the nominal 1.059 GHz over the tested temperature range.

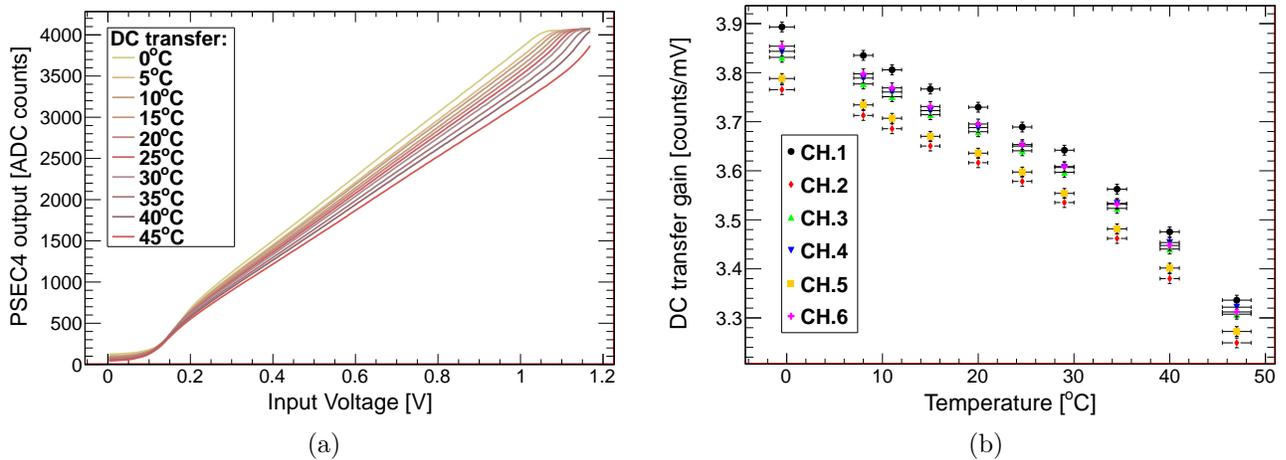|	
(a)	(b)

Figure A.8: (a) Average DC response of a single PSEC4 channel over a temperature range of 0°C to 45°C. (b) The extracted DC transfer gains as a function of temperature for all channels.

Temperature Dependance

The ring oscillator ADC clock is the most temperature sensitive circuit and is servo-controlled using the FPGA to better than 0.1% over a wide temperature range as shown in Figure A.7. The ADC clock frequency was measured using 50k events at each temperature. Other temperature sensitive circuitry, including the chip-global ramp generator, are not feedback

⁷¹⁶ controlled.

⁷¹⁷ The count-to-voltage transfer also shows temperature variation due to changes in the
⁷¹⁸ ADC ramp slope. The average DC transfer curves at different temperatures are shown
⁷¹⁹ in Figure A.8a. The count-per-voltage gain is extracted from a fit to the linear region of
⁷²⁰ the DC transfer curve and is plotted in Figure A.8b. Since the ADC ramp is common to
⁷²¹ all channels, the average DC tranfer gains of all channels are observed to have the same
⁷²² temperature dependence. To mitigate this effect, a feedback loop that serves the ramp
⁷²³ current source could be implemented.

⁷²⁴ A.4.2   Sampling Calibration

⁷²⁵ For precision waveform feature extraction, both the overall time-base of the VCDL and
⁷²⁶ the cell-to-cell time step variations must be calibrated. With the rate-locking DLL, the
⁷²⁷ overall PSEC4 sampling time base is stably servo-controlled at a default rate of 10.24 GSa/s.
⁷²⁸ The time-base calibration of the individual 256 delay stages, which vary due to cell-to-cell
⁷²⁹ transistor size mismatches in the VCDL, is the next task. Since this is a fixed-pattern
⁷³⁰ variation, the time-base calibration is typically a one-time measurement.

⁷³¹ The brute force 'zero-crossing' time-base calibration method is employed [40]. This tech-
⁷³² nique counts the number of times a sine wave input crosses zero voltage at each sample
⁷³³ cell. With enough statistics, the corrected time per cell is extracted from the number of
⁷³⁴ zero-crossings (N_{zeros}) using

$$< \Delta t >= \frac{T_{input} < N_{zeros} >}{2\, N_{events}} \tag{A.3}$$

⁷³⁵ where T_{input} is the period of the input and N_{events} is the number of digitized sine waveforms.
⁷³⁶ A typical PSEC4 time-base calibration uses 10^6 recorded events of 400 MHz sinusoids.

⁷³⁷ The variation of the time-base sampling steps is $\sim$13% as shown in Figure A.9a. Due
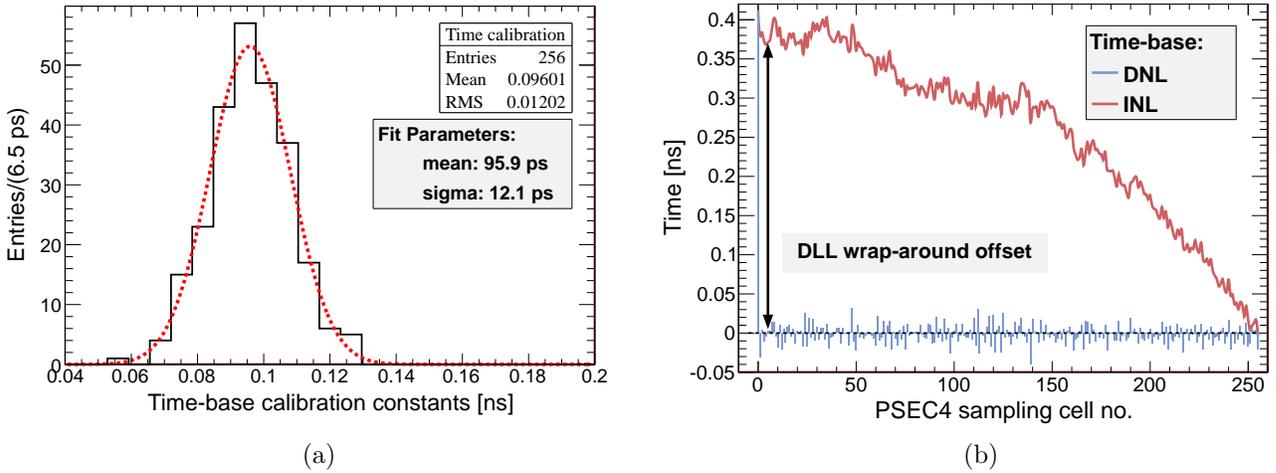⁷³⁸ to a relatively large time step at the first cell, the average sampling rate over the remaining

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(a)   (b)

Figure A.9: (a) A histogram of the extracted time-base calibration constants (Δt) from a single channel. These values are calculated using the zero-crossing technique and are used to correct the sampling time-base of the PSEC4 chip. (b) The differential (DNL) and integral non-linearity (INL) of the PSEC4 time-base. The extracted Δt's are compared to an ideal linear time-base with equal time-steps per sample point. The large time-step at the first sample bin is caused by a fixed DLL latency when wrapping the sampling from the last cell to the first.
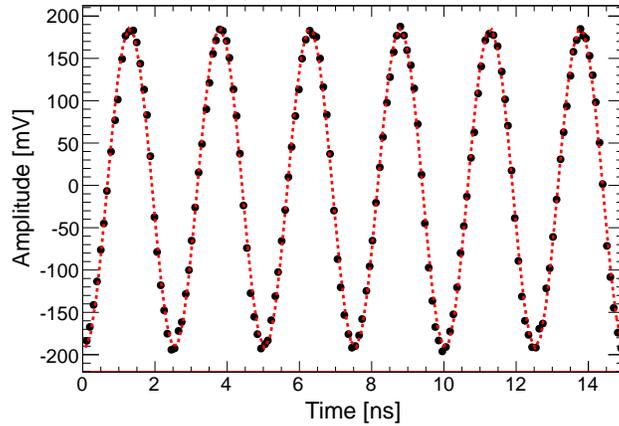

Figure A.10: A 10.24 GSa/s capture of a 400 MHz sine input is shown (black dots) after a channel-only linearity correction and time-base calibration. A fit (red dotted line) is applied to the data.

739   VCDL cells is ∼10.4 GSa/s, slightly higher than the nominal rate. With the servo-locking

740   DLL the INL is constrained to be zero at the last cell. A digitized 400 MHz sine wave is

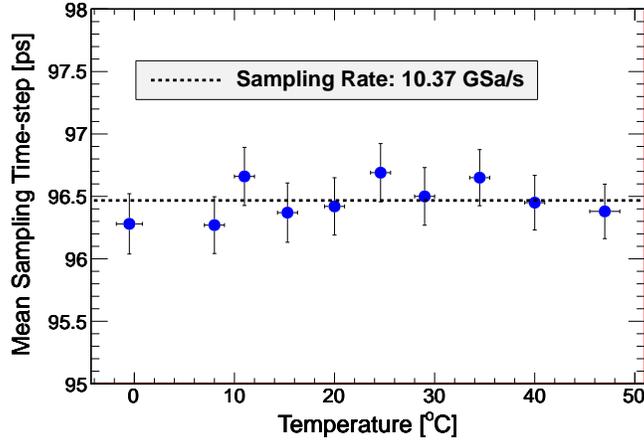741   shown in Figure A.10 after applying the time-base calibration constants.

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Figure A.11: Mean time-base step as measured over a temperature range -1°C to 46°C. The sampling rate is held constant over temperature with the on-chip DLL.

⁷⁴²   The non-linearity of the PSEC4 time-base is shown in Figure A.9b. Each bin in the ⁷⁴³ plot is indicative of the time-base step between the binned cell and its preceding neighbor ⁷⁴⁴ cell. The relatively large DNL in the first bin, which corresponds to the delay between the ⁷⁴⁵ last (cell 256) and first sample cells, is caused by a fixed DLL latency when wrapping the ⁷⁴⁶ sampling from the last cell to the first.

⁷⁴⁷   The mean sampling rate is shown in Figure A.11 to be uniform over temperature. This ⁷⁴⁸ is an expected feature of the on-chip DLL. Fifty-thousand events were recorded at each ⁷⁴⁹ temperature point and the zero crossing algorithm was run on each dataset. No temperature ⁷⁵⁰ dependence is observed.

A.5   Performance

⁷⁵² Measurements of the PSEC4 performance have been made with several chips on custom ⁷⁵³ evaluation boards shown in Figure A.12. The sampling rate was fixed at a nominal rate ⁷⁵⁴ of 10.24 GSa/s. Here we report on bench measurements of linearity (§A.4.1), analog leak- ⁷⁵⁵ age (§A.5.1), noise (§A.5.2), power (§A.5.3), frequency response (§A.5.4), sampling calibra- ⁷⁵⁶ tions (§A.4.2), and waveform timing (§A.5.5). A summary table of the PSEC4 performance ⁷⁵⁷ is shown in §**??**.
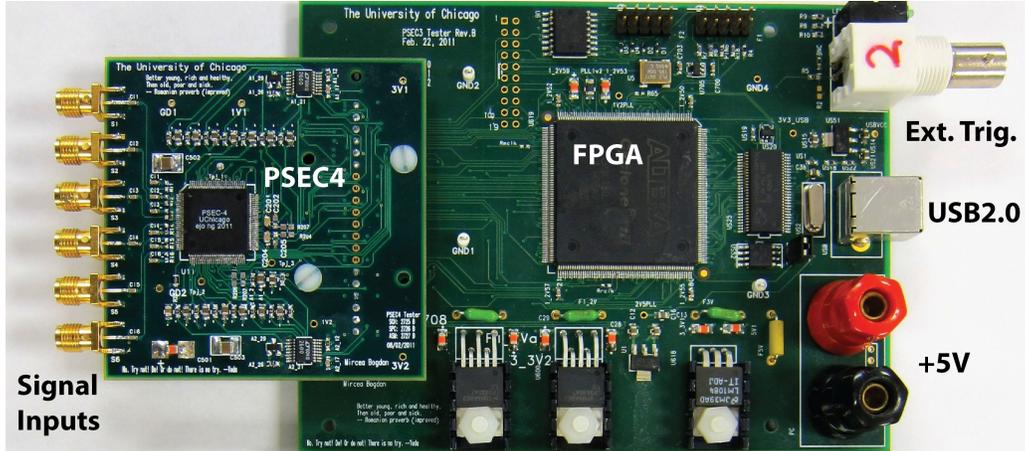
Figure A.12: The PSEC4 evaluation board. The board uses a Cyclone III Altera FPGA (EP3C25Q240) and a USB 2.0 PC interface. Custom firmware and acquisition software were developed for overall board control. The board uses +5 V power and draws <400 mA, either from a DC supply or the USB interface.

A.5.1   Sample Leakage

When triggered, the write switch on each cell is opened and the sampled voltage is held at high impedance on the 20 fF capacitor (Fig. A.3). Two charge leakage pathways are present: 1) sub-threshold conduction through the write switch formed by transistors T1 and T2; and 2) gate-oxide tunneling through the NFET at the comparator input. The observable leakage current is the sum of these two effects.

To measure the leakage current, a 300 ns wide, variable-level pulse was sent to a single PSEC4 channel. Since the sampling window is 25 ns, each SCA cell sampled the transient level. After triggering, the sampled transient voltage was repeatedly digitized at 1 ms intervals and the change in voltage on the capacitor was recorded over a 10 ms storage-time.

The room temperature PSEC4 leakage current as a function of input voltage over the full 1 V dynamic range is shown in Figure A.13. A pedestal level of $V_{DD}/2 = 0.6$ V was set at the input. The measured leakage is shown in the 2-D histogram. A large spread (RMS $\sim$70 fA) is seen at each voltage level. Results from a 0.13 μm CMOS SPICE simulation show that the write-switch leakage is the dominant pathway. A small amount ($\leq$100 fA) of NFET gate-oxide tunneling is also consistent with the data.
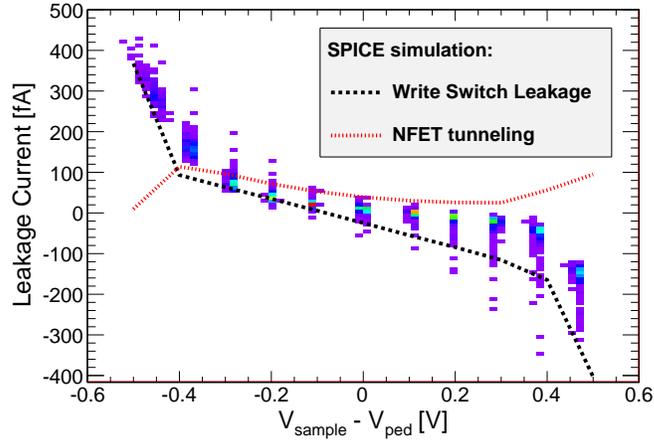
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Figure A.13: PSEC4 sample cell leakage measured at room temperature. The measured leakage is shown by the histogrammed data points. Results from a 0.13 μm CMOS SPICE simulation are also included. The simulation shows the leakage current contributions from 1) sub-threshold conduction through the disengaged write switch; and 2) gate-oxide tunneling from the NFET in the input stage of the comparator.

In normal operation, the ADC is started immediately after a trigger is registered. In this case, the analog voltage hold time is limited to the ADC conversion time. Assuming a constant current, the leakage-induced voltage change is given by

$$\Delta V = \frac{I_{leakage}\,\Delta t}{C_{sample}} \tag{A.4}$$

where Δt is the ADC conversion time. With the maximum leakage current of ± 500 fA and a conversion time of 4 μs, ΔV is ± 100 μV. This value is at least $5\times$ lower than the electronics noise. In other cases, the analog voltage may be held for a period time in order to wait for a trigger decision. This configuration was used in the OTPC trigger and is dicussed in §**??**.

A.5.2 Noise

After fixed-pattern pedestal correction and event-by-event baseline subtraction, which removes low-frequency noise contributions, the PSEC4 electronic noise is measured to be $\sim$700 μV RMS on all channels as shown in Figure A.14a. The noise level is consistently sub-mV over a $\pm 20^\circ$C temperature range around room temperature. Above $\sim 20^\circ$C, the
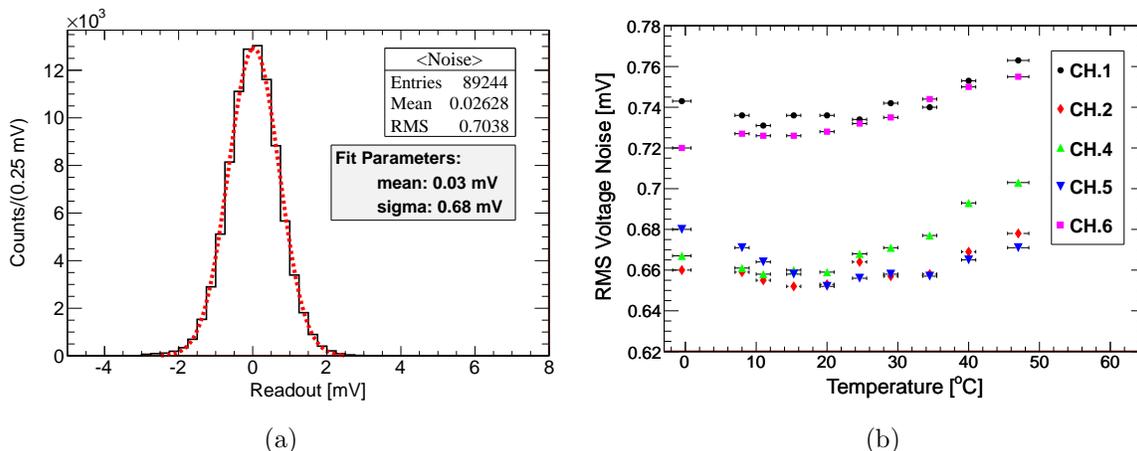
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Figure A.14: (a) A PSEC4 baseline readout showing the electronic noise. The data are recorded from single channel after offset correction. The RMS value of $\sim$700 μV is representative of the electronics noise on all channels. (b) Channel RMS noise measured over temperature.

electronics noise increases with temperature, which is consistent with the thermal noise expectation of $\sqrt{k_B T/C}$ (Figure A.14b). The noise figure is dominated by broadband thermal noise on the 20 fF sampling capacitor, which contributes 450 μV (RMS 60 electrons) at 300 K. Other noise sources include the ADC ramp generator and comparator. The noise corresponds to roughly 3 least significant bits (LSBs), reducing the DC RMS dynamic range to 10.5 bits over the signal voltage range.

A.5.3 Power

The power consumption is dominated by the ADC, which simultaneously clocks 1536 ripple counters and several hundred large digital buffers at up to 1.4 GHz. The total power draw per chip as a function of ADC clock rate is shown in Figure A.15. To reduce the steady state power consumption and to separate the chip's digital processes from the analog sampling, the ADC is run only after a trigger is sent to the chip. Without a trigger, the quiescent power consumption is $\sim$40 mW per chip, including the locked VCDL sampling at 10.24 GSa/s and the current biases of all the comparators.

Initiating the ADC with a clock rate of 1 GHz causes the power draw to increase from
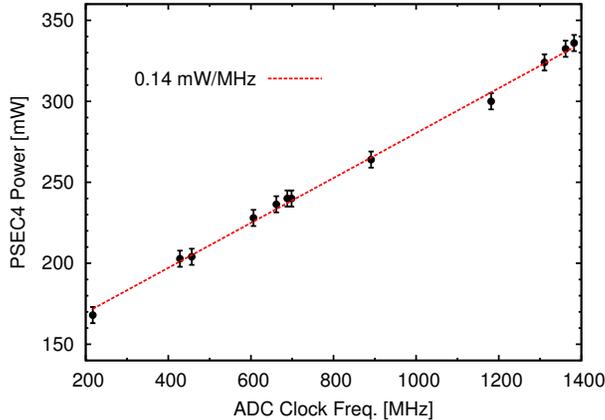
Figure A.15: Total PSEC4 power as a function of the ADC clock rate. Clock rates between 200 MHz and 1.4 GHz can be selected based on the power budget and targeted ADC speed and resolution. When the ADC is not running, the quiescent (continuous sampling) power consumption is ∼40 mW per chip.

40 mW to 300 mW within a few nanoseconds. To mitigate high-frequency power supply fluctuations when switching on the ADC, several 'large' (2 pF) decoupling capacitors were placed on-chip near the ADC. These capacitors, in addition with the close-proximity evaluation board decoupling capacitors (∼0.1-10 μF), prevent power supply transients from impairing chip performance.

At the maximum PSEC4 sustained trigger rate of 50 kHz, in which the ADC is running 20% of the time, a maximum average power of 100 mW is drawn per chip.

A.5.4   Frequency Response

The target analog bandwidth for the PSEC4 design was ≥1 GHz. The bandwidth is limited by the parasitic input capacitance (C_{in}), which drops the input impedance at high frequencies[3] as

$$|Z_{in}| = \frac{R_{term}}{\sqrt{1 + \omega^2\, R_{term}\, C_{in}}} \tag{A.5}$$

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3. This ignores negligible contributions to the impedance due to the sampling cell input coupling. The write switch on-resistance (≤ 4 kΩ over the full dynamic range) and the 20 fF sampling capacitance introduce a pole at ≥2 GHz.
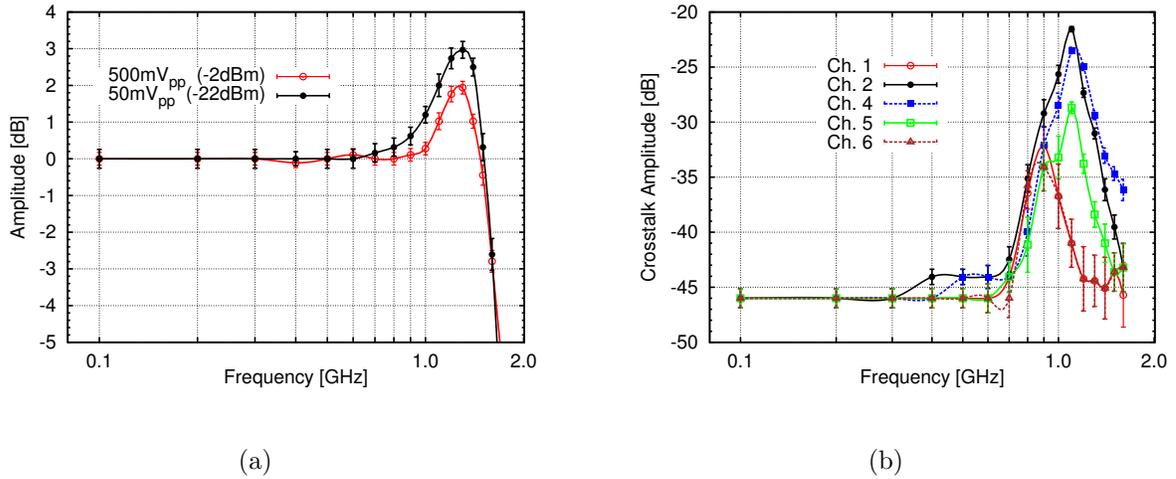
Figure A.16: (a) PSEC4 frequency response. The -3 dB analog bandwidth is 1.5 GHz. The positive resonance above 1 GHz is due to bondwire inductance of the signal wires in the chip package. Similar responses are shown for large and small sinusoidal inputs. (b) Channel-to-channel crosstalk as a function of frequency. Channel 3 was driven with a -2 dBm sinusoidal input. Adjacent channels see a maximum of -20 dB crosstalk at 1.1 GHz. The electronic noise floor is -50 dB for reference.

where R_{term} is an external 50 Ω termination resistor. Accordingly, the expected half-power bandwidth is given by:

$$f_{3dB} = \frac{1}{2\pi \, R_{term} \, C_{in}} \tag{A.6}$$

The extracted C_{in} from post-layout studies was ∼2 pF, projecting a -3 dB bandwidth of 1.5 GHz which corresponds to the measured value shown in Figure A.16a. The chip package-to-die bondwire inductance gives a resonance in the response above 1 GHz that distorts signal content at these frequencies. An external filter may be added to flatten the response.

The error bars correspond to the measurement procedure, in which several thousand sine waves are recorded at each frequency and histogrammed. The histogram bins with the maximum values are at the high and low peaks of the PSEC4-digitized sine wave. These peaks are fitted with a Gaussian function, from which the mean sine wave amplitude and measurement error (σ from fits) is extracted

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The measured channel-to-channel crosstalk is -25 dB below 1 GHz for all channels as shown in Figure A.16b. For frequencies less then 700 MHz, this drops to better than -40 dB. The primary crosstalk mechanism is thought to be the mutual inductance between signal bondwires in the chip package. High frequency substrate coupling on the chip or crosstalk between input traces on the PSEC4 evaluation board may also contribute.

Figure A.17 shows the crosstalk correlations between channels at 500 and 1000 MHz driving channel 3 with a -2 dBm sinusoid. In the 500 MHz case, the cross talk is relatively small and the magnitude is consistent with sub-1% crosstalk. Comparatively large correlations are observed on all non-driven channels for the 1000 MHz situation. The largest magnitude, $\sim$10%, is found on the closest proximity channel 2. These measurements were performed with no inductive on-board pedestal isolation so the magnitudes are higher than the previously reported crosstalk values. The crosstalk phase and amplitude can be inferred from the correlation ellipses.

AC linearity

The PSEC4 response to sinusoidal signals of varying magnitude is shown in Figure A.18. The AC signals were calibrated using the DC transfer count-to-voltage LUT (Figure A.5). Saturation is observed for signals as low as 100 MHz ($\sim$9% above V_{pp} of 500 mV) and this effect becomes constant for frequencies above 500 MHz ($\sim$15% above V_{pp} of 500 mV).

This AC saturation effectively reduces the PSEC4 ADC dynamic range. With a DC calibration, it was shown that 10.5 bits effectively covered a 1 V range including electronics noise. At 100 MHz, the dynamic range drops to $\sim$10.35 bits. For signals up to 1 GHz, the dynamic range is 10.3 bits. Additionally, an AC count-to-voltage conversion calibration LUT can be used for correct for this saturation.
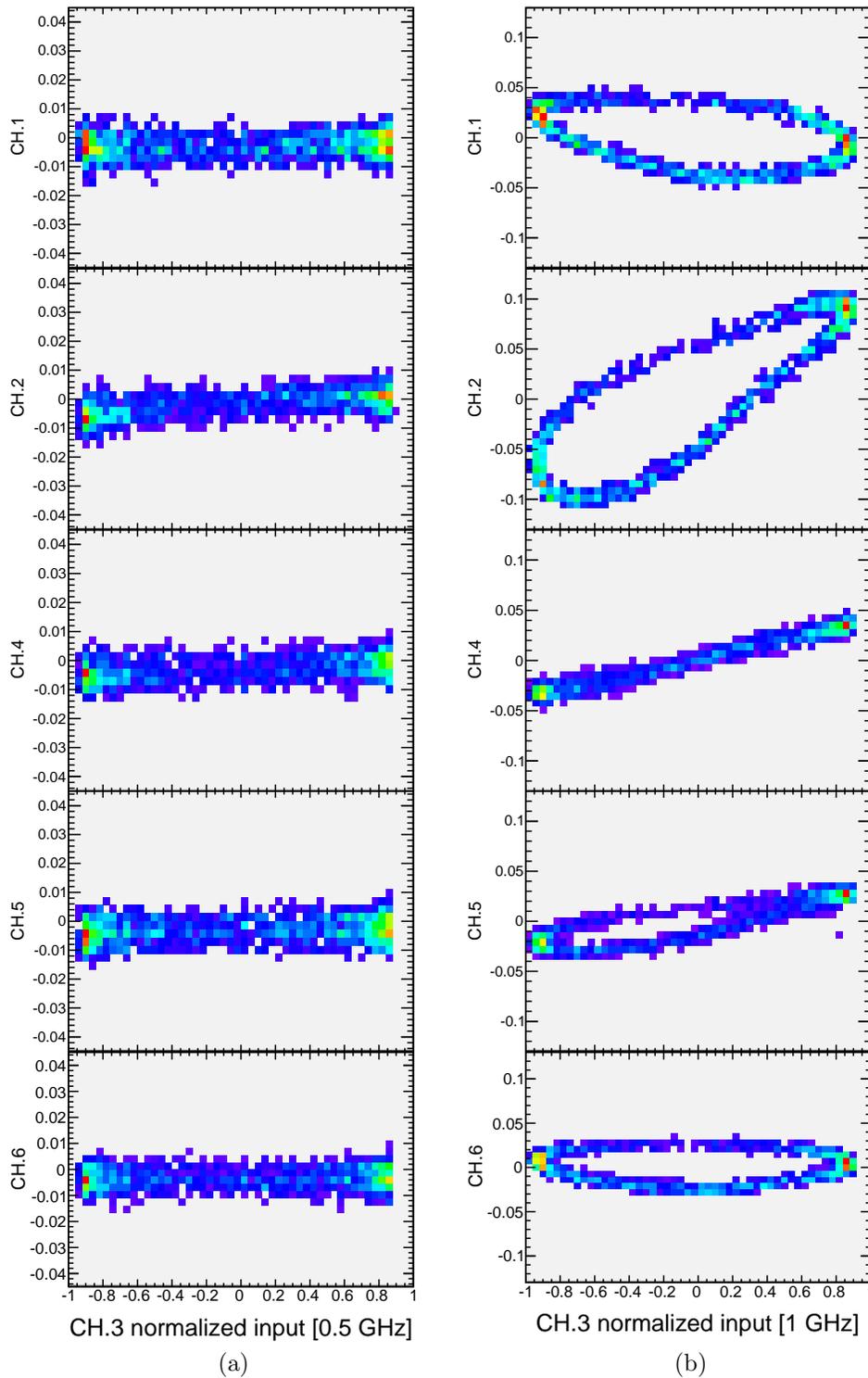
Figure A.17: Crosstalk correlation ellipses. (a) Crosstalk correlations at 500 MHz with a -2 dBm sinusoidal driving channel 3. A small correlation is observed in Channel 2, but otherwise no correlations are present. The magnitude is consistent with sub-1% crosstalk. (b) Crosstalk correlations at 1 GHz with a -2 dBm sinusoidal driving channel 3.
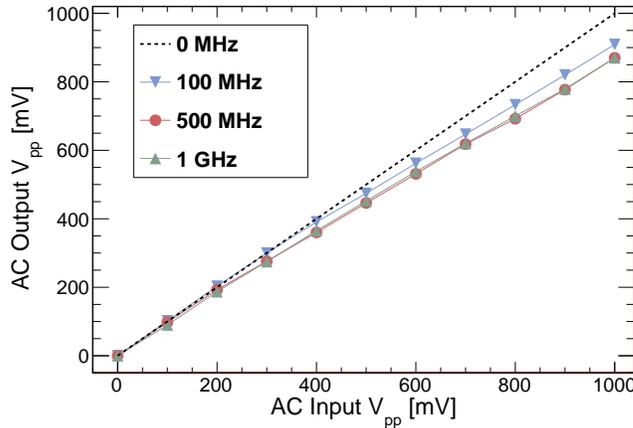
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Figure A.18: AC response of a single channel. The PSEC4 data were converted to voltage using the DC linearity LUT as shown in Fig. A.5. Saturation of the AC signals is observed for all frequencies, most clearly above 500 mV$_{pp}$

A.5.5 Waveform Timing

The effective timing resolution of a single measurement is calculated by waveform feature extraction after linearity and time-base calibration. A 0.5 V$_{pp}$, 1.25 ns FWHM Gaussian pulse was created using a 10 GSa/s arbitrary waveform generator. The output of the generator was sent to 2 channels of the ASIC using a broadband-RF 50/50 splitter. This pulse, as recorded by a channel of PSEC4, is shown in Figure A.19. A Gaussian functional fit is performed to the leading edge of the pulse. The pulse times from both channels are extracted from the fit and are subtracted on an event-by-event basis.

The timing resolution was measured by asynchronous pulse injection to two channels of PSEC4. In this measurement, the two pulses were delayed relative to one-another and the waveforms were captured uniformly across the 25 ns PSEC4 sampling buffer. Ten-thousand events were recorded at each delay stage. The time difference resolution was extracted by the waveform fitting procedure shown in Figure A.19, before and after applying the time-base calibration to both channels. Figures A.20a and A.20b show the timing resolution results for pulse separations in the PSEC4 buffer of 0 ns and 16 ns, respectively. For uncalibrated data in which the pulse separation is non-zero, the bimodal timing distribution is due to the fixed DLL-wraparound offset.
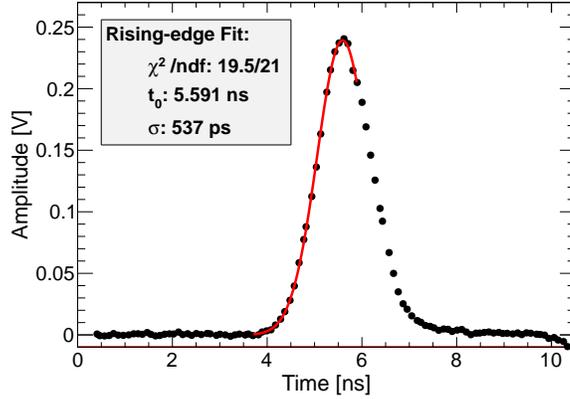
Figure A.19: An example PSEC4 digitized pulse (black dots) and waveform fit (red line) that was used for the timing resolution measurement. A 1.25 ns FWHM Gaussian pulse was split and injected into two channels of the chip. The waveform was captured at 10.24 GSa/s and is shown after applying the time-base calibration constants.
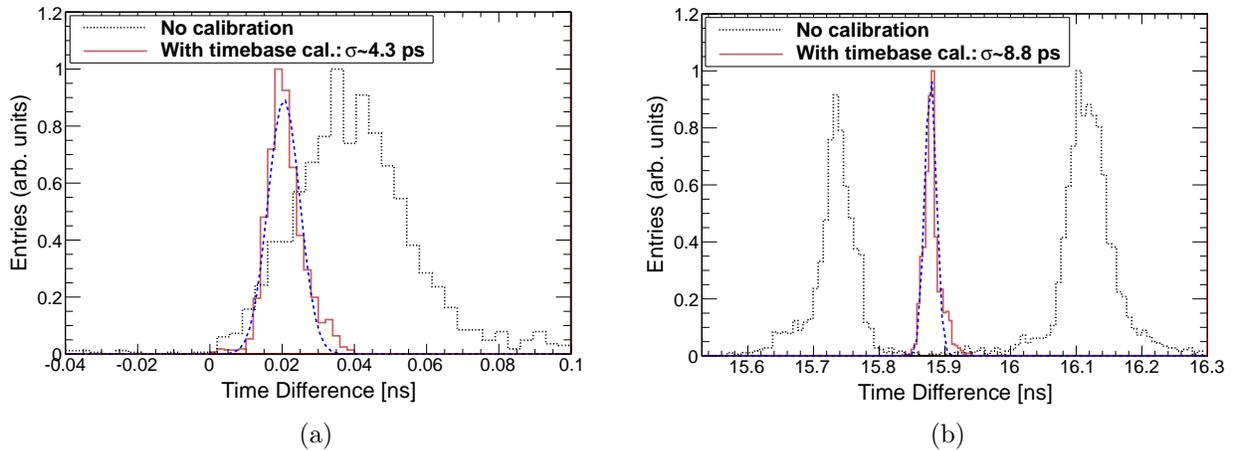

Figure A.20: Time resolution results before (black-dashed) and after (maroon-solid lines) applying timebase calibrations. Pulses were injected asynchronously into 2 channels of PSEC4. Data are shown for pulse separations of (a) ~0 ns, and (b) ~16 ns. The bimodal distribution in the pre-calibration data of (b) corresponds to the fixed DLL wraparound offset.

A PSEC4-calibrated timing resolution of 9 ps or better was measured over a 20 ns span of pulse separation. The 1σ resolution was extracted by fitting the calibrated timing distributions shown in Figure A.20. For simultaneous pulses the resolution is ~4 ps, but the timing resolution slightly degrades as the time difference between pulses is increased. The large RMS in the timing for uncalibrated data is due to the DLL wraparound offset of roughly

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Table A.1: PSEC4 architecture parameters and measured performance results.

Parameter	Value	Comment
Channels	6	die size constraint
Sampling Rate	4-15 GSa/s	servo-locked on-chip
Samples/channel	256	249 samples effective
Recording Buffer Time	25 ns	at 10.24 GSa/s
Analog Bandwidth	1.5 GHz	
Crosstalk	7%	max. over bandwidth
	<1%	typical for signals <800 MHz
Noise	700 μV	RMS (typical). RF-shielded enclosure. After calibration.
DC RMS Dynamic Range	10.5 bits	12 bits logged. Linearity calibration for each cell.
Signal Voltage Range	1 V	after linearity correction
ADC conversion time	4 μs	max. 12 bits logged at 1 GHz clock speed
	250 ns	min. 8-bits logged at 1 GHz
ADC clock speed	1.4 GHz	max.
Readout time	$0.8n$ μs	n is number of 64-cell blocks to read ($n = 24$ for entire chip)
Sustained Trigger Rate	50 kHz	max. per chip. Limited by [ADC time + Readout time]$^{-1}$
Power Consumption	100 mW	max. average power
Core Voltage	1.2 V	0.13 μm CMOS standard

400 ps.

The performance and key architecture parameters of PSEC4 are summarized in Table A.1.

APPENDIX B

G4BEAMLINE FLUX SIMULATIONS

B.1   Beam Monte Carlo

To understand the flux, momenta, and particle types at the OTPC location, a simulation

was written using the G4beamline toolkit [47]. Figure B.2 and Figure B.3 and Figure B.4

Table B.1: Simulated particle ID, count, and expectation value of total momentum, $<P_{tot}>$, at the OTPC location with an 8 GeV/c π^+ secondary beam. Particles with P_{tot} greater than 10 MeV/c were counted. (POT=π^+ on target). Numbers taken from simulation results shown in Figure B.4a.

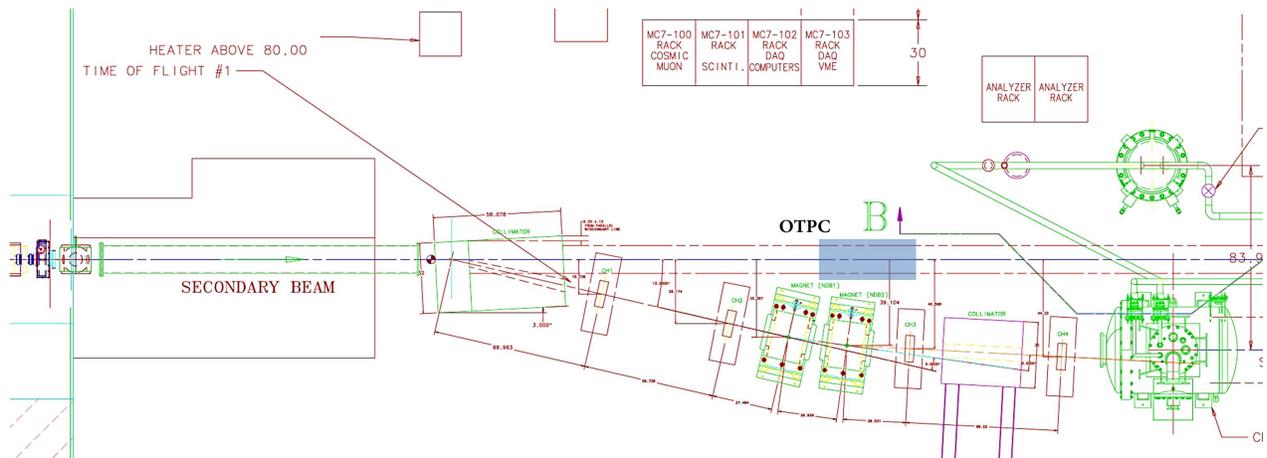| PID	N/(10^6 POT)	$<P_{tot}>$	Note:
$\mu^\pm$	800	4.5 GeV/c	broadband 2.5-6 GeV/c
$\pi^\pm$	20	5 GeV/c	small peak at 6GeV/c (absorber punch-thru dE/dx), otherwise scattered over 1-6 GeV/c
e$^\pm$	<5	<100 MeV/c	
γ	20	<100 MeV/c	
p	<5	<2 GeV/c	

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Figure B.1: Plan view of the MCenter-7 (MC7) enclosure. The OTPC was installed ∼3 m behind a 1.08 m thick steel collimator/absorber block, which sits directly behind a Copper target along the secondary beam-line. The flux at the OTPC location is the punch-thru and ejecta from the collimator block. (Mechanical drawing is courtesy of the Fermilab PPD/Mechanical Department)
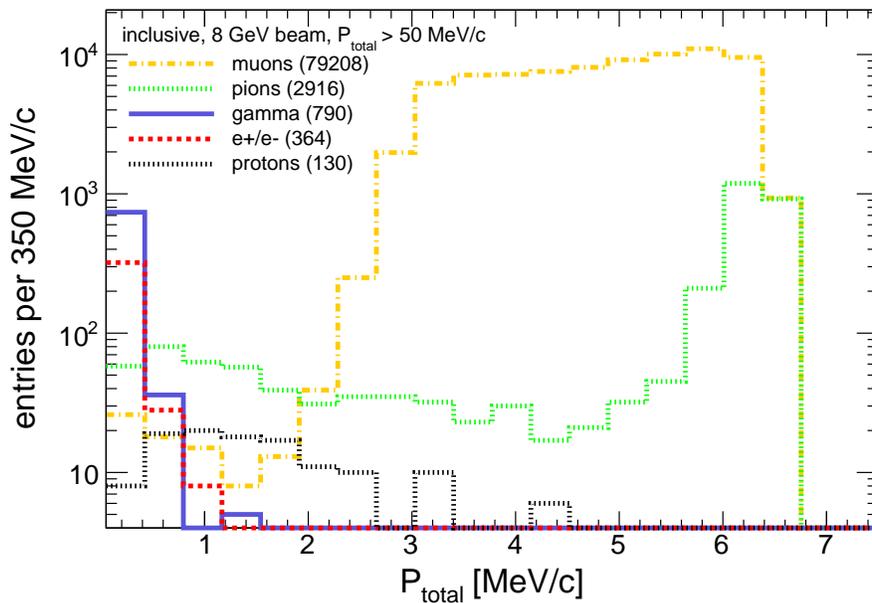

Figure B.2: Simulated particle type and total momentum, inclusive over the OTPC fiducial cross-section for an 8 secondary π^+ beam on target. Two-million pions-on-target (POT) were simulated.
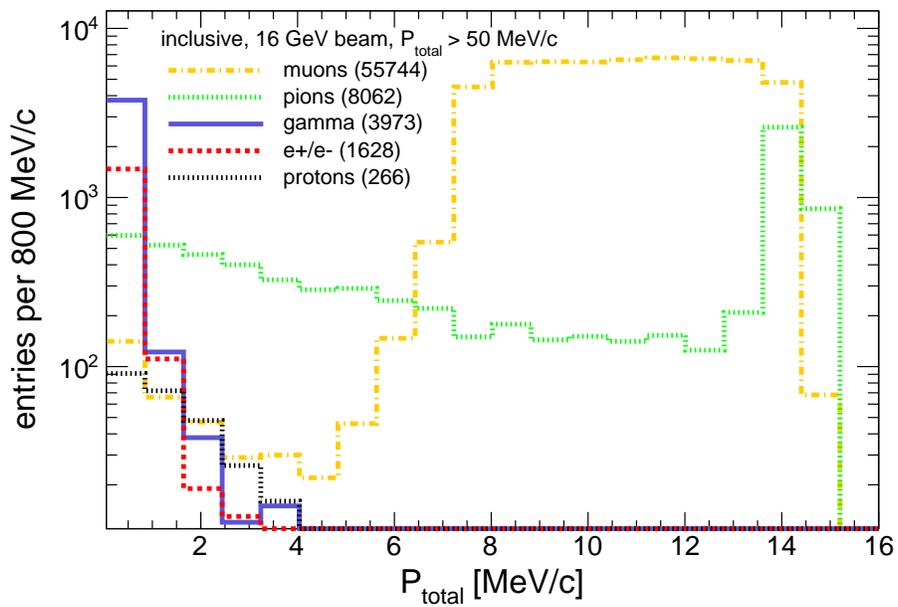
Figure B.3: Simulated particle type and total momentum, inclusive over the OTPC fiducial cross-section for a 16 GeV/c secondary π^+ beam on target. This simulation was the result of 1.7M POT.
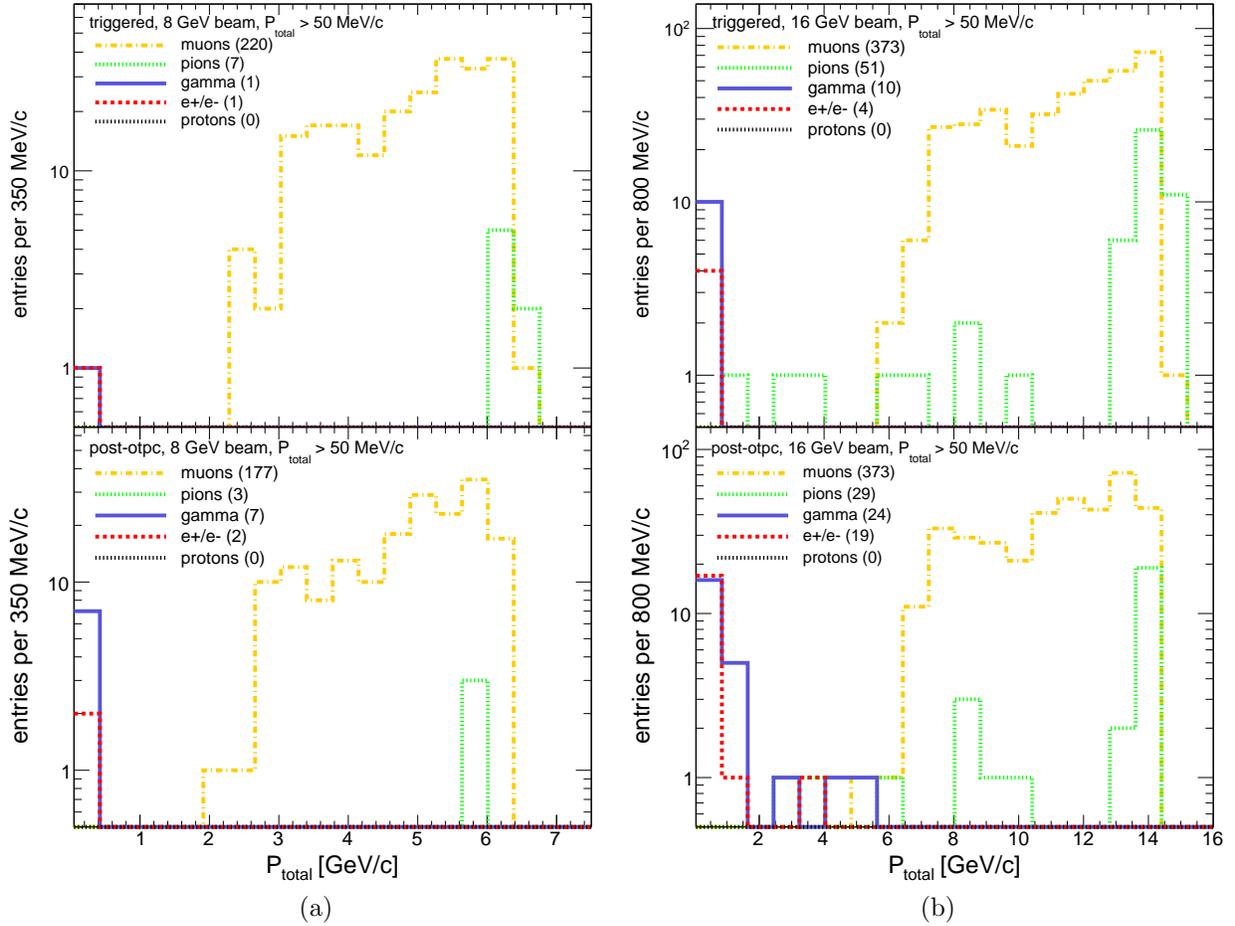
Figure B.4: Simulated beam at OTPC: triggered, particle type and momenta for (a) 8 and (b) 16 GeV/c secondary π^+ beam. The upper plots are cut on only beam that passes the front-trigger cut, and the bottom plots show these that also pass the back-trigger cut.
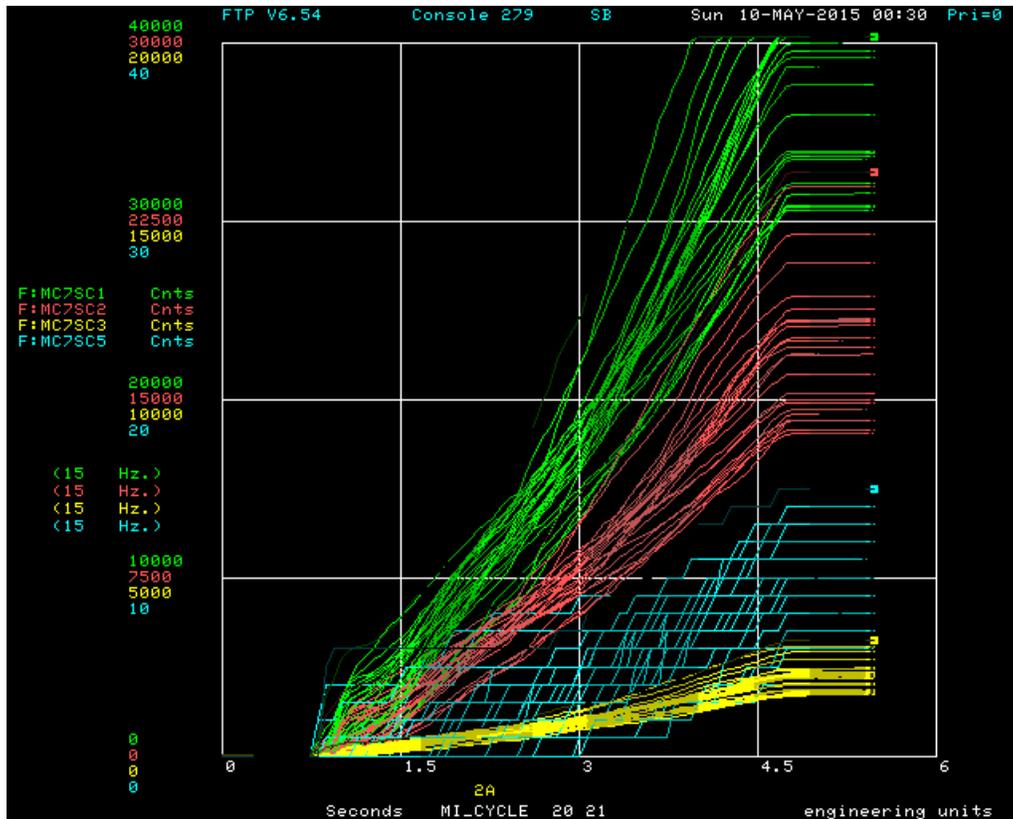
Figure B.5: ACNET plot of the π^+ counts delivered to MCenter on 10-May 2015 00:00-00:30. The counts on the copper target are represented by the green lines, which max out at ~40kCounts per spill. Plot courtesy of Fermilab Accelerator Divion/LArIAT collaboration.

REFERENCES

[1] D.R. Nygren. The Time-Projection Chamber - A new 4π detector for charged particles. *SLAC Reports PEP-144*, 1974.

[2] D. Fancher, H.J. Hilke, S. Loken, P. Martin, J.N. Marx, D.R. Nygren, P. Robrish, G. Shapiro, M. Urban, W. Wenzel, W. Gorn, and J. Layter. Performance of a time projection chamber. *Nucl.Instr.Meth A*, 161:383–390, 1979.

[3] S. Klein. The time projection chamber turns 25. *CERN Courier*, 2004.

[4] H.J. Hilke. Time projection chambers. *Rep. Prog. Phys.*, 73, 2010.

[5] C. Rubbia. The liguid-argon time projection chamber: a new concept for neutrino detectors. *CERN-EP/77-08*, 1977.

[6] P. A. Čerenkov. Visible radiation produced by electrons moving in a medium with velocities exceeding that of light. *Phys. Rev.*, 52:378–379, Aug 1937.

[7] J. Brack et. al. Characterization of the Hamamatsu R11780 12 inch Photomultiplier Tube. *Nucl.Instr.Meth A*, 712:162–173, 2013.

[8] MiniBooNE Collaboration (S.J. Brice et al.). Photomultiplier tubes in the MiniBooNE experiment. *Nucl.Instr.Meth A*, 562:97–109, 2006.

[9] R.B. Patterson et al. The extended-track event reconstruction for MiniBooNE. *Nucl.Instr.Meth A*, 608:206–224, 2009.

[10] LAPPD collaboration, `psec.uchicago.edu`.

[11] B.W. Adams et. al. An internal ALD-based high voltage divider and signal circuit for MCP-based photodetectors. *Nucl.Instr.Meth A*, 780:107–113, 2015.

[12] B.W. Adams et. al. Timing characteristics of large area picosecond photodetectors. *Nucl.Instr.Meth A*, 795:1–11, 2015.

[13] J. Milnes and J. Howorth. Picosecond time response characteristics of micro-channel plate PMT detectors. *SPIE USE*, 8:89–100, 2004.

[14] N. Kishimoto, M. Nagamine, K. Inami, Y. Enari, and T. Ohshima. Lifetime of MCP-PMT. *Nucl.Instr.Meth A*, 564:204–211, 2006.

[15] O.H.W. Siegmund et al., for LAPPD Collaboration. Atomic layer deposited borosilicate glass microchannel plates for large area event counting detectors. *Nucl.Instr.Meth A*, 695:168–171, 2012.

[16] M.J. Minot, et. al. Pilot production & commercialization of LAPPD™. *Nucl.Instr.Meth A*, 787:78–84, 2015.

72

[17] H. Grabas, H.Frisch, E.Oberla, J.-F. Genat, R. Northrop, D. McGinnis, B. Adams, M. Wetstein, R. Obaid, and F. Tang. RF Strip-Line Anodes for Psec Large-Area MCP-based Photodetectors. *Nucl.Instr.Meth A*, 711:123–131, 2013.

[18] PHOTONIS USA Pennsylvania, Inc. Planacon XP85022 32×32 datasheet, Jan 2014. `http://www.photonisusa.com`.

[19] I. Tamm. Radiation emitted by uniformly moving electrons. *J. Phys. USSR*, 1:439, 1939.

[20] J. Beringer, et. al. (PDG). Review of Particle Physics - Passage of particles through matter. *Phys. Rev. D*, 86:323–338, 2012.

[21] J.D. Jackson. *Classical Electrodynamics*. John Wiley & Sons, Inc., 3rd edition, 1999.

[22] B. Ratcliff and J. Schweining. *Handbook of particle detection and imaging*, volume 2, chapter 18: Cherenkov Counters. Springer, 2012. Edited by C. Grupen and I. Buvat.

[23] M. Daimon and A. Masumura. Measurement of the refractive index of distilled water from the near-infrared region to the ultraviolet region. *Appl. Opt.*, 46:3811–3820, 2007.

[24] G. Orebi Gann et. al. Advanced Scintillator Detector Concept (ASDC): A Concept Paper on the Physics Potential of Water-Based Liquid Scintillator. arxiv:1409.5864, 2014.

[25] M.C. Sanchez, M. Wetstein, et. al. Letter of Intent: The Accelerator Neutrino Neutron Interaction Experiment (ANNIE). *arXiv:1504.0180*, 2015.

[26] C Aberle, A Elagin, H J Frisch, M Wetstein, and L Winslow. Measuring directionality in double-beta decay and neutrino interactions with kiloton-scale scintillation detectors. *Journal of Instrumentation*, 9(06):P06012, 2014.

[27] M. Askins, et al. The Physics and Nuclear Nonproliferation Goals of WATCHMAN: A WAter CHerenkov Monitor for ANtineutrinos. arXiv:1502.01132, 2015.

[28] Credit to H. Nicholson first considering the idea of a photon-TPC in a neutrino experiment.

[29] S. Seibert and A. LaTorre. Fast Optical Monte Carlo Simulation With Surface-Based Geometries Using *Chroma*. `http://chroma.bitbucket.org/`, 2011.

[30] Optical data from: (1) Enhanced Aluminum 4-6 λ First-Surface Mirror, Edmunds Optics (2) Fused-silica glass port `www.mcmaster.com` (3) Optical coupling gel, code 0607, Cargille Labs. Spray paint used for light absorbing surfaces: Rust-oleum, textured, indoor/outdoor, black.

[31] W. Walkowiak. Drift velocity of free electrons in liquid argon. *Nucl.Instr.Meth A*, 449:228–294, 2000.

[32] S. Fukuda et al. The Super-Kamiokande detector. *Nucl.Instr.Meth A*, 501:418–462, 2003.

[33] S. Dazeley and M. Yeh. Private communication, 2015.

[34] F. Tang. Private communication.

[35] H.A. Wheeler. Transmission-line properties of a Strip on a Dielectric Sheet on a Plane. *IEEE Trans. Microwave Theory Tech*, 25:631–647, 1977.

[36] P. Russer. *Electromagnetics, Microwave Circuit, And Antenna Design for Communications Engineering*. Artech House, 2nd edition, 2006. Chapter 7, Transmission-Lines and Waveguides.

[37] Samtec, Inc. 34 AWG Micro Coax Cable Datasheet, May 2015.

[38] E. Oberla, H. Grabas, J.-F. Genat, H.J. Frisch, K. Nishimura, and G. Varner. A 15 GSa/s, 1.5 GHz bandwidth waveform digitizing ASIC. *Nucl.Instr.Meth A*, 735:452–461, 2014.

[39] G.S. Varner, L.L Ruckman, J.W. Nam, R.J. Nichol, J. Cao, P.W. Gorham, and M. Wilcox. The Large Analog Bandwidth Recorder and Digitizer With Ordered Readout (LABRADOR) ASIC. *Nucl.Instr.Meth A*, 583:447–460, 2007.

[40] K. Nishimura and A. Romero-Wolf. A Correlation-Based Timing Calibration & Diagnostic Technique for Fast Digitization ASICs. *Physics Procedia*, 37:1707–1714, 2012.

[41] D. Stricker-Shaver, S. Ritt, and B.J. Pichler. Novel calibration method for switched capacitor arrays enables time measurements with sub-picosecond resolution. *Nuclear Science, IEEE Transactions on*, 61(6):3607–3617, Dec 2014.

[42] Advanced Laser Diode Systems. Picosecond Diode Laser - PiLas Manual and Test Report, Jun 203.

[43] B.W. Adams et al. Measurements of the gain, time resolution, and spatial resolution of a 20×20 cm^2 MCP-based Picosecond Photo-Detector. *Nucl.Instr.Meth A*, 732:392, 2013.

[44] J.-F. Genat, G. Varner, F. Tang, and H.J. Frisch. Signal Processing for Pico-second Resolution Timing Measurements. *Nucl.Instr.Meth A*, 607:387–393, 2009.

[45] Fermilab Test-Beam Facility. `http://ppd.fnal.gov/ftbf/`.

[46] F. Cavanna et. al. LArIAT: Liquid Argon In A Testbeam. arXiv:1406.5560, 2014.

[47] T.J. Roberts and D.M. Kaplan. G4beamline simulation program for matter-dominated beamlines. In *Particle Accelerator Conference, 2007. PAC. IEEE*, pages 3468–3470, 2007.

[48] J.Defazio, Photonis USA. Private communication, 2015.

[49] A.S. Tremsin and O.H.W Siegmund. Spatial distribution of electron cloud footprints from microchannel plates: Measurements and modeling. *Review of Scientific Instruments*, 70(8):3282–3290, 1999.

[50] D. Breton, E. Delagnes, J. Maalmi, K. Nishimura, L.L. Ruckman, G. Varner, and J. Va'vra. High resolution photon timing with MCP-PMTs: A comparison of a commercial constant fraction discriminator (CFD) with the ASIC-based waveform digitizers TARGET and WaveCatcher. *Nucl.Instr.Meth A*, 629(1):123–132, 2011.

[51] S.A. Kleinfelder. Development of a switched capacitor based multi-channel transient waveform recording integrated circuit. *IEEE Trans. Nucl. Sci*, 35(1), Feb 1988.

[52] G. Haller and B. Wooley. A 700 MHz Switched Capacitor Analog Waveform Sampling Circuit. *SLAC-PUB-6414*, 1993.

[53] E. Delagnes, Y. Degerli, P. Goret, P. Naymana, F. Toussenel, and P. Vincent. SAM: A new GHz sampling ASIC for the H.E.S.S.-II Front-End Electronics. *Nucl.Instr.Meth A*, 567:21–26, 2006.

[54] K. Bechtol, S. Funk, A. Okumura, L. Ruckman, A. Simons, H. Tajima, J. Vandenbroucke, and G. Varner. TARGET: A Multi-Channel Digitizer Chip for Very-High-Energy Gamma-Ray Telescopes. *J. Astroparticle Physics*, 36:156–165, 2012.

[55] S.A. Kleinfelder. Gigahertz Waveform Sampling and Digitization Circuit Design and Implementation. *IEEE Trans. Nucl. Sci*, 50:156–165, 2003.

[56] G.S. Varner, P. Gorham, and J. Cao. Monolithic Multi-Channel GSa/s Transient Waveform Recorder for Measuring Radio Emissions from High Energy Particle Cascades. *Proc. SPIE Int. Soc. Opt. Eng*, 4858:31, 2003.

[57] C. Broennimann, R. Horisberger, and R. Schnyder. The Domino Sampling Chip: A 1.2 GHz Waveform Sampling CMOS Chip. *Nucl.Instr.Meth A*, 420:264–269, 1999.

[58] S. Ritt. The DRS Chip: Cheap Waveform Digitization in the GHz Range. *Nucl.Instr.Meth A*, 518:470–471, 2004.

[59] J. Milnes and J. Howorth. Picosecond Time Response Characteristics of Micro-channel Plate PMT Detectors. *SPIE USE*, 8 5580:89–100, 2009.

[60] P. Eraerds, M. Legré, A. Rochas, H. Zbinden, and N. Gisin. SiPM for fast Photon-Counting and Multiphoton Detection. *Optics Express*, 15:14539–14549, 2007.

[61] R.H. Dennard, F. H. Gaennsslen, H. N. Yu, V.L Rideout, E. Bassous, and A.R. LeBlanc. Design of Ion-Implemented MOSFETs with Very Small Physical Dimensions. *IEEE J. Solid-State Circuits*, SC-9:256–268, 1974.

[62] Y. Taur et. al. CMOS scaling into the nanometer regime. *Proc. IEEE*, 85(4):486–504, 1997.

[63] IBM Corporation. CMRF8SF Model Reference Guide, 2008. V.1.4.0.10.

[64] The MOSIS Service. Wafer Electrical Test Data and SPICE Model Parameters. Run: V18B. Available on-line (accessed 4 Feb. 2013). `http://www.mosis.com/pages/Technical/Testdata/ibm-013-prm`.

[65] E. Oberla, H. Grabas, M. Bogdan, H. Frisch, J.-F. Genat, K. Nishimura, G. Varner, and A. Wong. A 4-Channel Waveform Sampling ASIC in 0.13 μm CMOS for Front-End Readout of Large-Area Micro-Channel Plate Detectors. *Physics Procedia*, 37:1690–1698, 2012.

[66] M. Cooney, M. Andrew, K. Nishimura, L. Ruckman, G. Varner, H. Grabas, E. Oberla, and J.-F. Genat. Multipurpose Test Structures and Process Characterization using 0.13 μm CMOS: The CHAMP ASIC. *Physics Procedia*, 37:1699–1706, 2012.

[67] H. Chang et. al. A Wide-Range Delay-Locked Loop With a Fixed Latency of One Clock Cycle. *IEEE J. Solid-State Circuits*, 37:1021–1027, 2002.

[68] O. Milgrome, S. Kleinfelder, and M. Levi. A 12 Bit Analog to Digital Converter for VLSI Applications in Nuclear Science. *IEEE Trans. Nucl. Sci*, 39:771–775, 1992.