 Transmission-Line Readout with Good Time and Space Resolution for Large-Area MCP-PMTs

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- Summary & plan

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Introduction: Applications of Time-of-Flight for HEP

Courtesy of H. Frisch
Introduction: Planacon MCP-PMT Tube & Anode Array

- 1024 anode pads (1.1x1.1mm), with pitch of 1.6mm
- Pore Size 25μm
- Pores with gain of $10^5$-$10^6$

Charged Particle → Photon → Photoelectric cathode → Electron → Electron Shower → To Electronics

F. Tang
Characteristics of MCP-PMT Output Signal From Simulation

J-F. Genat’s simulation for a MCP-PMT with 25um pores to reproduce Jerry Va’Vra’s measurements at 50PEs, SN=80, Analog BW = 1.5GHz.
MCP-PMT Output Signal with Test Beam

Tube Dimension: 2x2 inches
Pore Size: 25um
Readout Techniques for Picoseconds Timing Measurements

**Graph:**
- Single Threshold
- Multiple Thresholds
- Constant-Fraction Discriminator
- Pulse Sampling (40Gsps)

**Time Resolution (ps)** vs **Number of Photoelectrons**

- Analog Bandwidth: 1.5GHz
- (based on 0.13um CMOS process)

Courtesy of J-F. Genat
Advantages of transmission-line and fast sampling techniques:

• Readout timing, position and energy information
• Good transmission-line bandwidth (up to 3.5GHz)
• Use many fewer readout channels (1024 down to 64 channels)
**Timing:**
(Sampling over the peak)

\[
t_0 = \frac{t_1 + t_2}{2}
\]

**Position:**

\[
x_i = \frac{t_1 - t_2}{t_1 + t_2}
\]

**Energy:**
(Full waveform sampling)

\[
E_i = q_1 + q_2
\]
Proposed Transmission-line Anode Board (top view)

32 microstrip $Z=50\,\Omega$ lines
Width=$1.1\,\text{mm}$
Pitch=$1.6\,\text{mm}$
Prototype Transmission-line Readout Board Design and Simulations Based on Commercial 2’x2’ 1024-Anode Tube

Interconnection:
1. Elastomer
2. Low-T solder (indium)
3. Conductive Epoxy
4. Ultimately capacitive coupling
Layout of Prototype Transmission-line Readout Board

Board Size: 130x60mm
Board Thickness: 1.2mm

Trace length: 5.36’, 4.83’, 3.97’

Tube Outline 58x58mm
Equal distributed 32 $C_L=100f$ along 2-inch line, it reduces impedance to $Z_0'$, however, it also reduced the BW.

$$Z_0' = \sqrt{\frac{L}{C + \alpha C_L}}$$

$$\alpha = \frac{nC_L}{\text{Length}}$$

$$\alpha C_L = 1.6p$$

$$\Delta t = 9.7\text{ps} < 0.5\tau$$

$$Z_0' \leq 50$$

$$BW \approx 3.5\text{GHz}$$

$$Tr = 2.2\tau = 2.2\frac{Z_0}{2} \alpha C_L \approx 100\text{ps}$$
System Modeling for Transmission-line Readout Simulation

Transmission-Line Anodes (Z₀')

Impedance discontinuity caused by vias and ball contacts

Via size: 15x10x5 mils
Board Thickness: h=62mils
Lv=0.3n, Cv=150f
Zvia=31.6Ω
Outputs on Each End of Transmission-line with Stub Anodes
(hit at pad-5)

Input Force:  \( Tr=tf=200 \text{ps} \)

Output on left_end (t1)

Output on right_end (t2)

Reflection caused by impedance mismatch and discontinuity

Electrons
Outputs on Each End of Transmission-line with Stub Anodes (hit at pad-16)

Input on Pad-16

Out_L
Out_R

Outputs on Each End of Transmission-line with Stub Anodes (hit at pad-16)

Baseline settled after a few ns

tr=tf=100ps
Outputs on Each End of Transmission-line without Stub Anodes (hit at the same position as pad-16)
Simulation Goal:
To understand analog signal bandwidth vs. the length of transmission-line for MCP anode design.

System Setup:
The simulation model is extracted from a board layout. The transmission-line impedance $Z=50$ ohms, the length is 48-inch with 4824 tapped anodes which induce 100f capacitance each.

Input Force:
A step voltage input force with a rise time of 100ps, an amplitude of 1.4V excites the line at the point 1-inch from the left end.

Outputs:
Comparing the rise time between both ends of the line.
Responses on each end of 48-inch transmission-line
(Hit at the position 1-ch to the left)

Input Force $T_r=100\text{ps}$

Output on Right (47-inch to the source)

Output on Left (1-inch to the source)

$T_r=319\text{ps}$ measured by simulation tool.
Corresponding to analog bandwidth of $1.15\text{GHz}$
Conceptual Design of Transmission-line and Fast Sampling Readout Electronics

Only 64-ch readout electronics needed!

64-CH
40Gsps
Analog Sampling Chips

FPGA

Cable Conn
Summary

Advantages:

- Readout timing, position and energy information (more applications)
- Use many fewer readout electronics channels
- Good signal bandwidth
- Easy to match impedance all the way to the chip input

Plans (short and long term):

- Prototype test with laser stand and 40Gsp s scope is in process
- Transmission-line readout with two LAB2 or two DRS4 Chips (possibly 2x interleaving?)

- Development of 40Gsp s sampling chip for large scale detectors (underway).
- Built-in transmission-line anode design and simulation (need to work with tube designers)