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Preliminary Specifications for a 1-Picosecond Resolution ASIC for the FTBF TOF System

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Dedicated to the Memory of Anatoly Ronzhin

Abstract

We present draft specifications for a fast-timing ASIC with 1 picosecond resolution. MCP-PMTs have achieved 5-psec resolution for charged particles generating Cherenkov light at the entrance window [1]. Since then a better understanding of the factors that limit the timing resolution has been documented [2], with the prediction that a 3 GHz system bandwidth should further improve the resolution. Here we present draft specs of an ASIC that does for timing what the QIE did for energy resolution. The multi-channel chip is intended to be used in the upgrade to the TOF system at the Fermilab Test Beam Facility (FTBF), with a goal of a 1-psec intrinsic resolution for the electronics system. The high-frequency design requires treating the signal propagation through the MCP-PMT amplification chain, anode signal generation and pickup, cabling and PC-board connections, and ASIC digitization as an integrated matched RF system. Candidate architectures include both constant-fraction discriminator (CFD) and wave-form sampling (WFS) designs.

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1 Introduction

We have drafted specifications for a fast-timing front-end ASIC with 1 picosecond resolution. MCP-PMTs have achieved 5-psec resolution for charged particles generating Cherenkov light at the entrance window [1]. Since then a better understanding of the factors that limit the timing resolution has been documented [2]. Here we present draft specs of an ASIC that does for timing what the QIE did for energy resolution. The multi-channel chip is intended to be used in the upgrade to the TOF system at the Fermilab Test Beam Facility (FTBF), with a goal of a 1-psec intrinsic resolution for the overall electronics system.

The structure of this little note is as follows: Section 2 presents the case for 1 picosecond time resolution, with the motivation in Subsection 2.1 and a brief introduction to the limiting factors in Section 2.2. A draft table of the ASIC specifications is presented in Section 3. Section 4 makes the case for wave-form sampling as the architecture for the ASIC. Section 5 is a short bibliography of selected fast-timing literature.

2 The 1 Picosecond challenge

2.1 Motivation and Payoff at the FTBF

Measuring the response of calorimetric detectors is a primary task of the TestBeam. The response is dependent on particle type, with, for example, the difference between K- and anti-protons being the most striking [1]. Particle ID at the TB will be much appreciated as LHC measurements get more and more precise and high-performance detectors at future colliders are prototyped. Figure 1 shows the contours of $\pi - K$ TOF differences as a function of momentum and the separation of the 2 TOF detector stations in the TB [4].

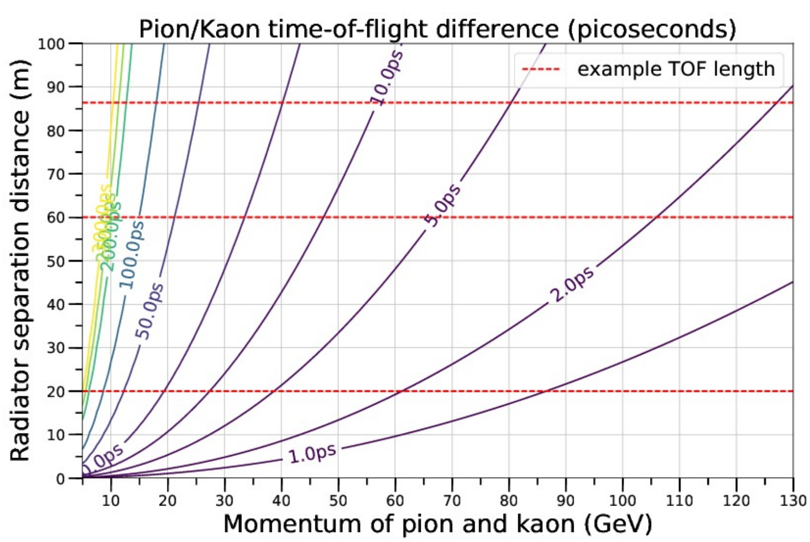

Figure 1: The contours of $\pi - K$ TOF differences as a function of momentum and the separation of the 2 TOF detector stations in the TB (Evan Angelico [4])

Applications other than charged particle ID for 1 psec resolution include:

[1]The K- with s and a $\bar{u}$ valence quarks is much smaller than the $\bar{p}$ with 2 $\bar{u}$ and one $\bar{d}$ quarks, and so has a much longer interaction length.

1. Identifying secondary and tertiary displaced vertices from heavy parents in colliders;
2. Rejecting combinatoric backgrounds from mis-associated gammas in rare kaon decay experiments;
3. Searches in rare η decay experiments such as RedTop;
4. Development of inexpensive compact muon TOF detectors for precision neutrino flux measurements;
5. Precision testbed for development of fast timing photodetectors and electronics.

2.2 Limiting Factors on the Resolution

Table 2 shows the predictions of Stefan Ritt's simple (but well-motivated) rule-of-thumb rule that the resolution currently depends on two parameters, the signal-to-noise (S/N) and the bandwidth [3]. The bottom row motivates the choice of bandwidth.

Signal	Noise	Sampling	Bandwidth	Resolution
U	Δu	f_s	f_{3db}	Δt
100 mV	1 mV	2 GSPS	300 MHz	~10 ps
1 V	1 mV	2 GSPS	300 MHz	1 ps
100 mV	1 mV	20 GSPS	3 GHz	0.7 ps
1V	1 mV	10 GSPS	3 GHz	$\boxed{0.1 \text{ ps}}$!
LAPPD: 1V	0.7 mv	15 GS/sec	1.5 GHz	??

Figure 2: Stefan Ritt's table of predictions from his 'rule-of-thumb'. See Stefan's talk in Session 5 at https://psec.uchicago.edu/workshops/fast_timing_conf_2011/

We believe a 1 ps goal is credible with an increased system bandwidth and a custom ASIC-based electronics system capable of 1 ps resolution. Using a MCP-PMT, Ohshima measured a time resolution for charged particles traversing a radiator of 5 ps in 2006 [1]. We have learned a lot since then [4].

3 Draft Table of ASIC Specifications

Parameter	Min Value	Max Value	Units	Comment
Front-end				
Analog Bandwidth	3	–	GHz	1ps resolution per S. Ritt, [3]
Input	–	-	–	Single-ended (bypass gd to MCP2-out)
Input impedance	50	200	Ohms	50 for current strips
Voltage Range	300	1000	mv	Max signal: S/N>>100
Noise	–	1	mv	1ps resolution per S. Ritt, [3]
Charge Range	3.2	160	pC	Max integrated charge
Charge Resolution	10	10	bits	set by 10% of 1% sharing
Cross-talk	–	0.1	%	?? channel-channel
Linearity	–	0.1	%	after calibration
2-pulse separation	1	–	nsec	(CFD) 1-foot unterminated strip far end
Trigger threshld	1	FS	mv	one per channel
Trigger latency	–	10	nsec	WAG- negotiable if needed
Temperature Coeff.	–	10^{-6}	%/degC	1ps FS for 10 degC
Max Time Recorded	–	12	μs	5 muon lifetimes??
Readout Buffers	4	–	–	parallel buffers
Channels/ASIC	8	–	–	negotiable
Power	==	???	mW	per chip, full rate
System and DAQ				
Digitization Time	–	20	μs ???	multiple buffers, 200 KHz
Readout Rate	200	–	kHz	Set by MTest
Strips or Pads	–	–	–	Either: Capacitive Coupling Pickup
MCP Current return	–	–	–	Bypass caps to MCP-2 out
Channels/FE card	32	64	channels	30 strips or 64 pads??
Local Sparsification	–	–	–	Yes
System # of channels	30	384	channels	1 strip MCP to 6 pad MCPs
Clock	–	–	–	External; White Rabbit compatible
Clock Jitter	–	10^{-12}	–	1 ps/s; e.g. WR PPS

Table 1: A draft of specs for the 1-ps upgrade to the FTFB TOF system. FE refers to a possible Front-End card; BE refers to a Back-End card. The implemented architecture may differ. Note that the 3 GHz analog bandwidth spec refers to the complete FE system (path) and not just the ASIC.

References

[1] K. Inami, N. Kishimoto, Y. Enari, M. Nagamine, and T. Ohshima; *A 5-ps Tof-counter with an MCP-PMT*; Nucl. Instr. Meth. A560, p.303, 2006

[2] See the talks by D. Breton, E. Delanges, and S. Ritt in *The Factors that Limit Time Resolution in Photodetectors*; Workshop, University of Chicago, Chicago, IL; 28-29 April 2011. See *h*ttp://psec.uchicago.edu/workshops/.

[3] See S. Ritt in Session 5 of the Workshop *The Factors that Limit Time Resolution in Photodetectors*, Univ. of Chicago; April 2011; https://psec.uchicago.edu/workshops/fast_timing_conf_2011/

[4] E. Angelico; *Development of Large-Area MCP-PMT Photo-Detectors for a Precision Time-Of-Flight System at the Fermilab Test Beam Facility*; Ph.D thesis, The University of Chicago. ProQuest Dissertations Publishing, 2020. 28023552.

4 Appendix A: The Unique Capabilities of Multi-Buffered Wave-Form Sampling

One possibility for the front-end of the Time-of-Flight Upgrade at the TestBeam is Eric Oberla's PSEC4A architecture [1] of a short sampling buffer that feeds multiple digization buffers for waveform sampling (WFS) for the TestBeam application.

The idea is to limit the number of channels that have to be calibrated and for which calibrations have to be kept in databases. In addition to problems maintaining a stable calibration, a long buffer also suffers from cumulative errors as each channel starts at the end of the previous one. Instead, the PSEC4A-like architecture is a short (e.g. 1024 samples) ring buffer with internal triggering that transfers the sampling buffer to one of 4 parallel digitizing buffers. The transfer would be time-stamped so that the effective buffer length (i.e. sensitive time) can be as long as there are bits to encode the cycle when triggered[2]. As long as at least one buffer is free when a trigger occurs, the operation is dead-timeless.

While there is much more initial overhead over a CFD architecture, advantages of WFS over other techniques [2] include:

1. For each pulse there is shape and time information, and so one can iteratively optimize the timing in analysis offline as opposed to thresholds set a priori;
2. Baseline shifts due to cross-talk, pile-up, ground problems, and RF interference can be identified and characterized from the baselines before and after the pulse.
3. While a CFD on average can produce results comparable to WFS [2], low occurrence environmental events such as RF noise, power glitches, baseline shifts, pileup, bad channels, and non-uniformities in the readout (e.g. anode edge strips) can put events into the tails of distributions, where they may have a significance beyond their small numbers (e.g. high-momentum K-).

[2]This is much like the highlighted little window on an oscilloscope that can be moved along the trace and then expanded.

4. A precise method of determining time and position that also cancels out some calibration issues, and lowers channel count, is to use anode strip-lines with single-ended operation- one end is unterminated so that the direct pulse and the reflected pulse from a strip are digitized on the same channel. In his thesis [3, 4] Eric used autocorrelation of the waveform to get the offset between the direct and reflected pulse; the difference gives the position and the average gives the time. Because both pulses are measured on the same channel less than a few nsec apart, channel-to-channel time calibrations do not enter.
5. While a comparable technique can be done with CFDs, with WFS a calibration sine wave can be digitized in one channel per card or per chip to provide direct measurement of the time basis, frequency response and system integrity.

Front-end				
Parameter	Min Value	Max Value	Units	Comment
Sampling Rate	20	40	Gs/sec	$\geq$ 4 samples on a 200 psec risetime
Buffer Length	512	2048	–	50 ns at 20 GS/s
# of Readout Buffers	4	4	–	

Table 2: Additional draft specs for a WFS implementation of the 1-ps upgrade to the FTFB TOF system.

References

[1] E. Oberla, J. Porter, and J. Stahoviak; *PSEC4A : A 10 GSa/s Waveform Sampling ASIC with Multi-Event Buffering Capability*; Proceedings of TWEPP 2018; Antwerp, Belgium (Sept. 2018)
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[3] E. Oberla and H.J. Frisch; *Charged particle tracking in a water Cherenkov optical time-projection chamber*, Nucl. Inst. Meth. Phys. Res. A. Volume 814, 1 April 2016,

[4] E. Oberla, *Charged Particle Tracking in a Water Cherenkov Optical Time Projection Chamber*, Ph.D Dissertation, University of Chicago, Aug. 2015

5 Appendix B: A Guide to Literature Relevant to the FTBF TOF Upgrade.

A guide to literature relevant to the FTBF TOF Upgrade. All of these should be available in the Psec Document Library; See http://psec.uchicago.edu/library/doclib/. The DocLib is searchable by Group, Category, and Author (tho these are self-assigned and so not to be trusted entirely); for example, to learn about the RF characteristics of strip-line anodes, search by Author on Tang.

Fast Timing

1. T. Credo, H. Frisch, H. Sanders, R. Schroll, and F. Tang; *Picosecond Time-of-Flight Measurement for Colliders Using Cherenkov Light* Proceedings of the IEEE, Rome, Italy, Oct. 2004; Nuclear Science Symposium Conference Record, 2004 IEEE, Vol. 1.
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Nucl. Instr. Meth. A71, pp124-131, (May 2013)

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A 15 GSa/s, 1.5 GHz Bandwidth Waveform Digitizing ASIC;
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2. M. Bogdan, H. Frisch, M. Heintz, A. Paramonov, H. Sanders, S. Chappa, R. DeMaat, R. Klein, T. Miao,P. Wilson, T. J. Phillips;
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2. *Meson Test Beam Cherenkov Counter Gas and Vacuum System Documentation*; 3/5/07; http://psec.uchicago.edu/library/Cherenkov_Counters_MTest
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