Picosecond Time Stretcher and Time-to-Amplitude Converter Design and Simulations

Fukun Tang
Enrico Fermi Institute, The University of Chicago

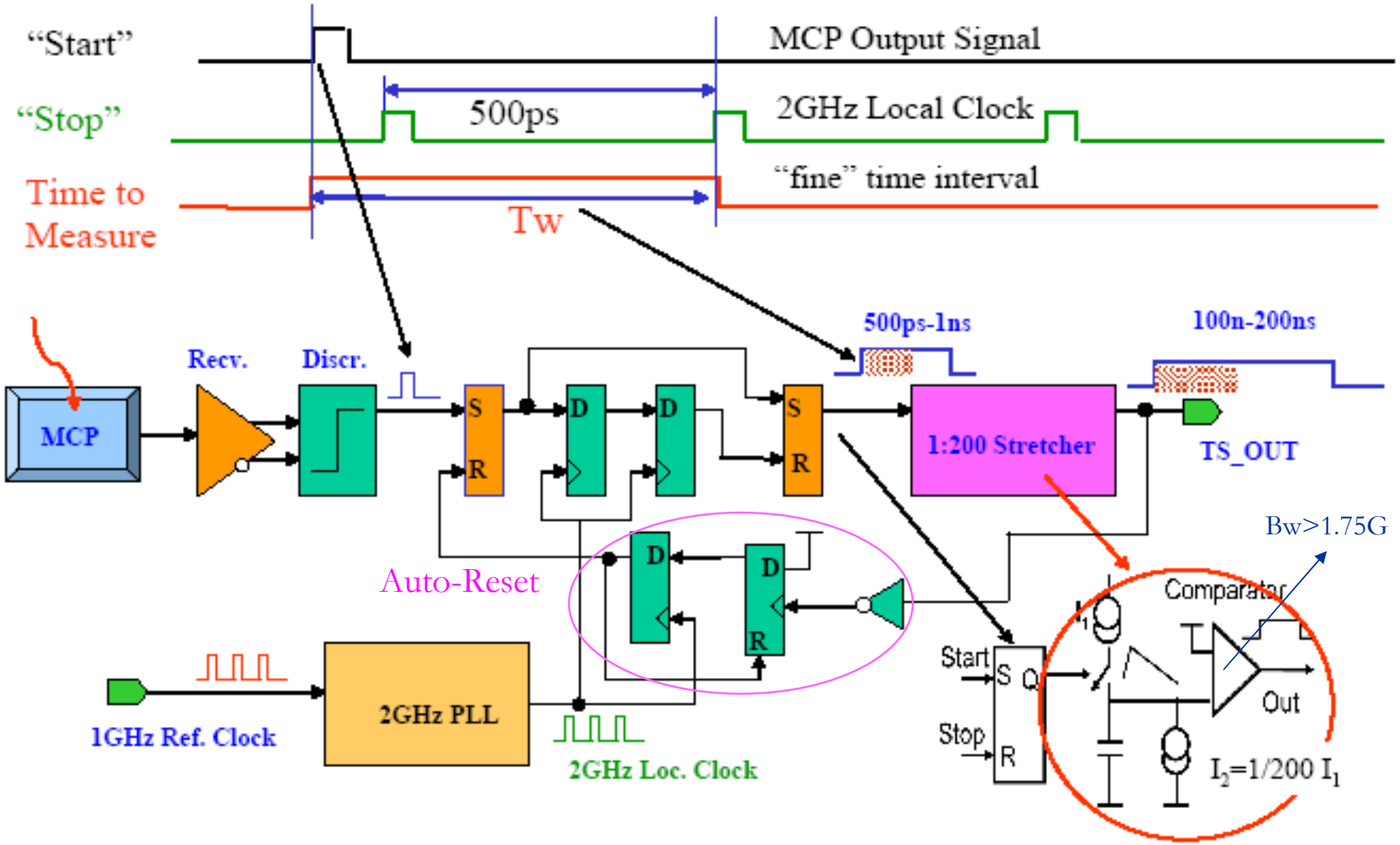
- Introduction

- Proposed Picosecond (pSec) Time Stretcher
- pSec Time Stretcher System Configuration
- pSec Stretcher Simulation Results
- The limitation of the pSec Time Stretcher

- Proposed pSec Time-to-Amplitude Converter (TAC)
- pSec TAC System Configuration
- pSec TAC Simulation Results

- Summary

Proposed Time Stretcher Diagram



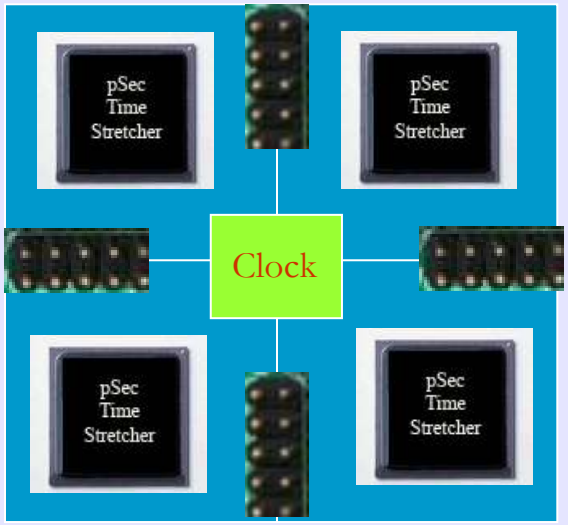
Time Stretcher System Configuration (Prototype)

DAQ → FE BOARD
SYS. CK (LVPECL) (1)

FE → DAQ BOARD
TS_OUT (LVPECL) (4)
(Crucial, signal integrity is required)

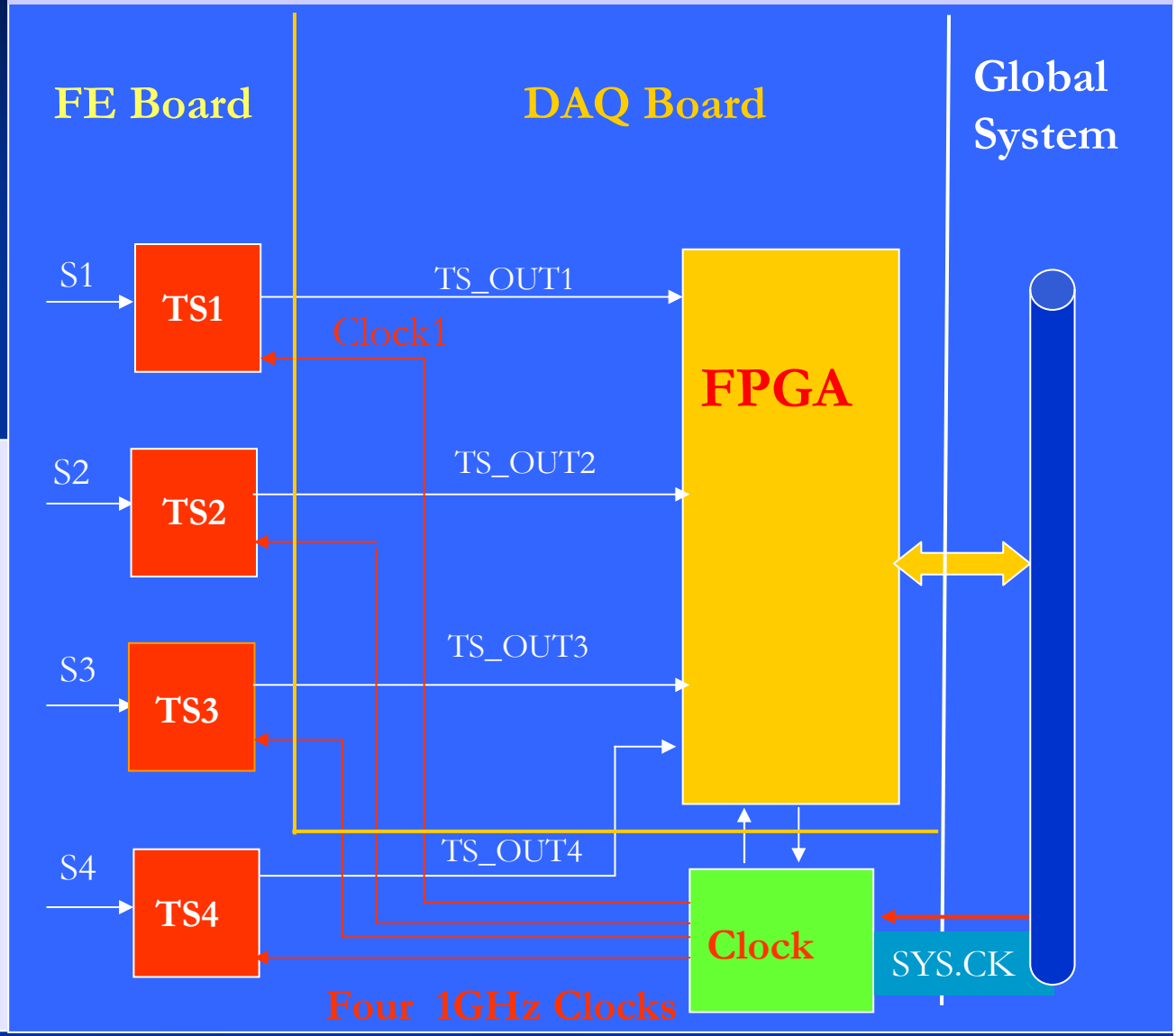
+2.5V, - 1.2V, AGND (3+)
+1.2V, DGND (2+)

Anode/FE Board



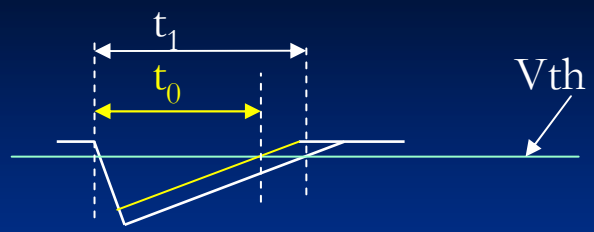
Thanks to John for the spec.

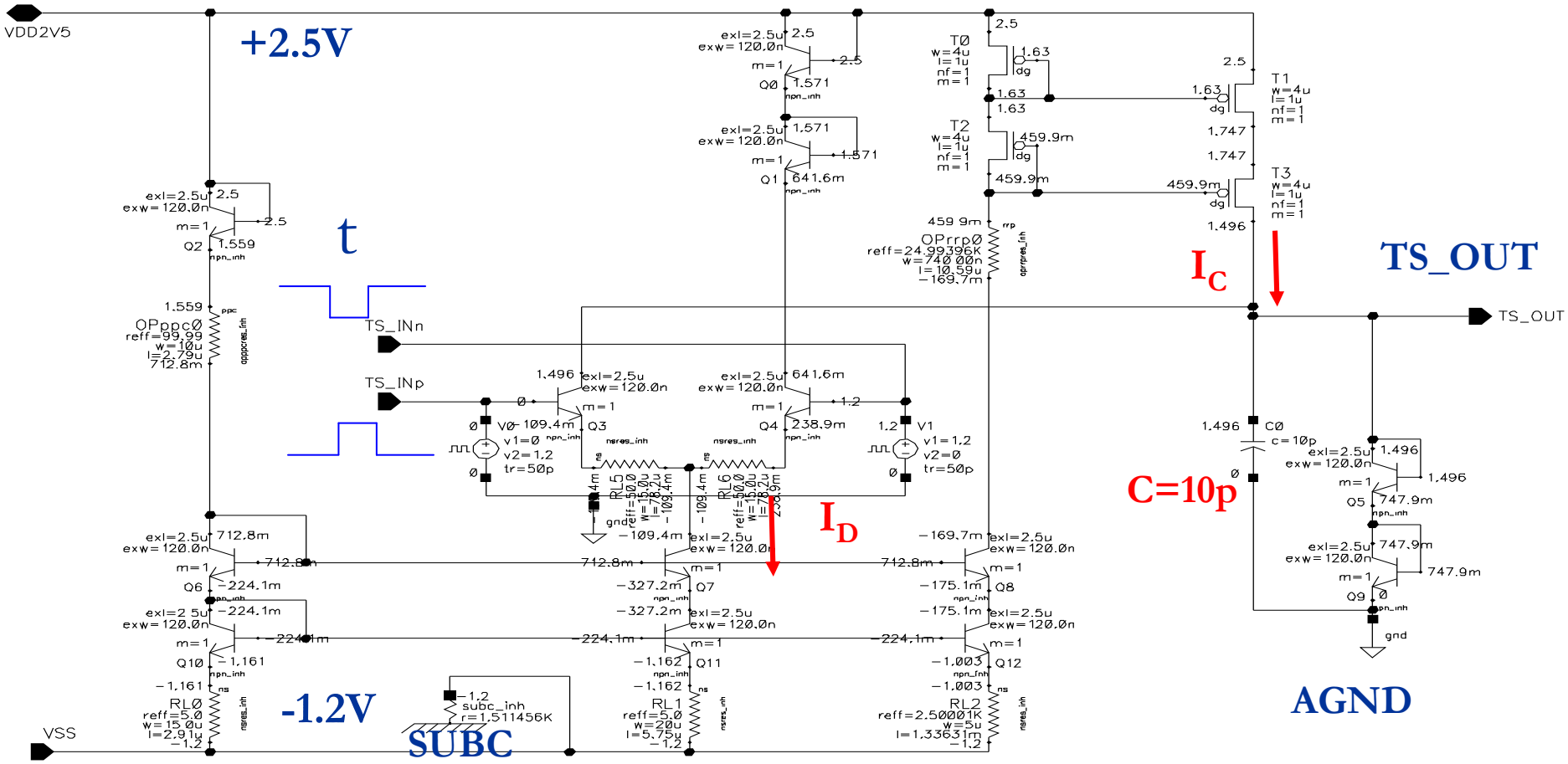
Signal Interconnection between FE and DAQ



Time Stretcher Design (IBM SiGe BiCMOS8HP)

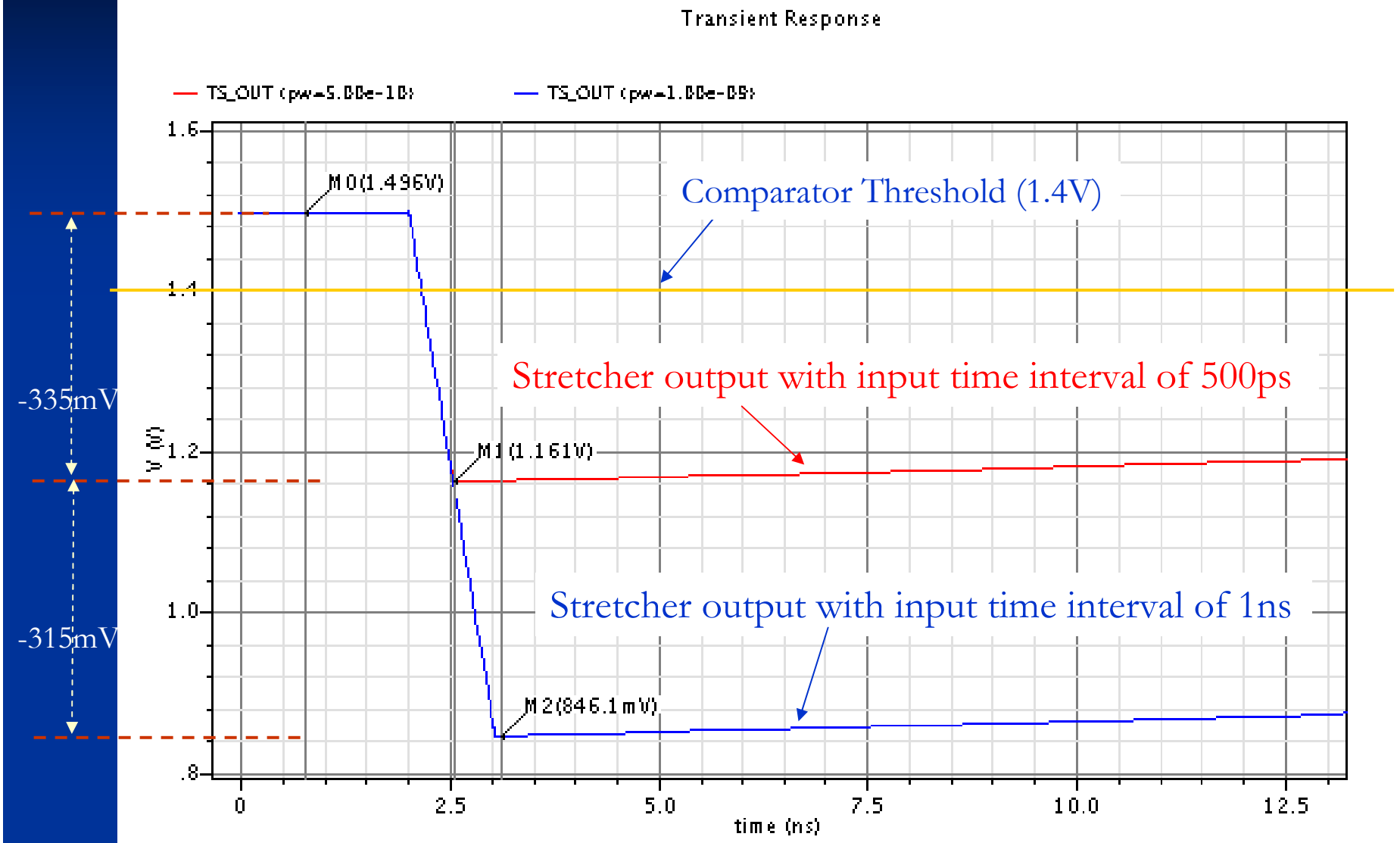
$$Tts\_out = \frac{I_D - I_C}{I_C} \cdot t$$



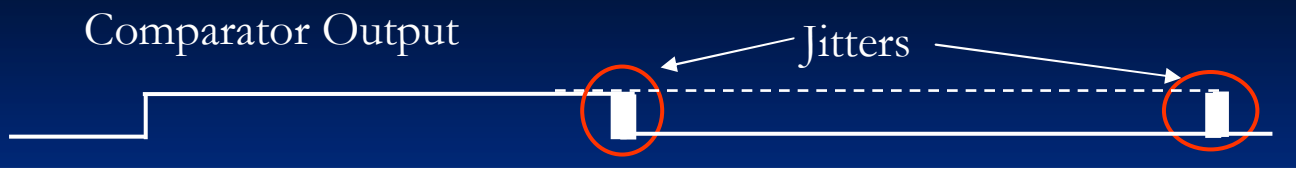


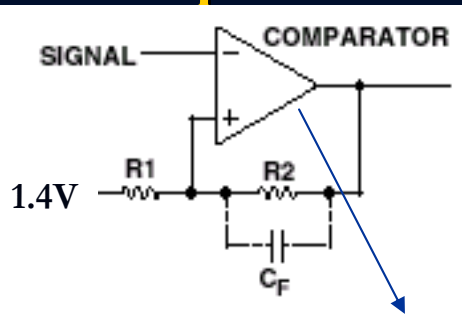
Time Stretcher Output Waveforms

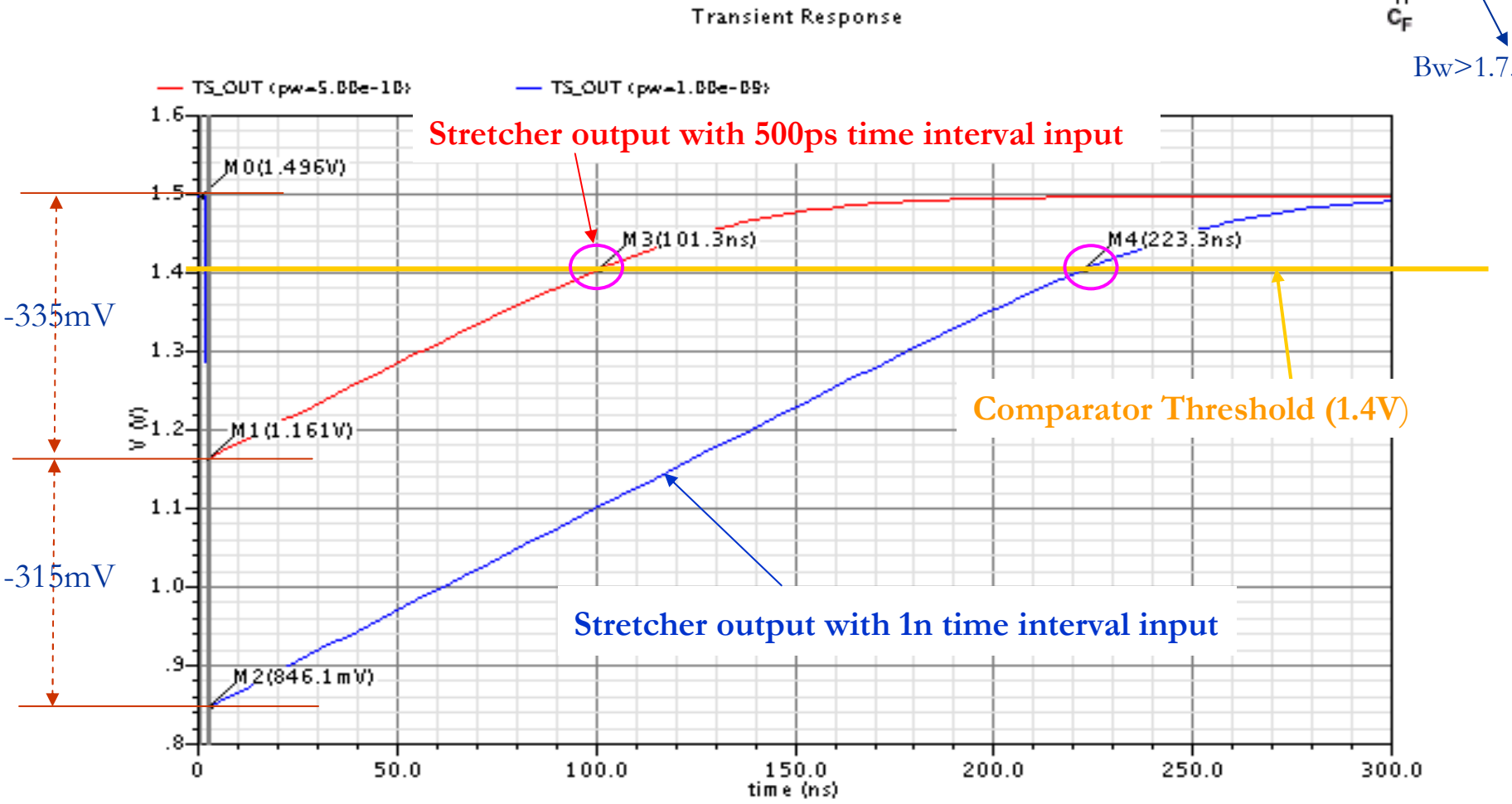
Input time interval from 500ps to 1n with 500ps step



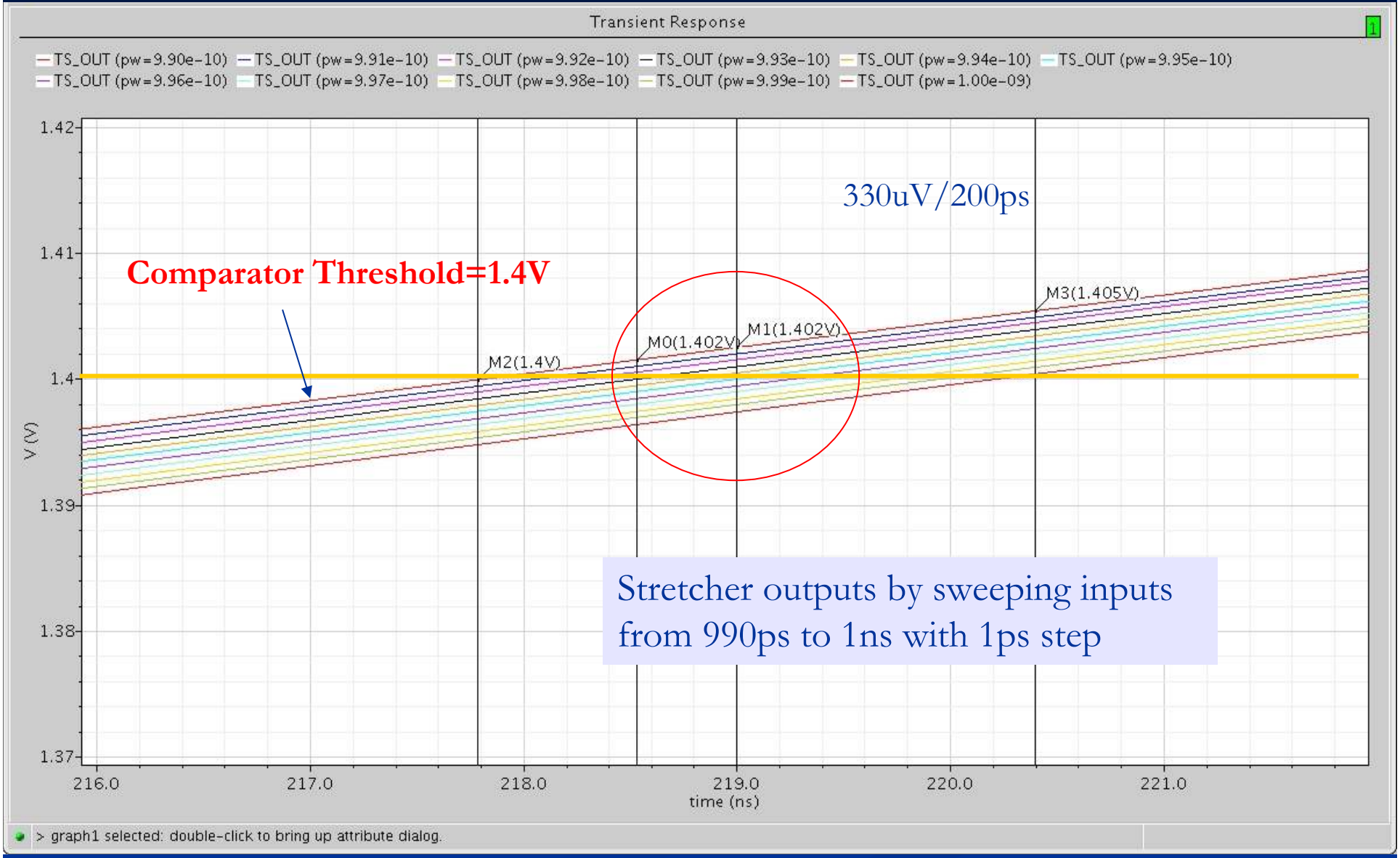
Stretched Time Interval and Comparator Output



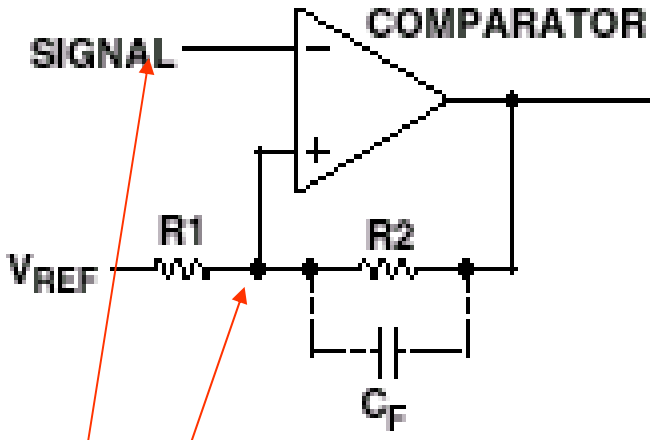




Slew Rate of the Time Stretcher Output



Design of Comparator with Hysteretic Threshold for Slow Slew Rate Input Signal



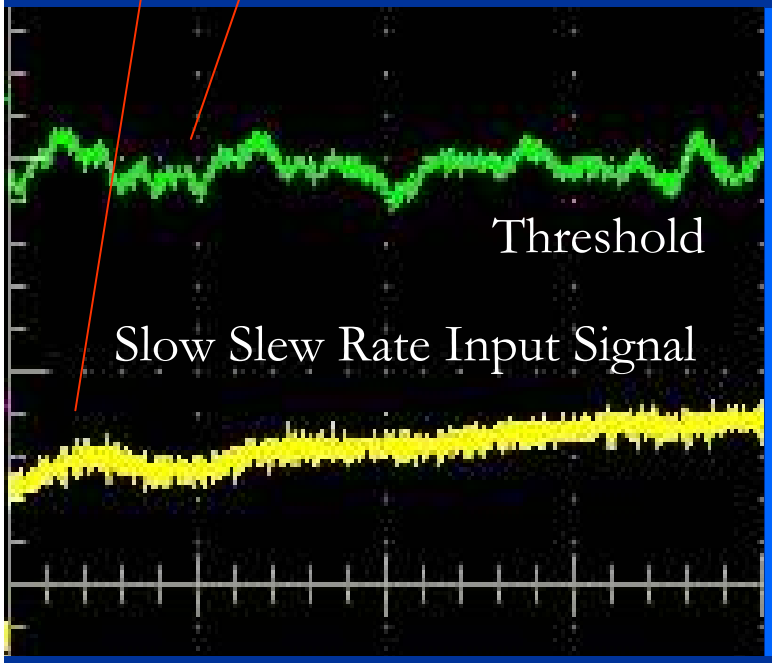
3 Major Factors With Comparator Design

(1) Timing Jitter ---- Noise & dv/dt

(2) Time Walk ---- Amplitude variations

(3) Drift ---- Rate & long term stability

Don't forget the crosstalk !



$$\text{Comparator Jitter} = \frac{Vn}{dv/dt}$$

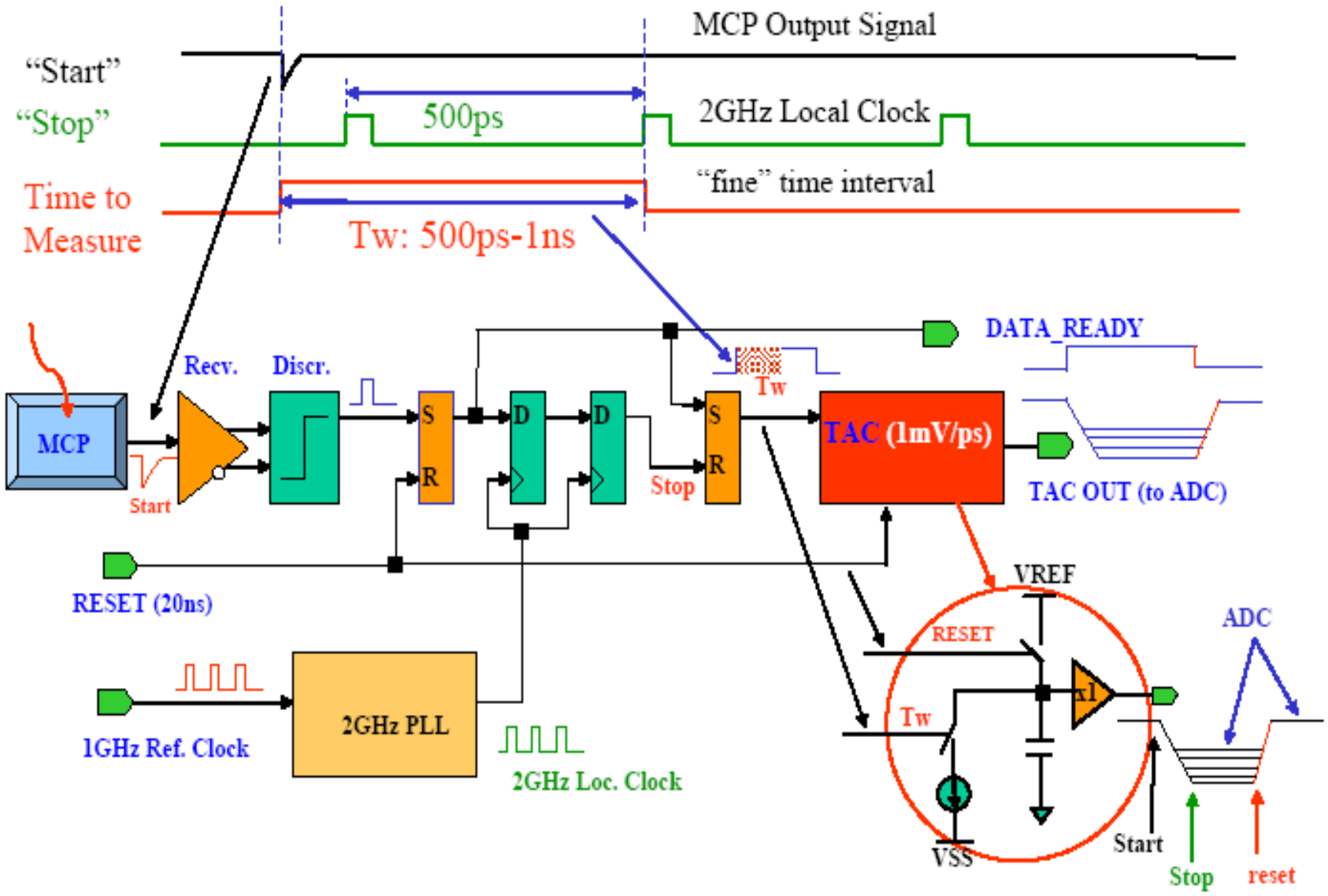
Vn: Total noise from input signal and comparator over the bandwidth.

dv/dt: Input signal slew rate (slope).

The limitations of the Time Stretcher

- A minimum bandwidth of 1.75 Ghz comparator is required for the DAQ digitizer with 200ps LSB. (high speed, high power, high crosstalk).
- The slew rate (dv/dt) of the stretched analog signal is too small. (330uV/200ps) comparing to the bandwidth of the comparator.
- The comparator threshold requires noise immunization and crosstalk rejection better than 330uV when input signal crosses the threshold.
- Frequent calibration may be required because threshold drift causing by the input signal rate and temperature variations.
- Lot of techniques are required to prevent the comparator from oscillating when the slow signal cross the threshold of an ultra-fast comparator (>1.75GHz).
- The estimated timing jitter missed our initial goal (1ps), based on the analysis of the electronics intrinsic noise, possible crosstalk and power supply noise both on stretched analog signal and the comparator threshold.

Proposed Time-to-Amplitude Converter (TAC)



Time Stretcher System Configuration (Prototype)

DAQ → FE BOARD

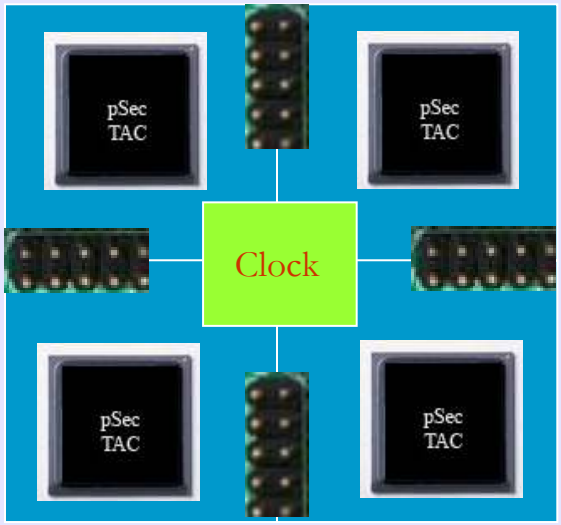
SYS. CK	(LVPECL)	(1)
Reset	(LVCMOS)	(4)

FE → DAQ BOARD

DATA_READY	(LVCMOS)	(4)
TAC_OUT	(DC)	(4)

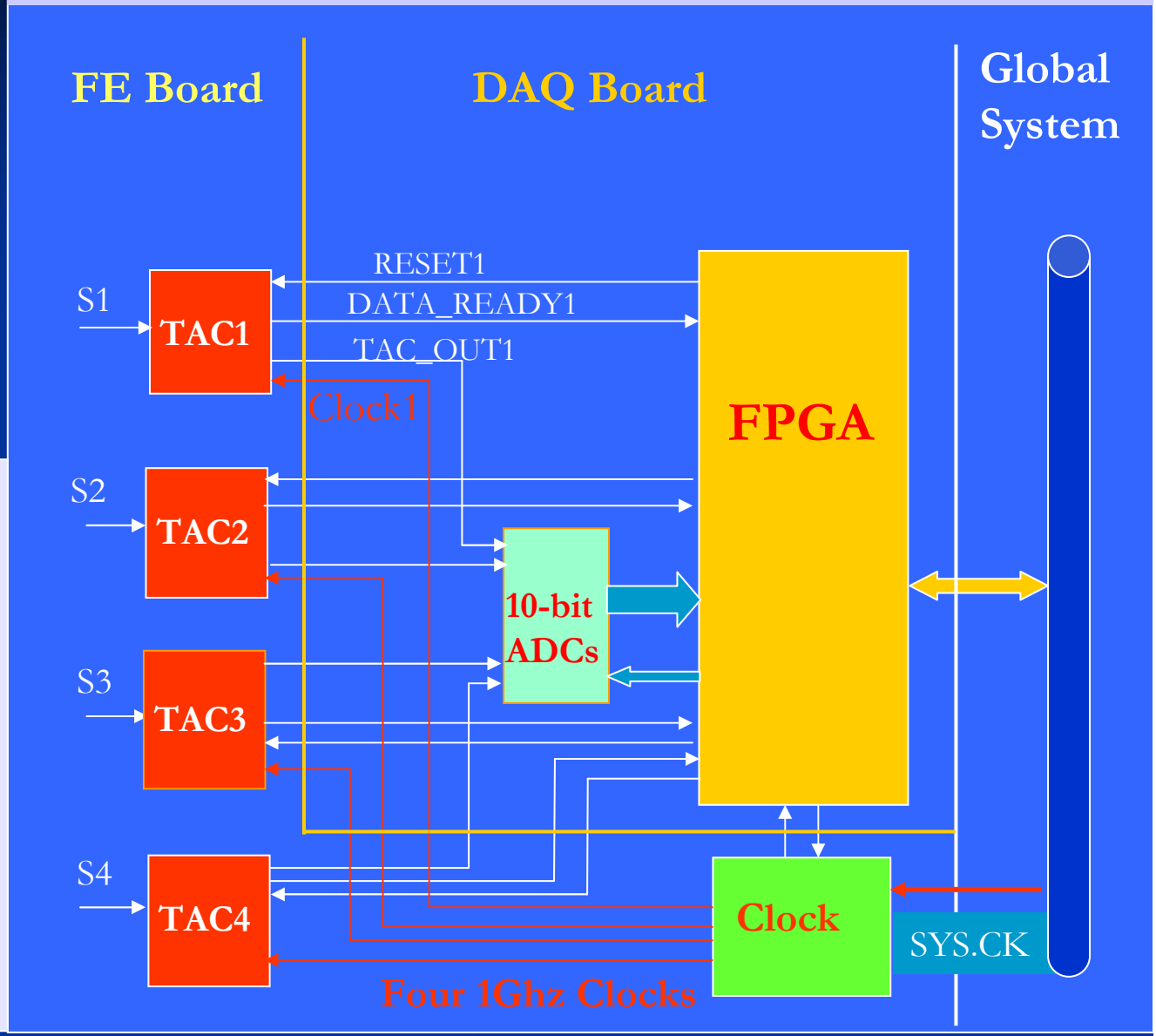
+2.5V, - 1.2V, AGND	(3+)
+1.2V, DGND	(2+)

Anode/FE Board



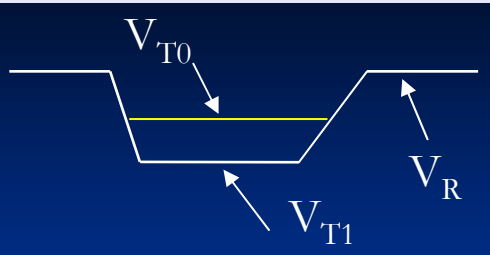
Thanks to John for the spec.

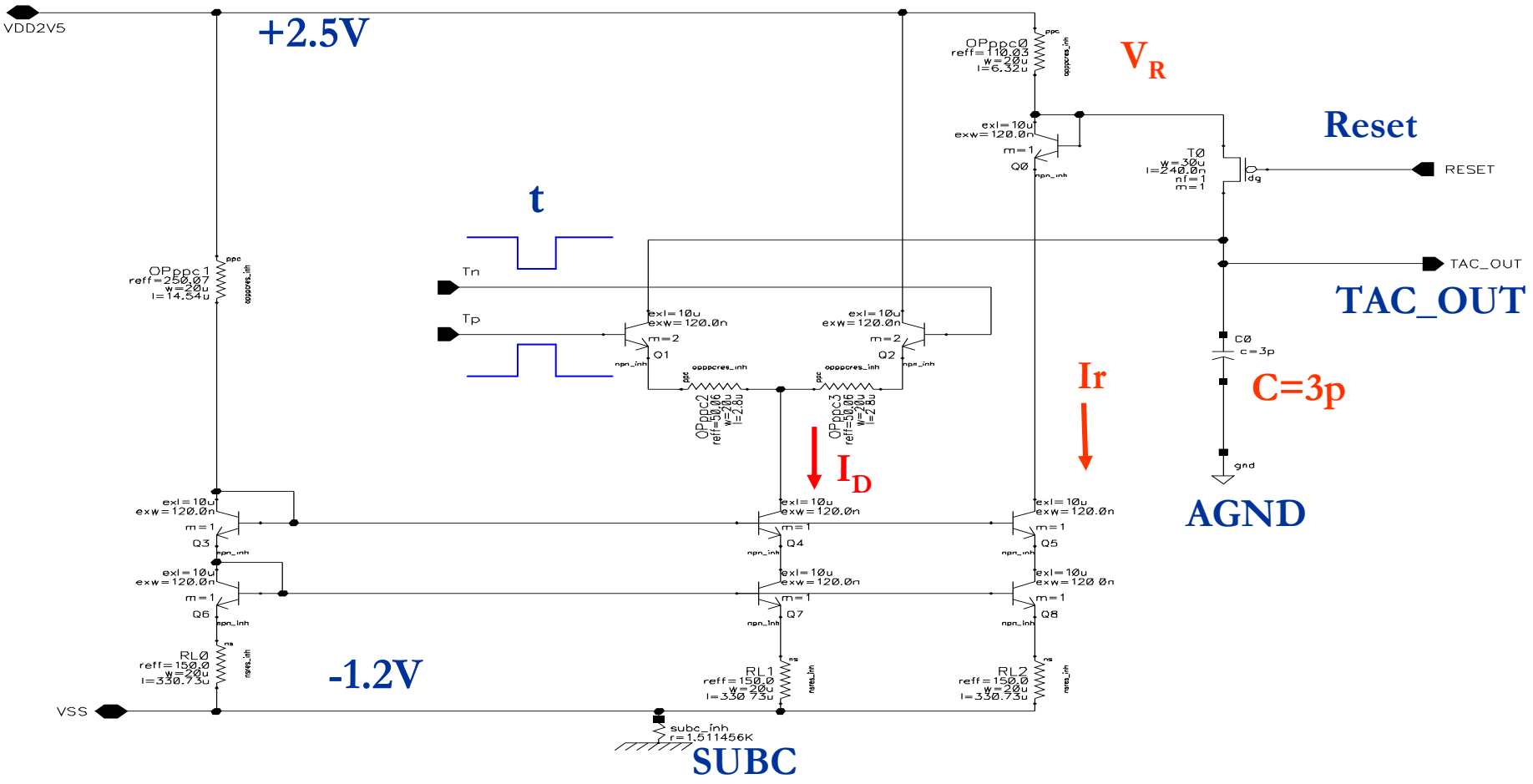
Signal Interconnection between FE and DAQ



TAC Design (IBM SiGe BiCMOS8HP)

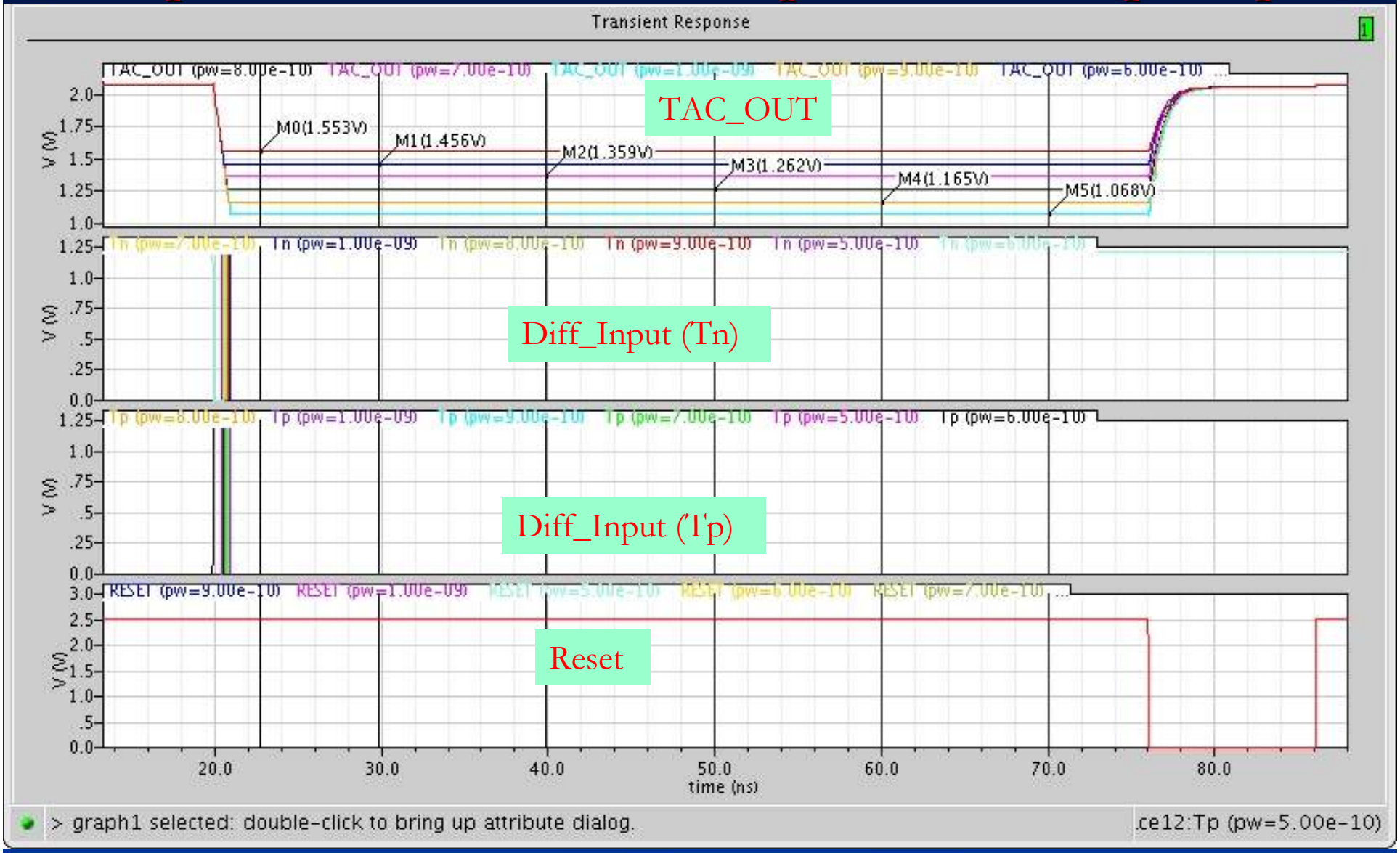
$$V_{TAC\_OUT} = V_R - \frac{I_D \cdot t}{C}$$





TAC Simulation

Input time intervals from 500ps-1ns with 100ps step

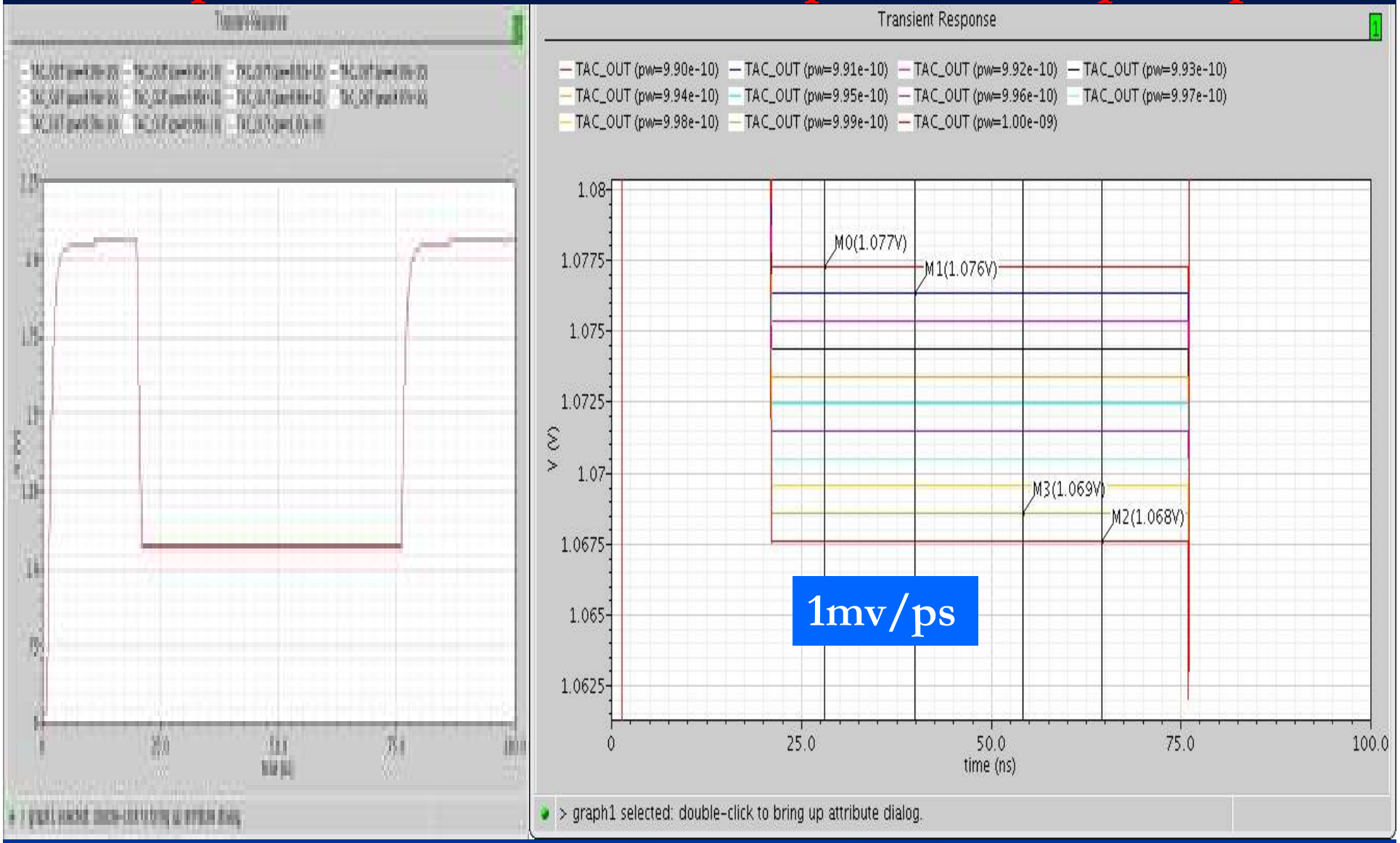


TAC Simulation

Input time intervals from 500ps to 1ns with 100ps step

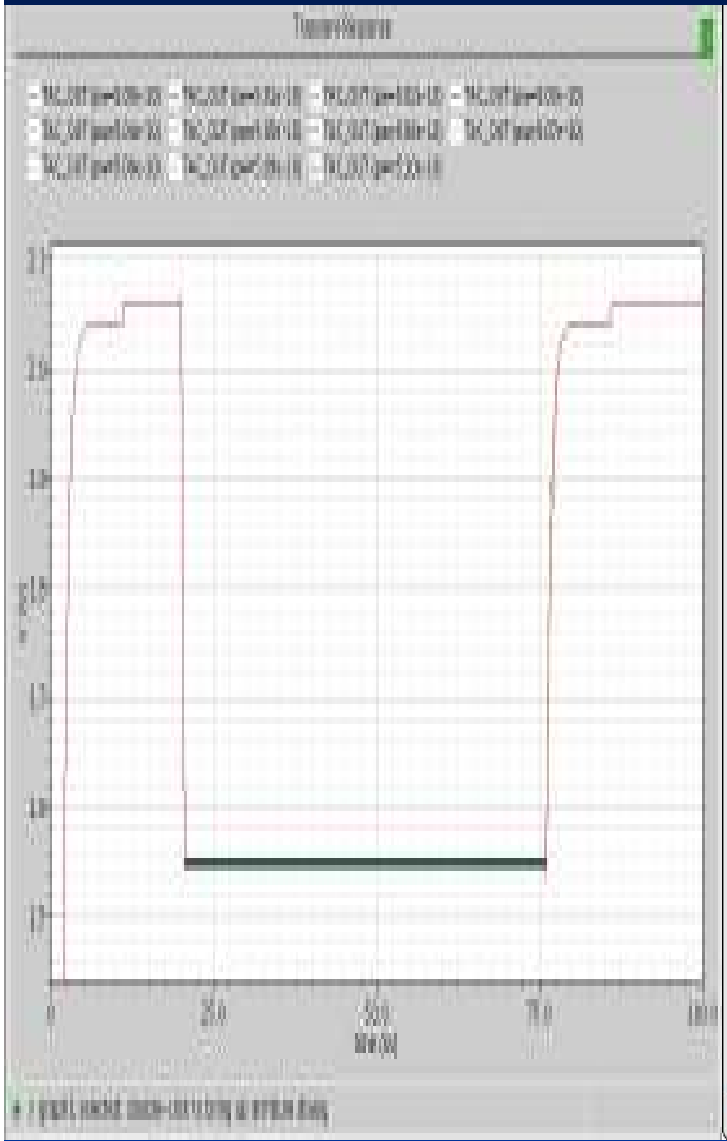
TAC Simulation

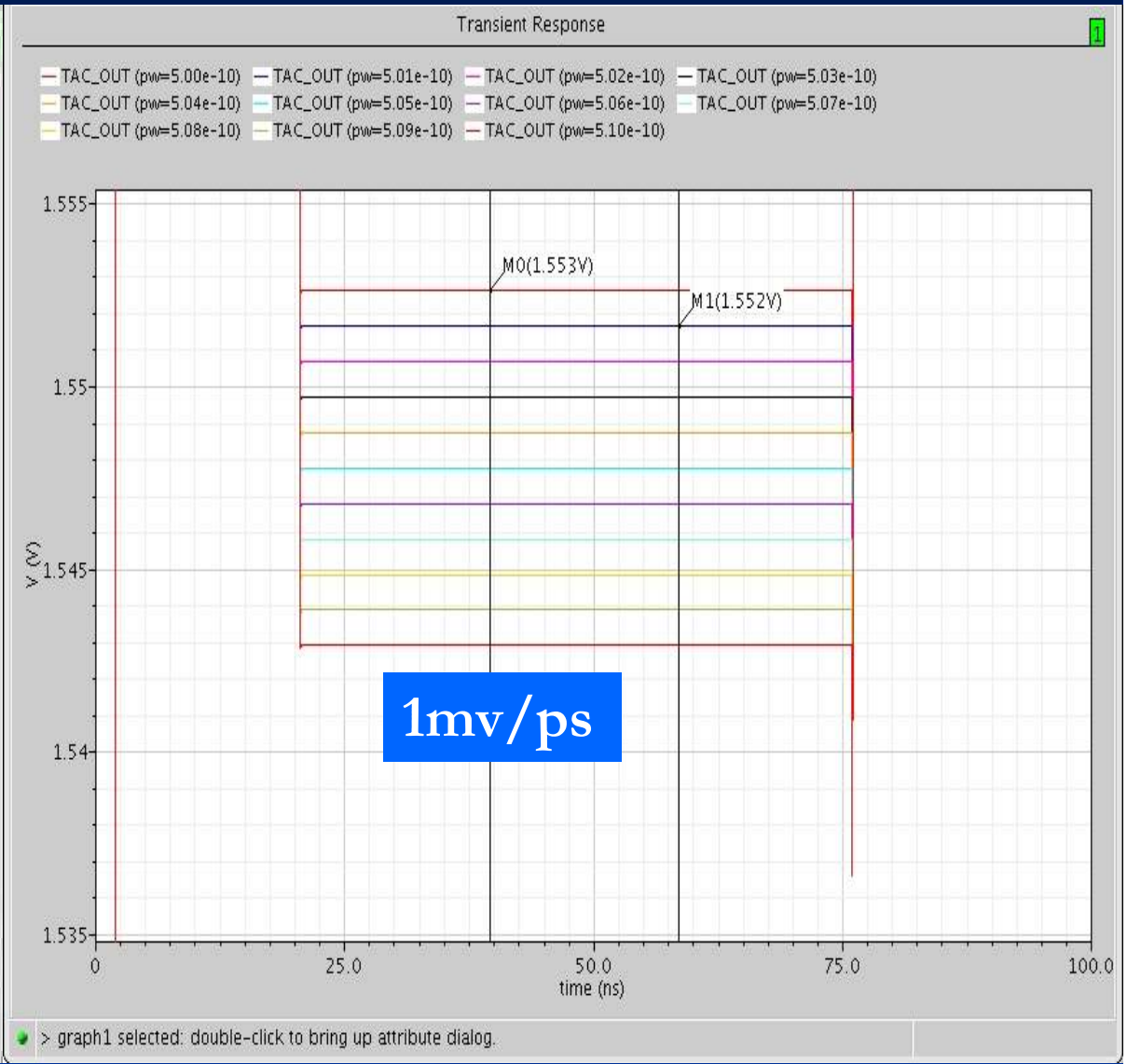
Input time intervals from 990ps-1ns with 1ps step



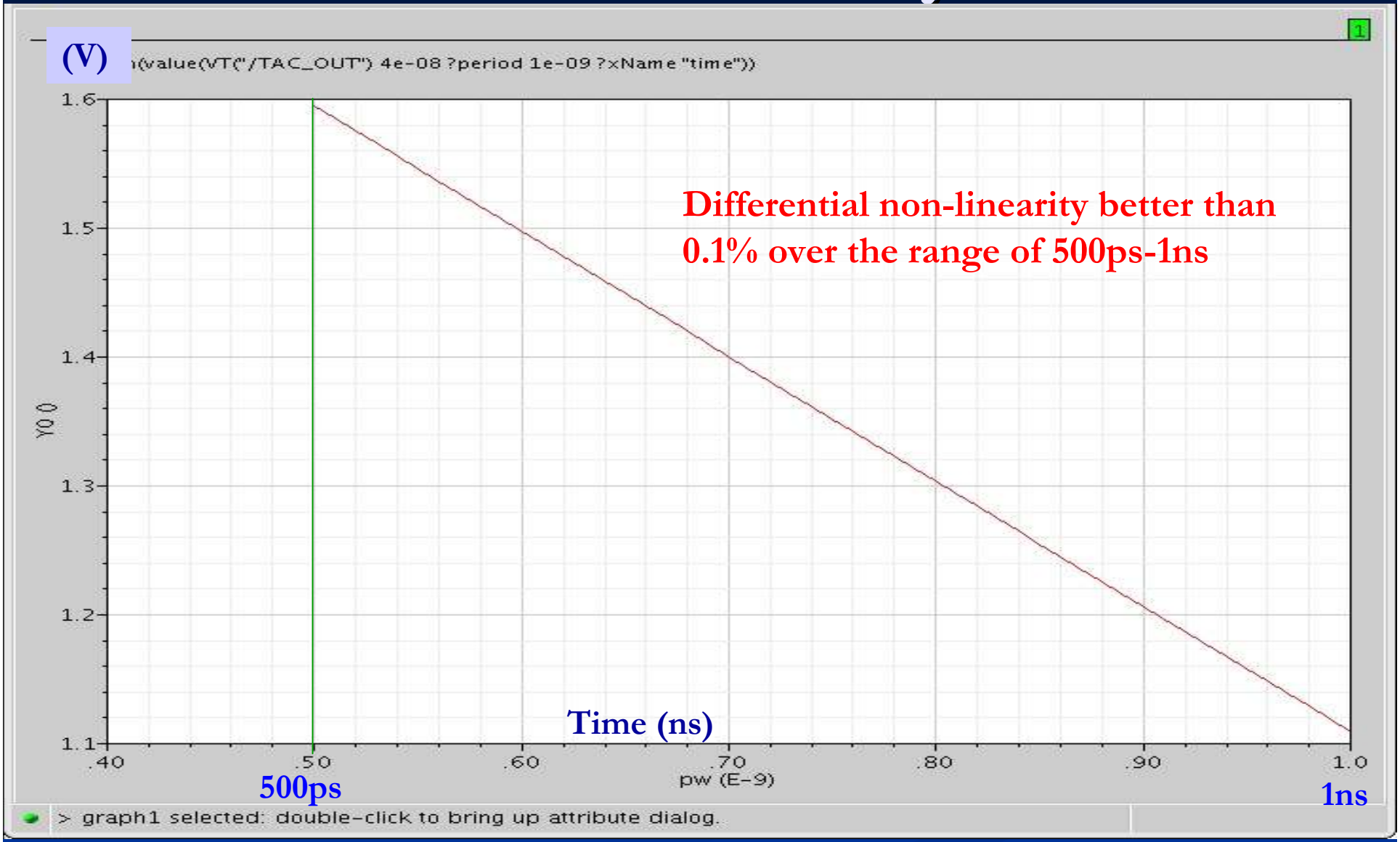
TAC Simulation

Input time intervals from 500ps to 510ps with 1ps step





TAC Linearity



Summary

Time Stretcher:

The main drawback is the limited dynamic range in ASIC design. The small signal slew rate (dv/dt) generates unacceptable jitters by the comparator. The estimated timing jitter out of the initial spec.

TAC:

- 1ps resolution is achievable (1mv/ps).
- Less techniques challenges on circuit design.
- Better linearity (One conversion instead of two).
- No fast signal transmission between FE to DAQ.
- Faster conversion (less system dead time).
- With multiple sampling, the TAC output noise is reduced by a factor of Sqrt(N).

ΔΣ ADC ----low rate, low bandwidth

S/H ADC with multiplexer

Sampling ADC ----high rate, high bandwidth

- No special requirement for FPGA.
- Lower cost.

- 4-ch ADCs added.
- 8 more signals (4 DATA_READY, 4 Reset) added.