

Electronics *Development* for *pSec Time-of-Flight Detectors*

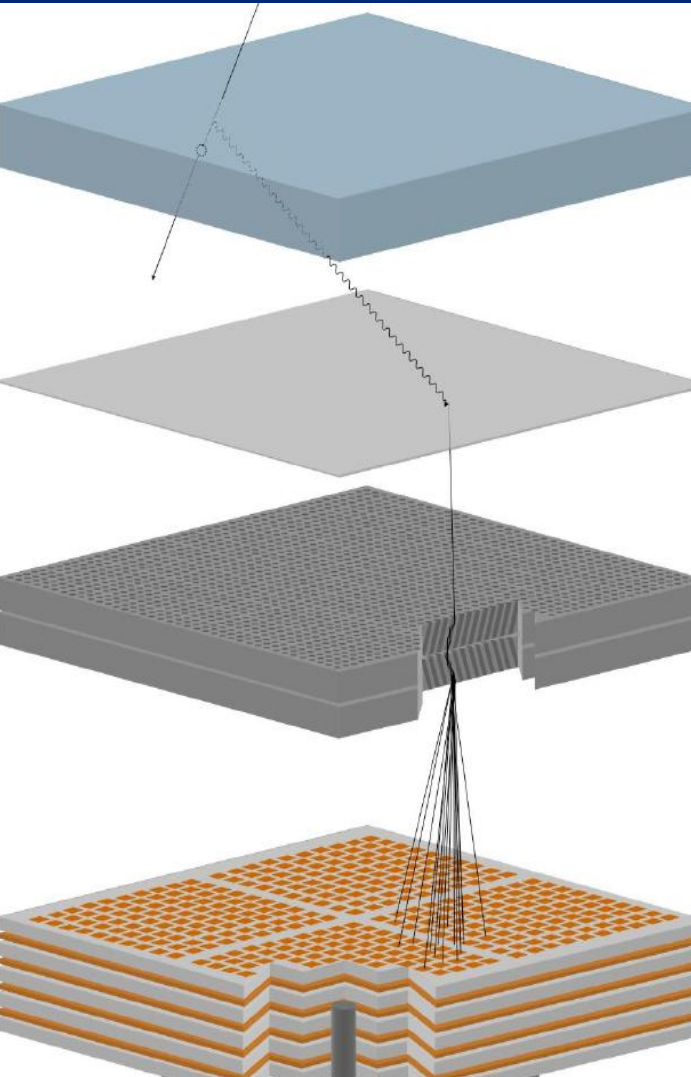
Fukun Tang

Enrico Fermi Institute
University of Chicago

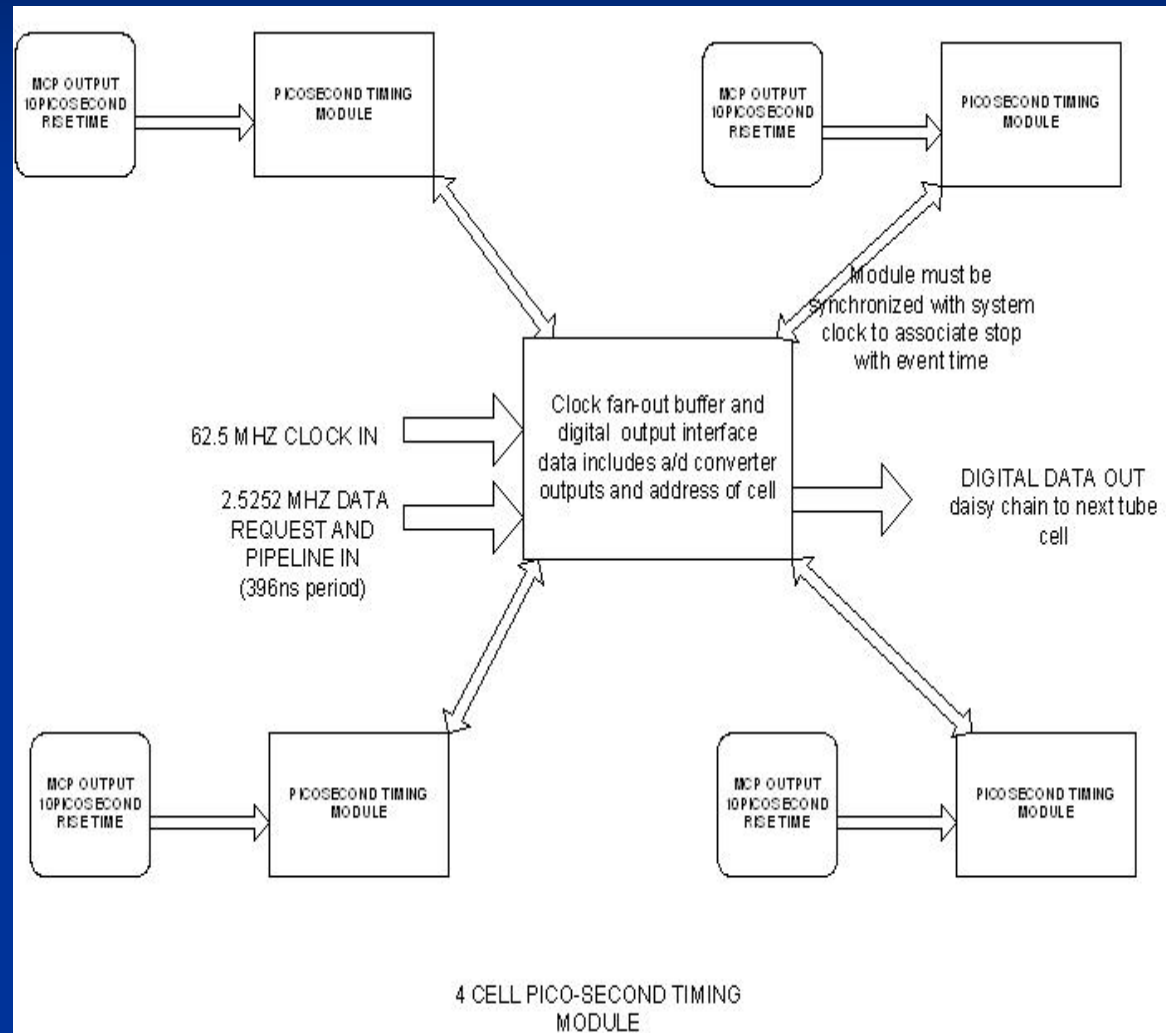
With Karen Byrum and Gary Drake (*ANL*)
Henry Frisch, Mary Heintz and Harold Sanders (*UC*)

Introduction: Readout Electronics System

Anode structure



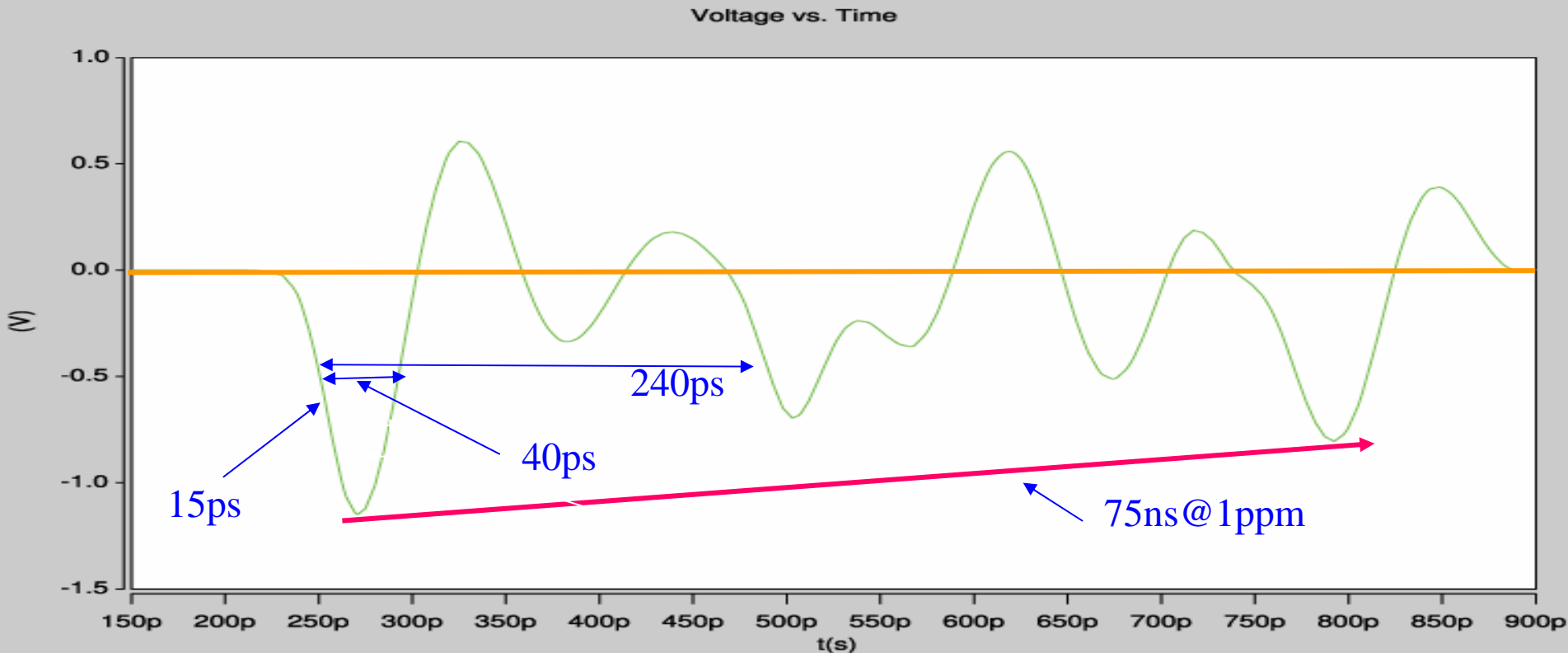
Harold's TOF system



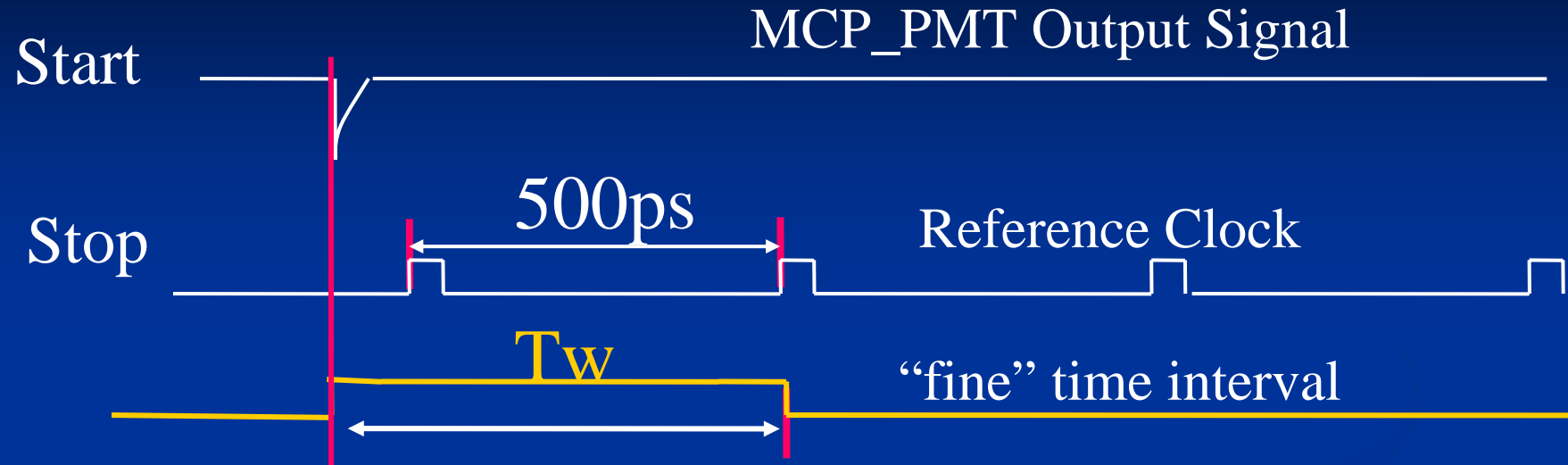
Characteristics of MCP-PMT Output Signal

MCP-PMT output signal from Tim' simulation

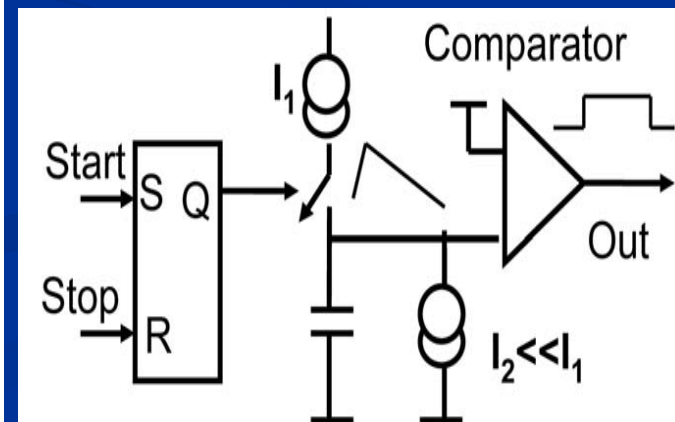
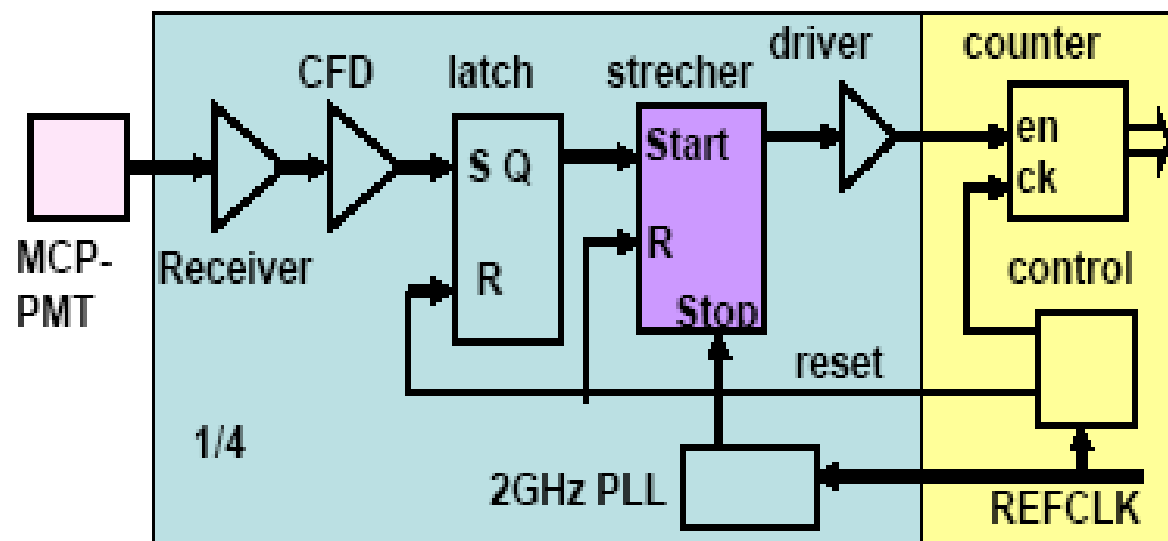
- 📖 Rise time 15ps (equivalents to a signal bandwidth of 23.3 GHz)
- 📖 Pulse width (FWHM): 40ps
- 📖 Reflection coefficient: -0.98 (Load=100 ohms)
- 📖 Reflection time delay (round trip): 240ps
- 📖 Recovery time: 75ns (Settled at 1ppm)



Proposed Time Stretcher TDC with 1ps Resolution



psFront-end



Electronics Requirements & Process Evaluations

<i>Input signal bandwidth:</i>	<i>~23.3GHz</i>
<i>Input signal width (FWHM):</i>	<i>~40ps</i>
<i>TDC resolution:</i>	<i>~1ps</i>

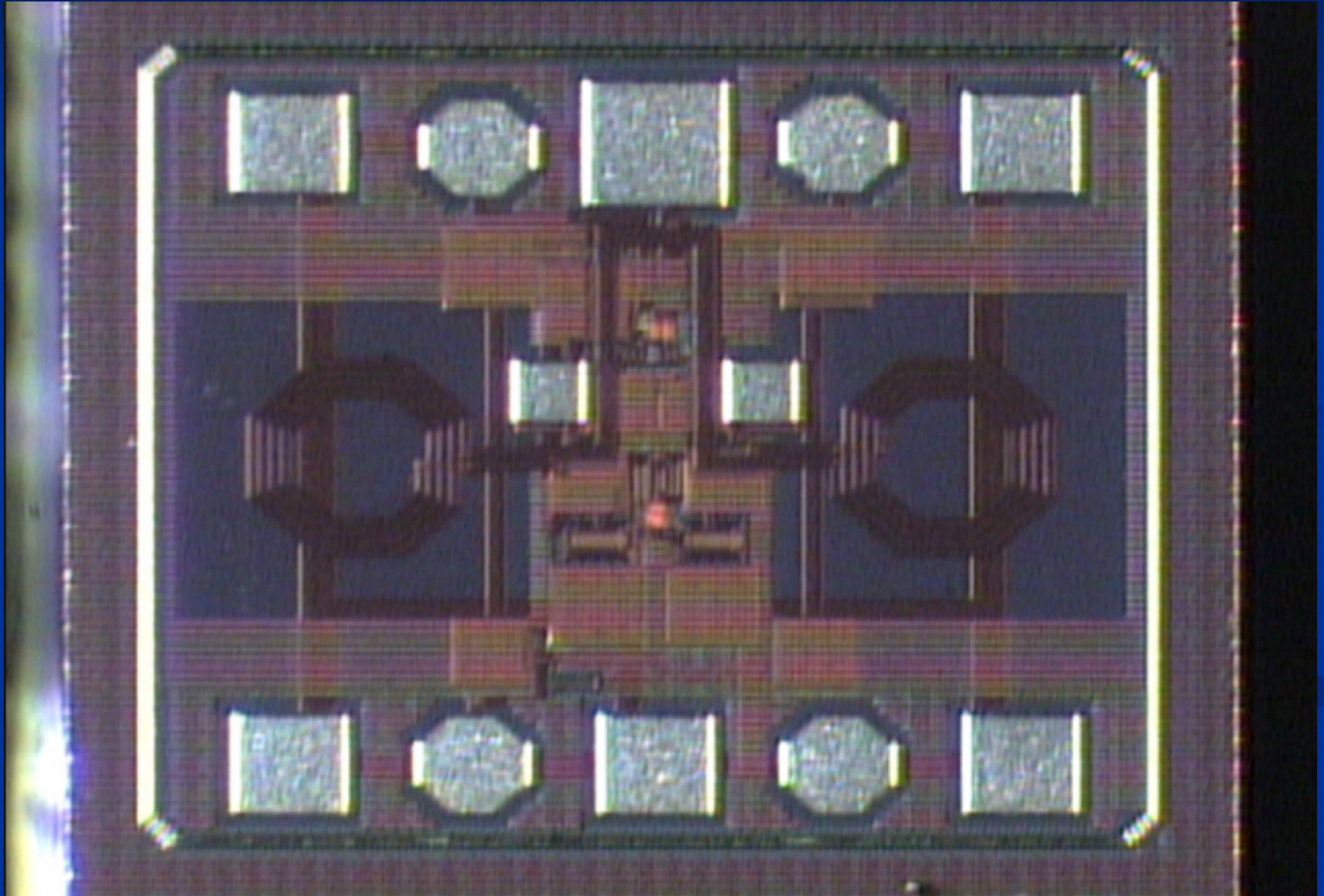
Minimum Requirements:

- ultra low noise, ultra high f_T transistors
> 5-10x of the input signal bandwidth ~ (110-220GHz)
- stable passive components
Inductors, MIM Capacitors, Resistors, Varactors ...

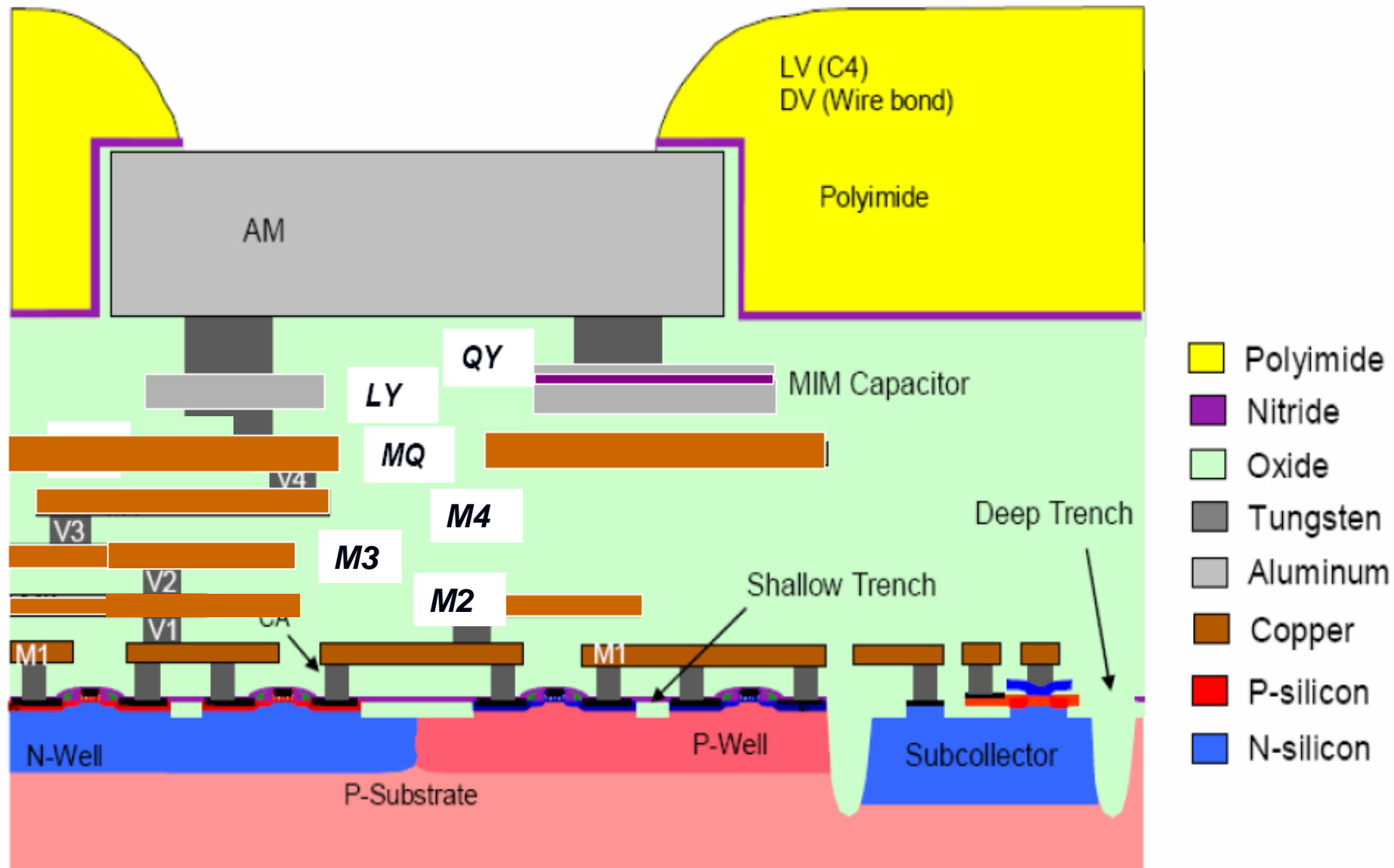
Available Processes:

- IHP SiGe BiCMOS 0.25 μ m technology:
(SG25H1, SG25H2) --- *Europactice*
- IBM SiGe BiCMOS 0.13 μ m Technology:
(8HP) --- *MOSIS*

UC designed 2 GHz VCO with 55 fsec Cycle-to-Cycle Timing Jitter Using IHP SG25H1 Process



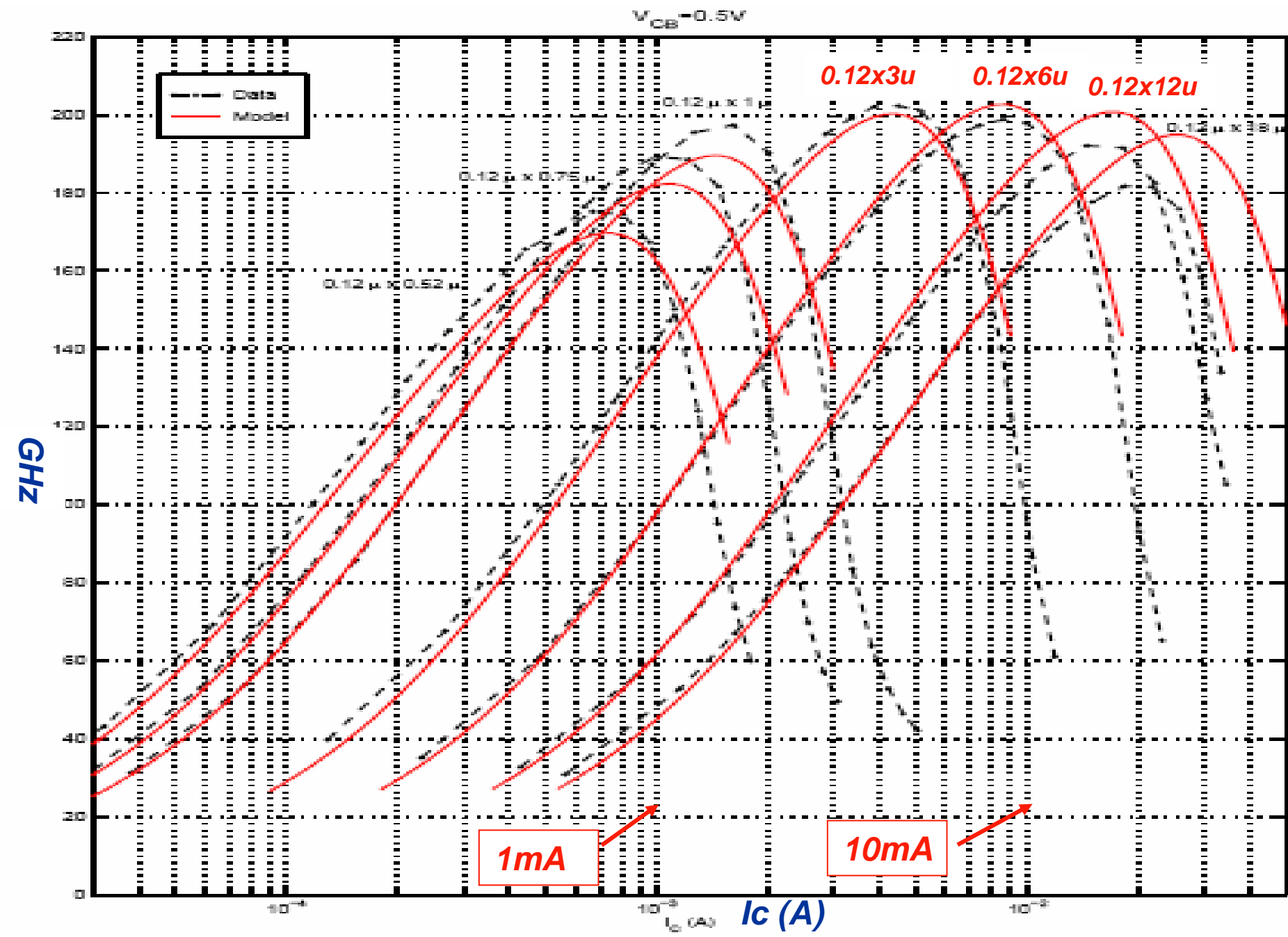
IBM SiGe BiCMOS8HP Process Cross-section



Brief Summary of IBM BiCMOS8HP Process

- **SiGe hetero-junction bipolar transistors**
 - *f_T (high performance): 200GHz, $BV_{ceo}=1.7V$, $BV_{cbo}=5.9V$*
 - *f_T (high breakdown): 57GHz, $BV_{ceo}=3.55V$, $BV_{cbo}=12V$*
- **High-Q inductors and metal-insulator-metal capacitors**
- **4 types of low-tolerance resistors with low and high sheet resistivity**
 - *$n+$ diffusion, tantalum nitride, $p+$ polysilicon and $p-$ polysilicon*
- **CMOS transistors ($V_{DD}=1.2V$ or 2.5/3.3V)**
 - *Twin-well CMOS*
 - *Hyperabrupt junction and MOS varactors*
- **Deep trench and shallow trench isolations**

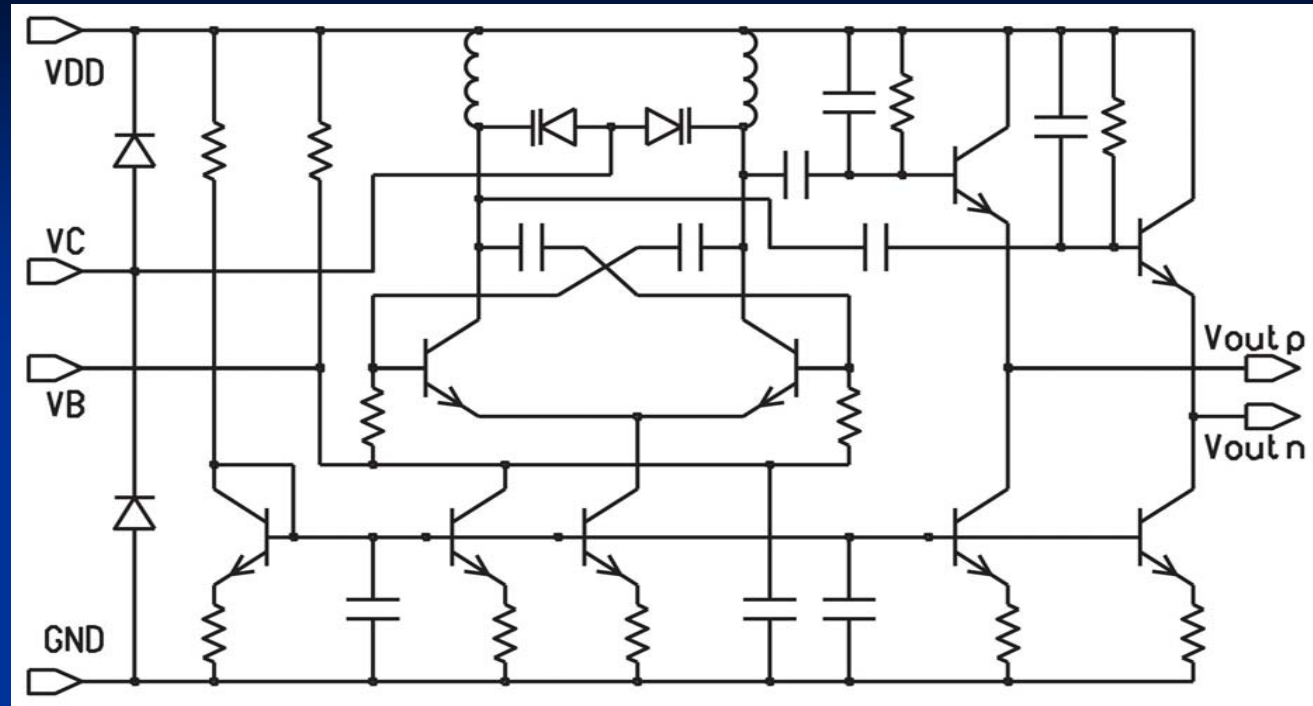
8HP NPN Ft Characteristics vs. Emitter size (25C)



2GHz VCO Design using IBM SiGe BiCMOS8HP Process

EDA Tools:
Cadence Virtuoso
Analog Environment

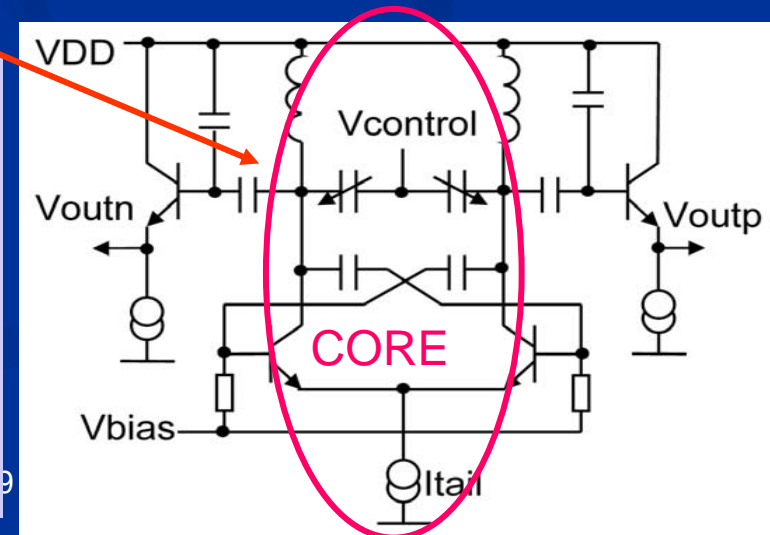
Verification Tools:
Diva/Assura



Simplified VCO Schematic

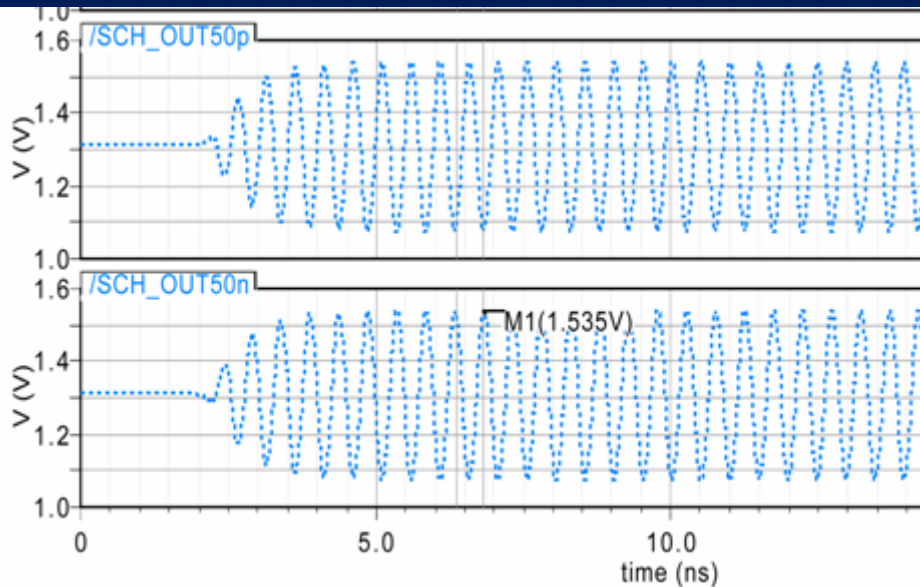
- Purely hetero-junction transistors
- Negative resistance
- On-chip high-Q LC tank
- High Frequency PN diode Varactors
- Capacitor voltage dividers
- 130Mhz tuning range
- Full differential 50-ohm line drivers

Core

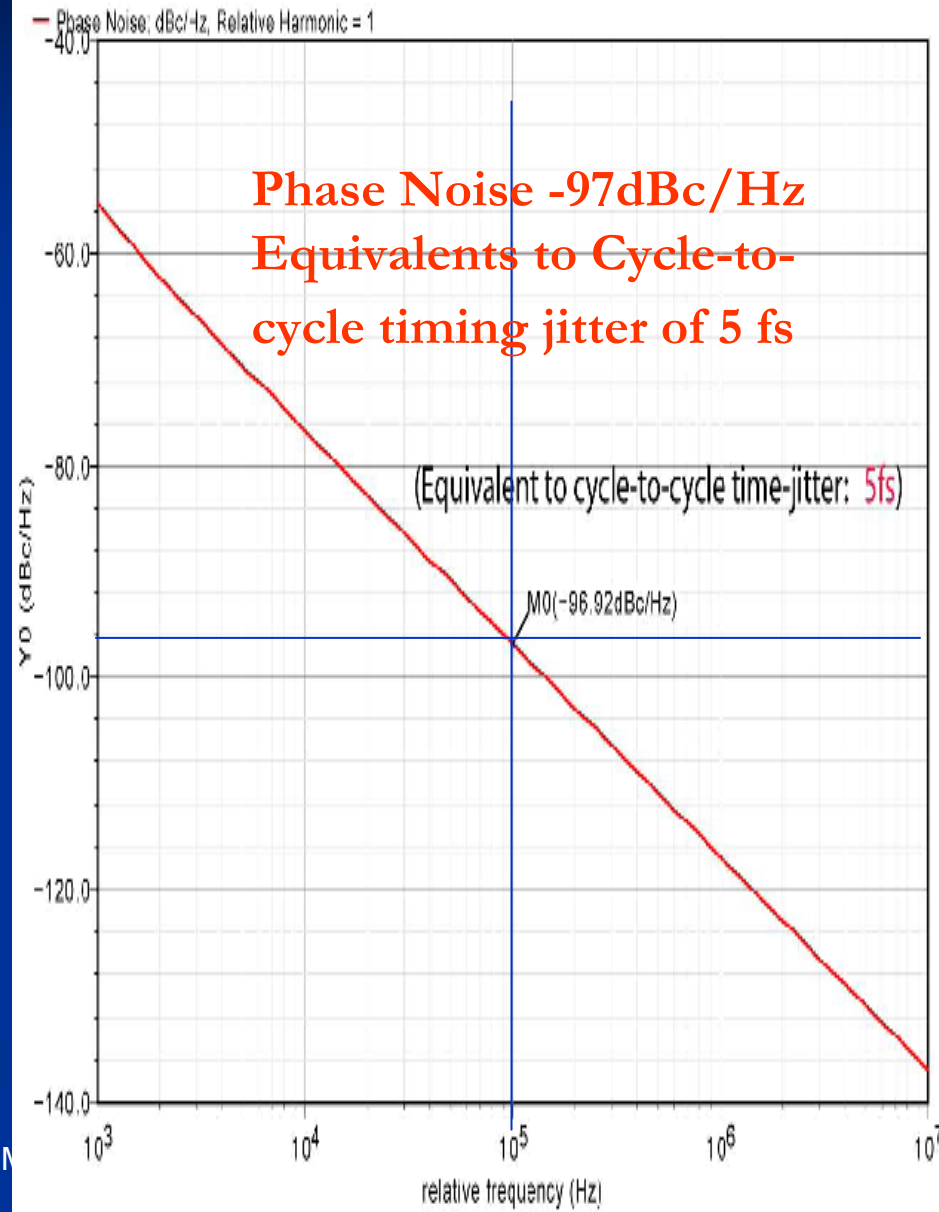


VCO Schematic (Pre-layout) Simulation Result

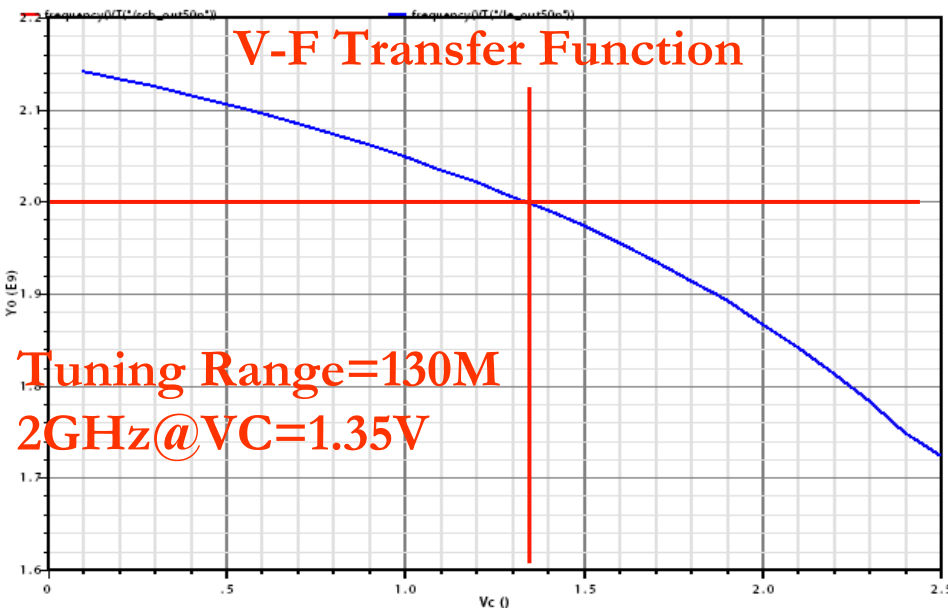
Transit Outputs



Phase Noise



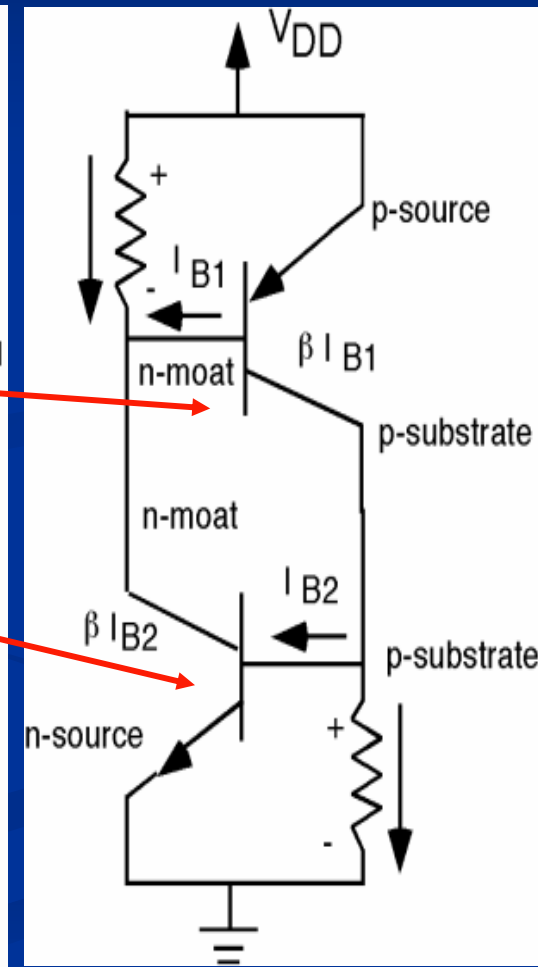
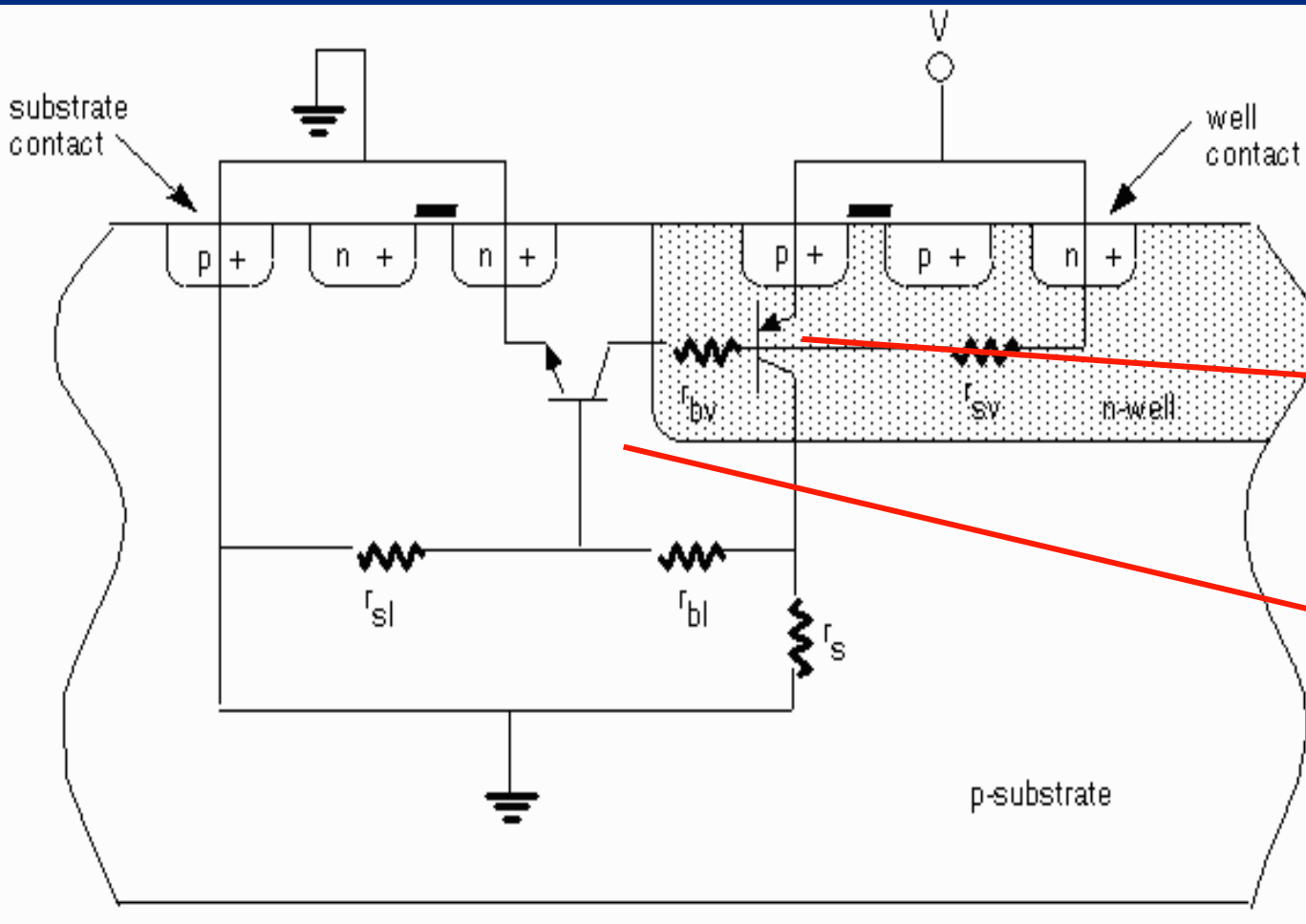
V-F Transfer Function



Analysis of CMOS Latchup

Famous CMOS latch-up which created by parasitic lateral pnp and npn transistors

Solution: apply substrate contacts and tie them to the lowest voltage terminals
apply shallow trenches to increase isolation



Substrate Noise Minimization

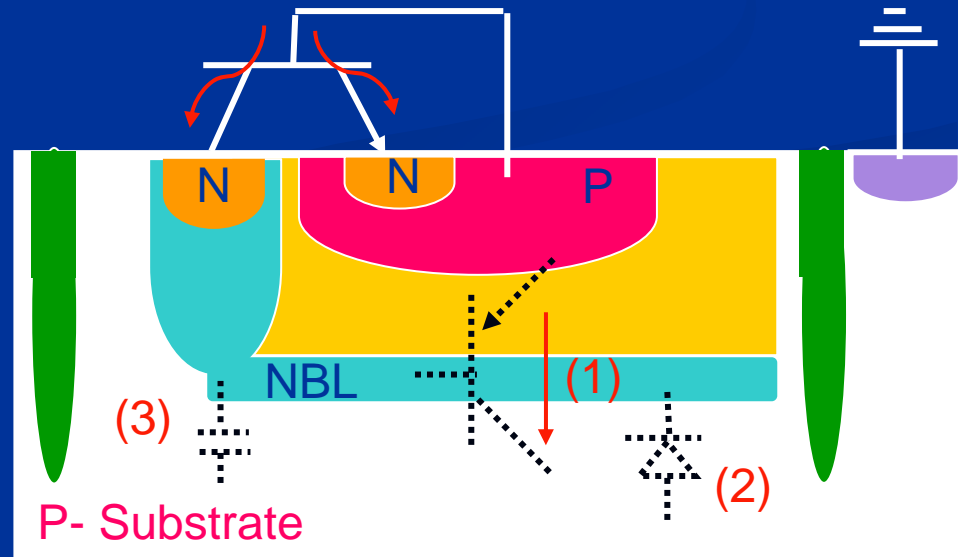
- (1) One of the major substrate noise is caused by current injection from bipolar transistors working in saturation mode.
- (2) Substrate PN diode occasionally forward biased by EMI interference or some other reasons.
- (3) Parasitic coupling capacitance

Solution:

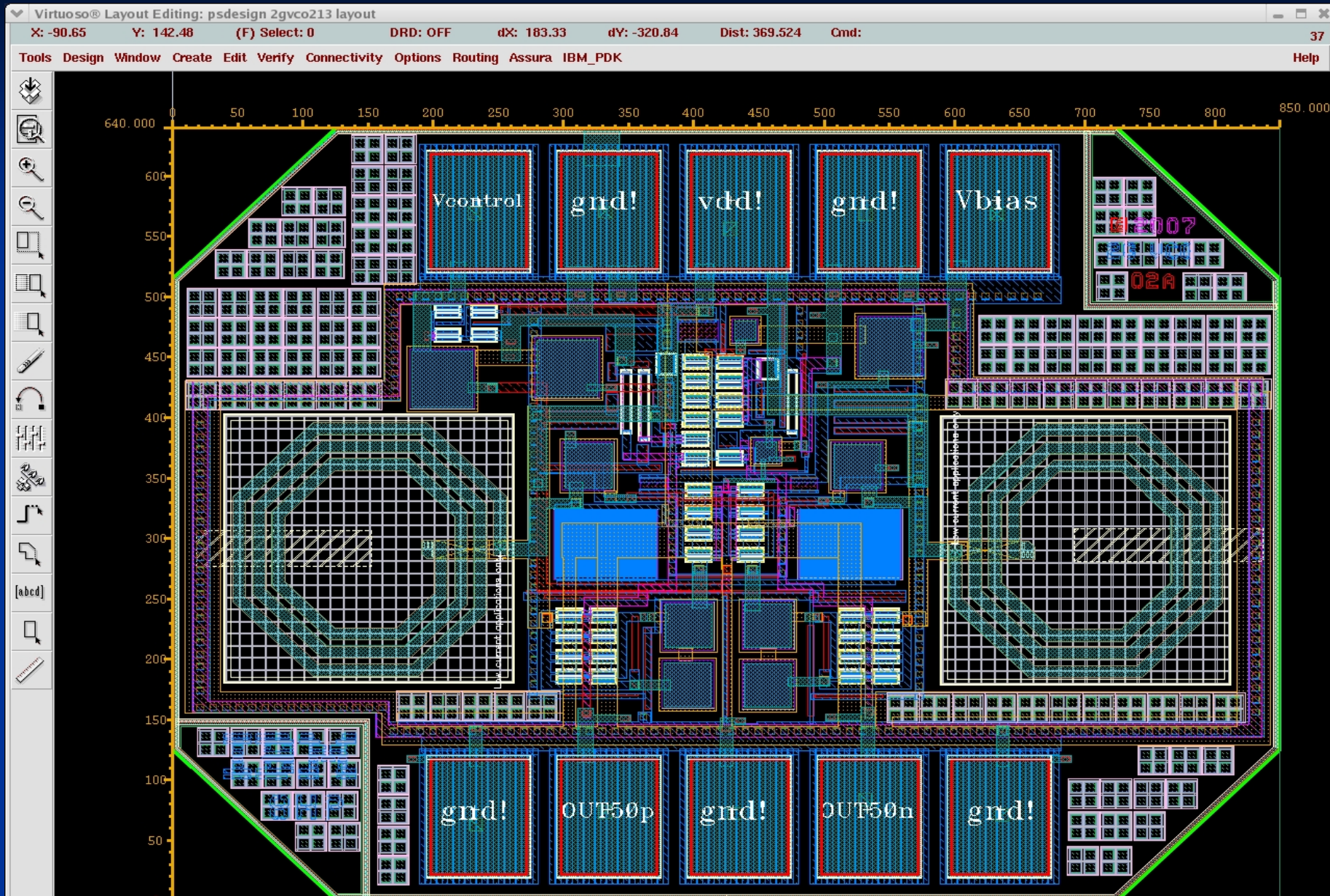
Prevent transistors from working in saturation mode unless you have to.

apply substrate contacts and tie them to the lowest voltage potential on the chip.

apply deep or shallow trench shielding rings to increase isolation



UC Designed 2GHz VCO Chip with 5 fsec Cycle-to-Cycle Time Jitter Using IBM 0.13 μ m SiGe BiCMOS8HP Process (Feb. 2007)

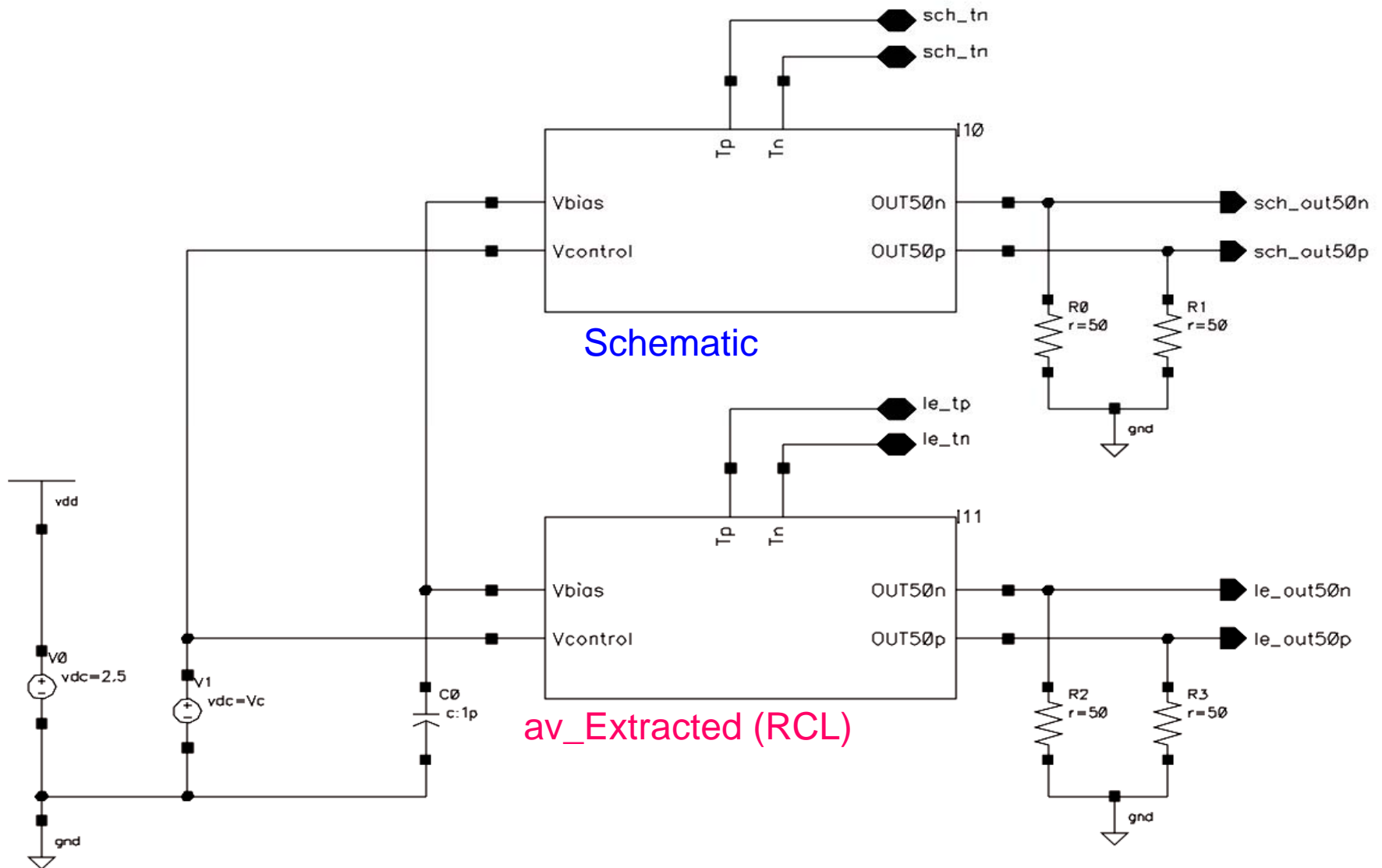


Layout and Parasitic Extraction

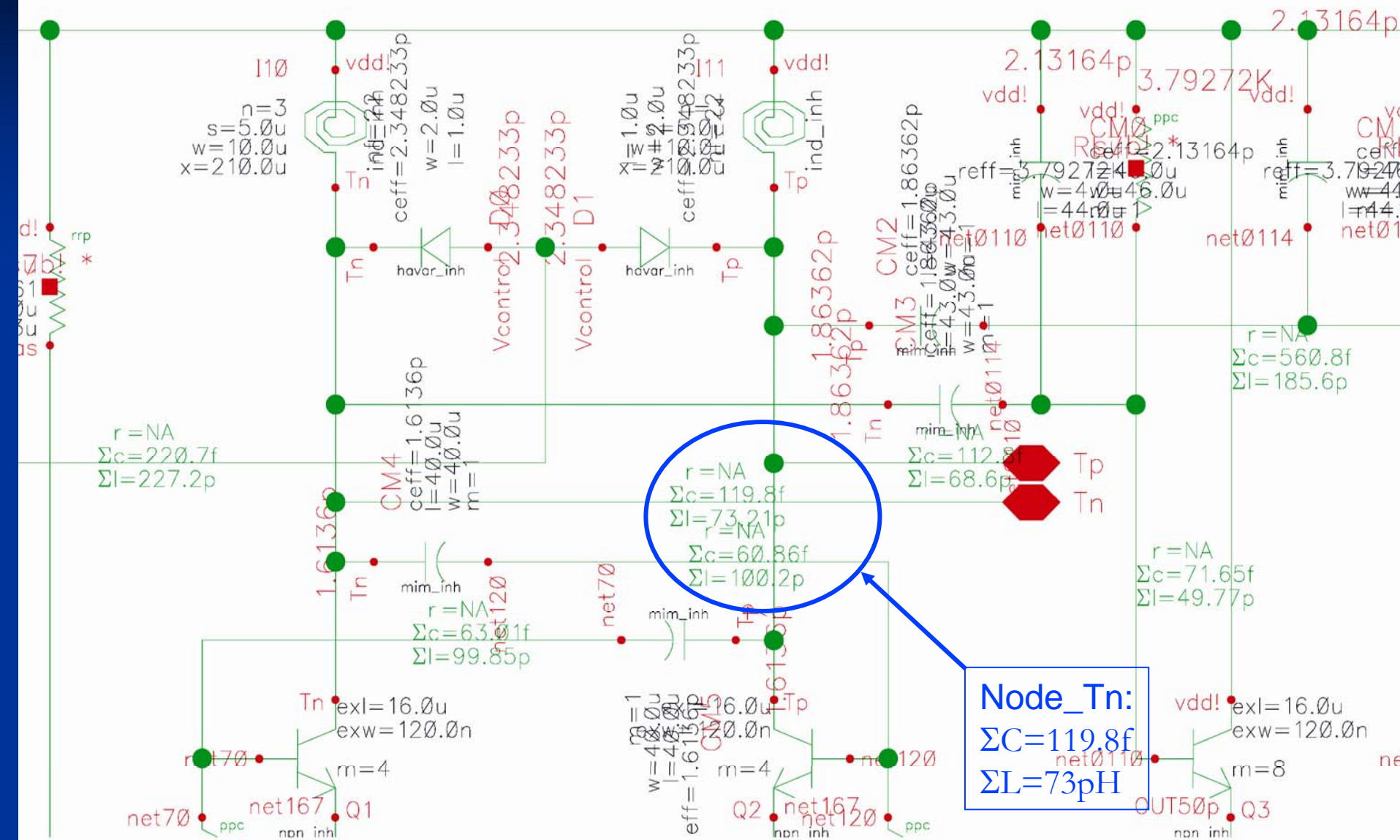
- Diva/Assura DRC Check
- Diva/Assura LVS Check
- Floating Gate, NWell & Antenna Check
- Global Pattern Density Check
- Local Pattern Density Check
- GR594 (Dendrite Rules) Check
- Assura RCL extraction
- GDSII Stream Out (CDS → GDSII mapping)
- GDSII/Layout Comparison Check

Backup your full data after you passed all checks!!!

Schematic & Post Layout Comparison: *Hierarchy Setup*



RLC_Extracted Schematic Back Annotation View



Post Simulation: *Configuration Setup*

The screenshot shows the Cadence hierarchy editor window titled "Cadence® hierarchy editor: (psdesign 2gvco208_top_tb config)". The window has a menu bar (File, Edit, View, Plug-Ins, Help) and a toolbar. The main area is divided into several sections:

- Top Cell:** Library: psdesign, Cell: 2gvco208_top, View: schematic, Open button.
- Global Bindings:** Library List: myLib, View List: spectre cmos_sch cmos.sch schematic veriloga ahdl, Stop List: spectre.
- Cell Bindings:** A table with columns: Library, Cell, View Found, View to Use, and Inherited View List.
- Messages:** A log of actions performed during the configuration setup.

Cell Bindings Table:

Library	Cell	View Found	View to Use	Inherited View List
bicmos8hp	risres_inh	spectre		spectre cmos_sch cmos.sch...
bicmos8hp	opppres	spectre		spectre cmos_sch cmos.sch...
bicmos8hp	opppres_inh	spectre		spectre cmos_sch cmos.sch...
bicmos8hp	oprrpres	spectre		spectre cmos_sch cmos.sch...
bicmos8hp	oprrpres_inh	spectre		spectre cmos_sch cmos.sch...
bicmos8hp	subc	spectre		spectre cmos_sch cmos.sch...
bicmos8hp	subc_inh	spectre		spectre cmos_sch cmos.sch...
psdesign	2gvco208	av_extracted	av_extracted	spectre cmos_sch cmos.sch...
psdesign	2gvco208	schematic	schematic	spectre cmos_sch cmos.sch...
psdesign	2gvco208_top	schematic		spectre cmos_sch cmos.sch...

Messages:

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RESTRICTED RIGHTS NOTICE (SHORT FORM)
Use/reproduction/disclosure is subject to restriction set forth at FAR 1252.227-19 or its equivalent.
Attempting to lock configuration (psdesign 2gvco208_top_tb config).
Opened the configuration (psdesign 2gvco208_top_tb config).
Bound instance "I7" in cellview (psdesign 2gvco208_top schematic) to view "schematic".
Saved the current configuration.
Saved the current configuration.
Bound instance "I10" in cellview (psdesign 2gvco208_top schematic) to view "schematic".
Bound instance "I11" in cellview (psdesign 2gvco208_top schematic) to view "av_extracted".
Saved the current configuration.

Annotations:

- A red circle highlights the "av_extracted" and "schematic" entries in the "View to Use" column of the Cell Bindings table.
- A red arrow points from the text "Parasitic Parameters Back Annotation" to the "av_extracted" entry.
- A red arrow points from the text "Parasitic Parameters Back Annotation" to the "Bound instance 'I11' in cellview (psdesign 2gvco208_top schematic) to view 'av_extracted'." message.

Status Bar: Ready... Filters OFF NameSpace: CDBA

Post Simulation Parasitic Parameter List

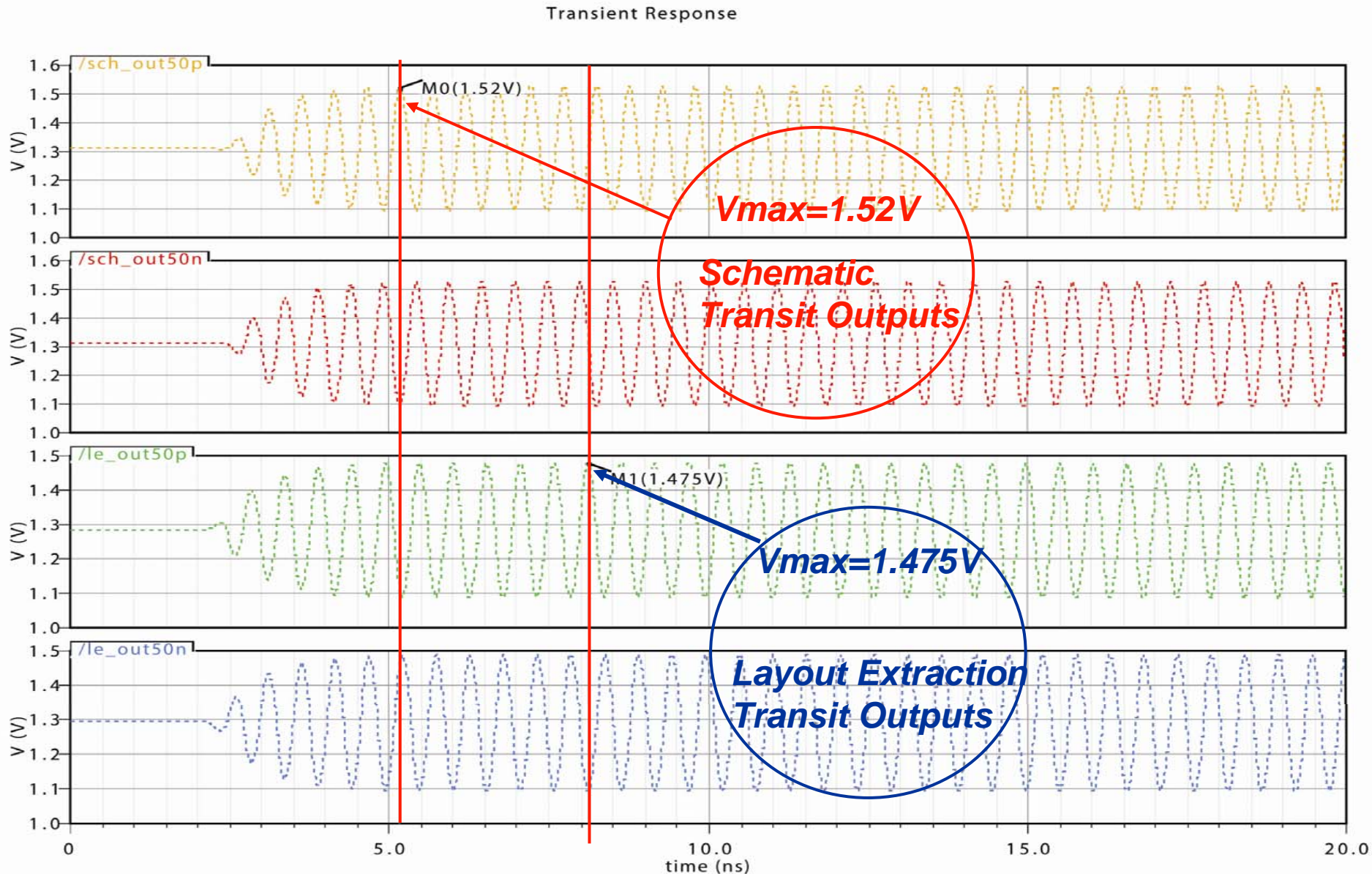
The figure displays three overlapping screenshots of a software interface, likely a circuit simulator or design tool, showing hierarchical tree views of circuit components and their associated view lists.

Screenshot 1 (Top Left): Shows a "Tree View" window. The left pane lists instances such as c3850 (analogLib pcapacitor spectre), c3851 (analo...), c3852 (analo...), c3853 (analo...), c3854 (analo...), c3855 (analo...), c3856 (analo...), c3857 (analo...), c3858 (analo...), c3859 (analo...), c3860 (analo...), c3861 (analo...), c3862 (analo...), c3863 (analo...), l1_1 (analogL...), l1_2 (analogL...), and l1_3 (analogL...). The right pane shows the "Inherited View List" for selected instances, listing spectre, cmos_sch, and cmos.sch ...

Screenshot 2 (Middle Right): Shows a "Tree View" window. The left pane lists instances such as l1_236 (analogLib pinductor spectre), l1_237 (analogLib pinductor spectre), l1_238 (analogLib pinductor spectre), l1_239 (analogLib pinductor spectre), l1_240 (analogLib pinductor spectre), l1_241 (analogLib pinductor spectre), l1_242 (analogLib pinductor spectre), l1_243 (analogLib pinductor spectre), l1_244 (analogLib pinductor spectre), l1_245 (analogLib pinductor spectre), l1_246 (analogLib pinductor spectre), l1_247 (analogLib pinductor spectre), l1_248 (analogLib pinductor spectre), l1_249 (analogLib pinductor spectre), l1_250 (analogLib pinductor spectre), ra1 (analogLib resistor spectre), ra11 (analogLib resistor spectre), ra12 (analogLib resistor spectre), and ra13 (analogLib resistor spectre). The right pane shows the "Inherited View List" for selected instances, listing spectre, cmos_sch, and cmos.sch ...

Screenshot 3 (Bottom Right): Shows a "Tree View" window. The left pane lists instances such as rg_1_307 (analogLib presistor spectre), rg_1_308 (analogLib presistor spectre), rg_1_309 (analogLib presistor spectre), rg_1_310 (analogLib presistor spectre), rg_1_311 (analogLib presistor spectre), rg_1_312 (analogLib presistor spectre), rg_1_315 (analogLib presistor spectre), rg_1_319 (analogLib presistor spectre), rg_1_322 (analogLib presistor spectre), rg_1_326 (analogLib presistor spectre), rg_1_358 (analogLib presistor spectre), rg_1_359 (analogLib presistor spectre), rg_1_424 (analogLib presistor spectre), rg_1_425 (analogLib presistor spectre), and rg_1_434 (analogLib presistor spectre). The right pane shows the "Inherited View List" for selected instances, listing spectre, cmos_sch, and cmos.sch ...

Schematic/Post Layout Simulation Comparison: Transit Outputs (first layout)



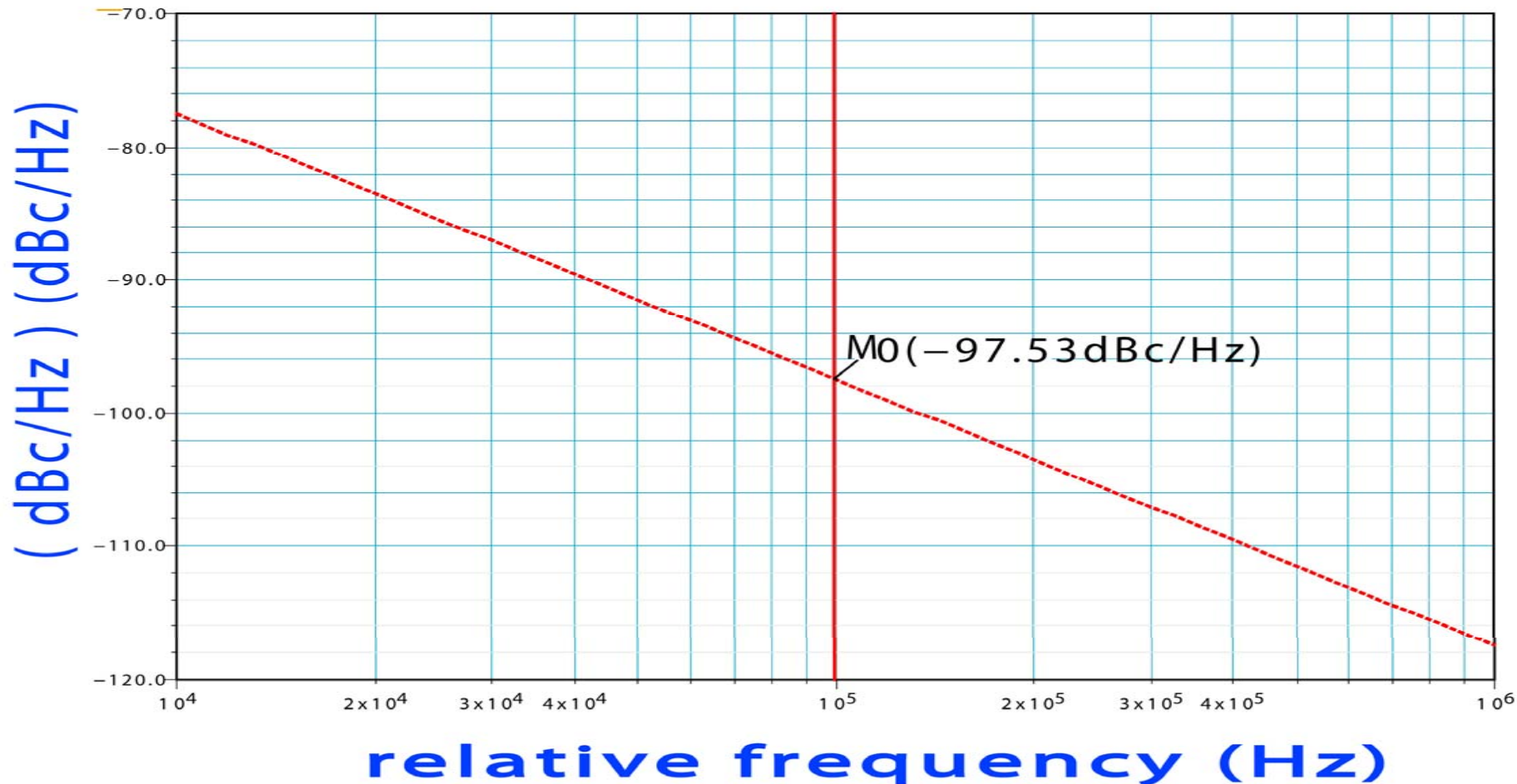
VCO Post Layout Simulation Result (First Layout)

Output Phase Noise Spectra Plot

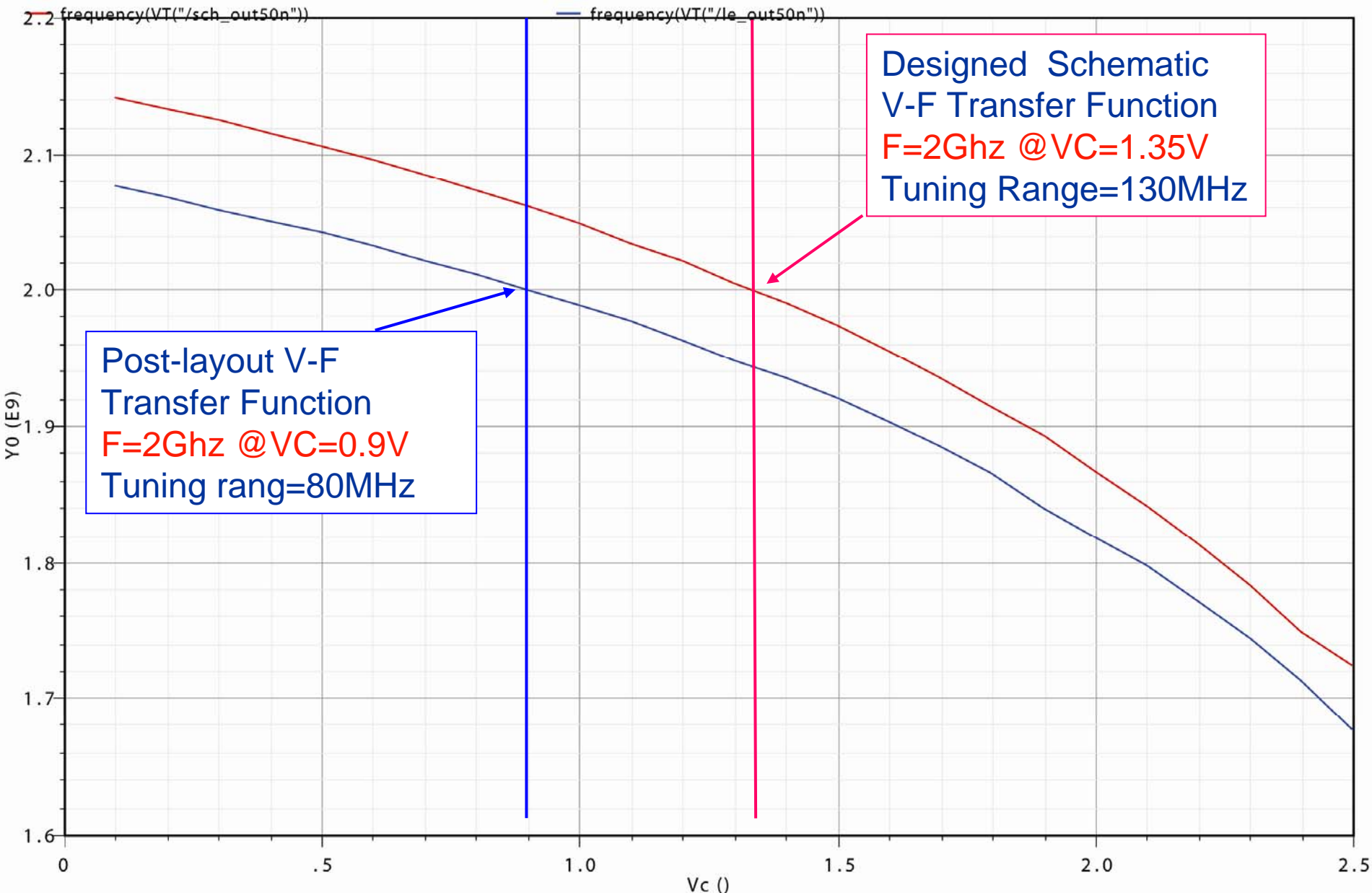
psdesign 2gvco208 av_extracted : Feb 14 16:41:16 2007

Phase Noise; dBc/Hz, Relative Harmonic = 1

Periodic Noise Response

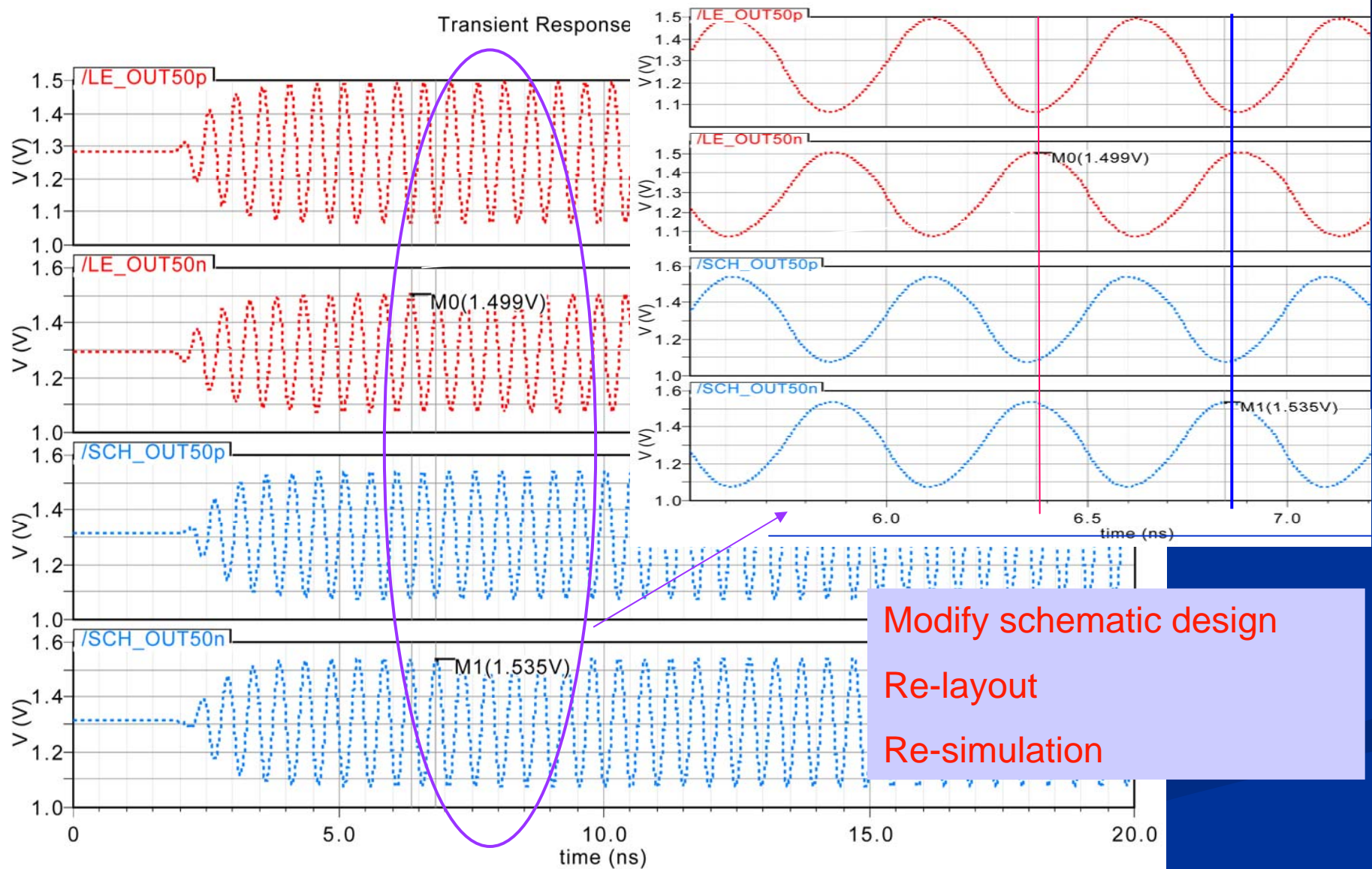


Schematic/Post Layout Simulation Comparison: V-F Transfer Function Plot (first layout)



VCO Post Layout Transit Simulation Result (Final)

Transit Output Waveforms



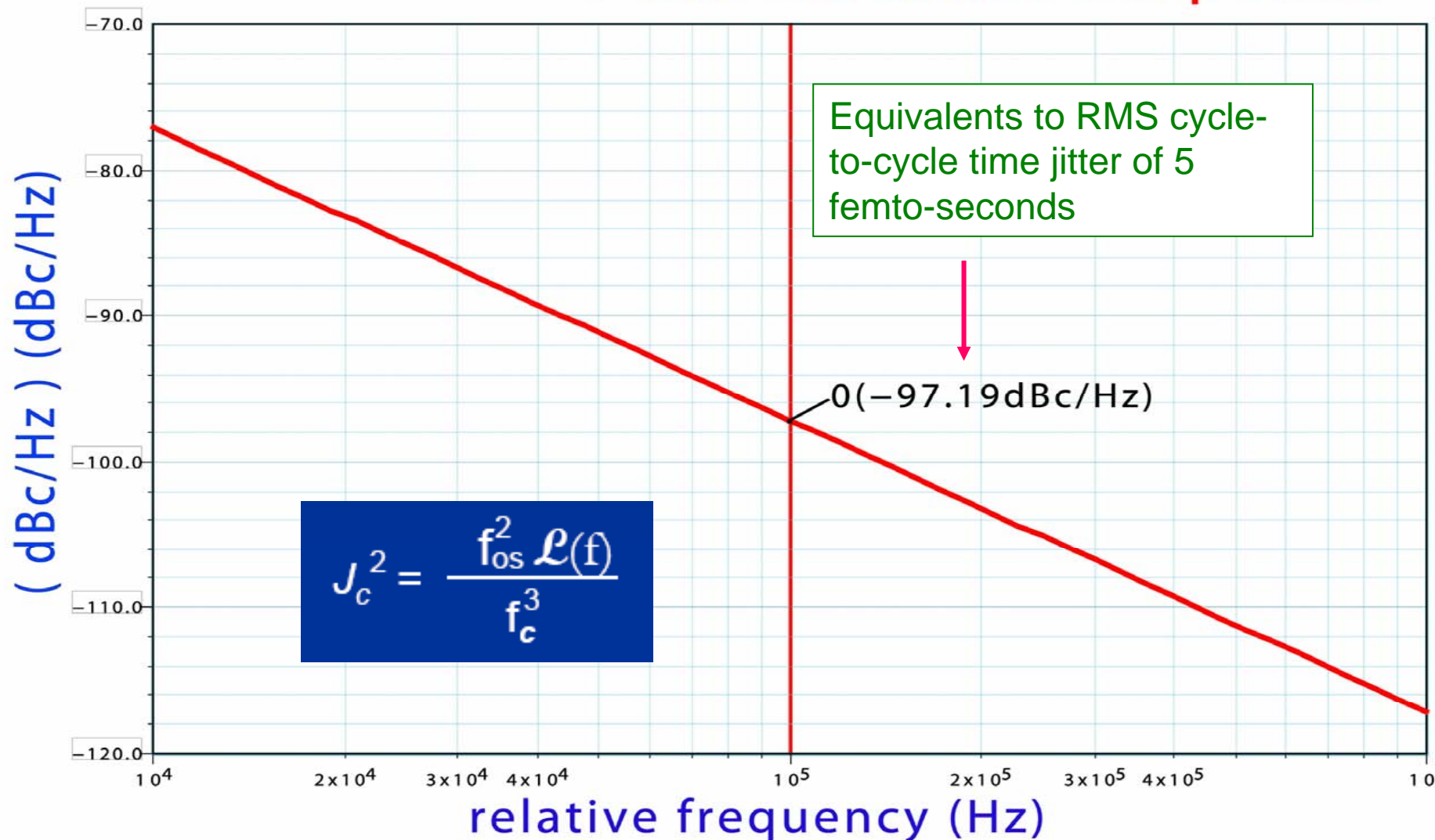
VCO Post Layout Simulation Result (Final)



Output Phase Noise Spectra Plot

Phase Noise; dBc/Hz, Relative Harmonic = 1

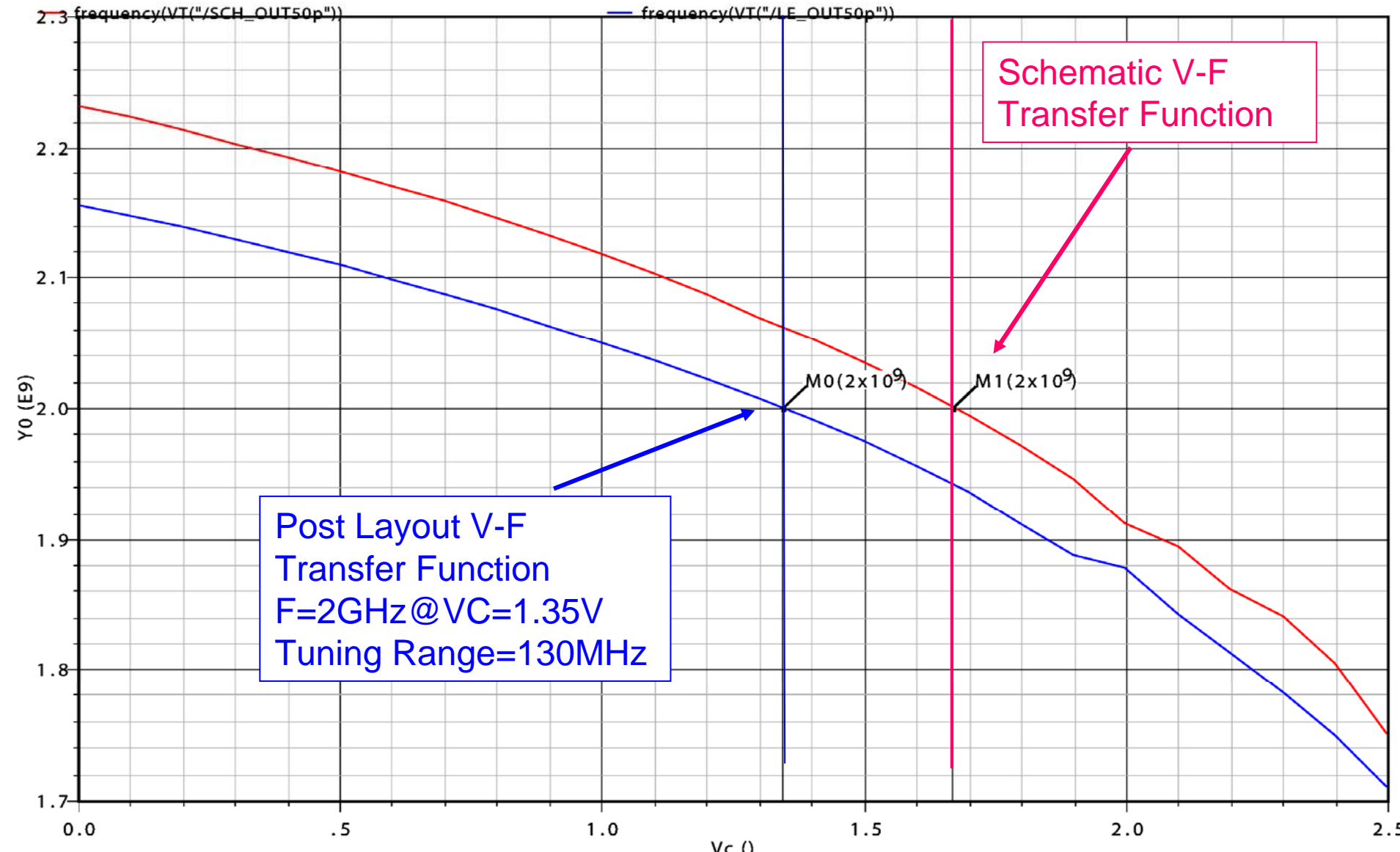
Periodic Noise Response



VCO Simulation Result (Final)



V-F Transfer Function Plot



Conclusion

- (1) IBM 0.13 μ m SiGe BiCMOS8HP has been evaluated; it is a user-friendly design kit.
- (2) Circuit performance meets our requirements (very) well.
- (3) MOSIS has resumed 8HP Multi-Project Wafer runs – schedule has been changing(!). We are in the process of understanding how to proceed toward a full chip design starting with our first little VCO chip.
- (4) Challenging Issues for the entire readout electronics.

Thanks!