Proposed Changes to the ACDC Board

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1 Introduction

The purpose of the ACquisition and Digitization with PseC4 (ACDC) board is to translate analog data collected by the PSEC4 ASICs into digital signals to be received by a Control Card. The existing board was designed by Eric Oberla in 2014 to work with the PSEC4 chips for the Large Area Picosecond PhotoDetector (LAPPD) project run by Professor Henry Frisch at the University of Chicago.

Now that the PSEC4 has been updated to make the PSEC4a, it is worthwhile to have a compatible board that could replace the ACDC and utilize the PSEC4a ASICs. The scope of this proposed redesign is to update the current ACDC board to use the new chips, dissipate less power, optimize the form of the board for use with an LAPPD tile, and simplify the board design by removing unnecessary components, while maintaining plug compatibility with the LAPPD tiles and ANNIE Control Card (ACC). Additionally, I propose that this new board be named the LAPPD Electronics Interface Board, or the LEIBowitz board.[1]

[1] In honor of the blessed Saint Leibowitz from Walter M. Miller's *A Canticle for Leibowitz*.

2 Hardware Changes

2.1 Power Regulation

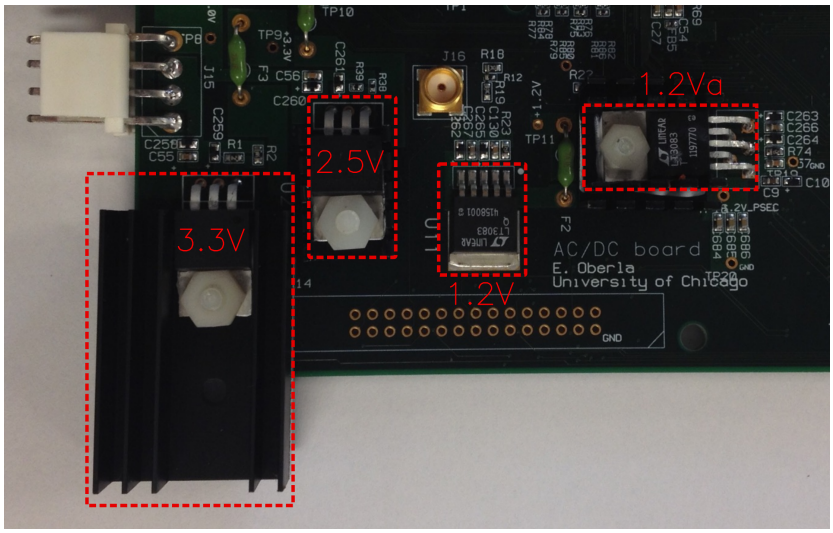

Figure 1: Power regulation system on the ACDC board.

The ACDC board currently uses four individual linear regulators to create supplies of 1.2V[2], 2.5V[3], and 3.5V[4], and a separate low-noise 1.2V (called "1.2Va") solely for the PSEC4 ASICs, with additional capacitor filtering. Linear regulators were used for the original board design because of their simplicity.

Using switching regulators for the board redesign was debated due to the concern that high frequency switching would contribute too much noise to the analog signals collected by the PSECs. However, I tested two ACDC boards with a switching regulator, and the results suggest that the noise contributed by a switching regulator is no greater than what is already present with the linear regulators. See Section 4.5 for details.

Therefore, I recommend a single three-output switching regulator, such as the Allegro A4490EESTR-T[5], be used with adequate filtering in lieu of the four linear regulators currently used to supply the required voltages for the new Leibowitz board.

The displayed values for the supporting circuitry in Figure 2 would be used to create three relatively low-noise voltage supplies. The A4490 and supporting electronics will occupy less on-board real estate than four linear regulators and power sinks, and dissipate less power.

2.2 Removing Unnecessary Components

Multiple components will be removed to simplify the board and eliminate redundancy.

2.2.1 PLL Chip

The PLL chip is being used to create a clean clock signal for the PSEC4s. To simplify the board, the job of the PLL chip could be completed by an unused PLL on the Cyclone IV FPGA (only three of which are being used, out of eight total). The pin assignment for the external clock input to the Cyclone chip is tricky, but could be done.[6] The clock signal from the FPGA's PLL will then be buffered by an external clock buffer chip with at least four outputs, and distributed to the four PSEC4a chips.

[2]The 1.2V and 1.2Va are each supplied by a Linear Technology LT3083 Adjustable Low Dropout Regulator.
[3]Supplied by a Texas Instruments LM317 Adjustable Regulator.
[4]Supplied by a Texas Instruments LM1084 Low Dropout Positive Regulator.
[5]www.digikey.com/product-detail/en/allegro-microsystems-llc/A4490EESTR-T/620-1245-1-ND/1831590
[6]The best strategy is to use automatic pin assignment before the FPGA programming gets too complex.

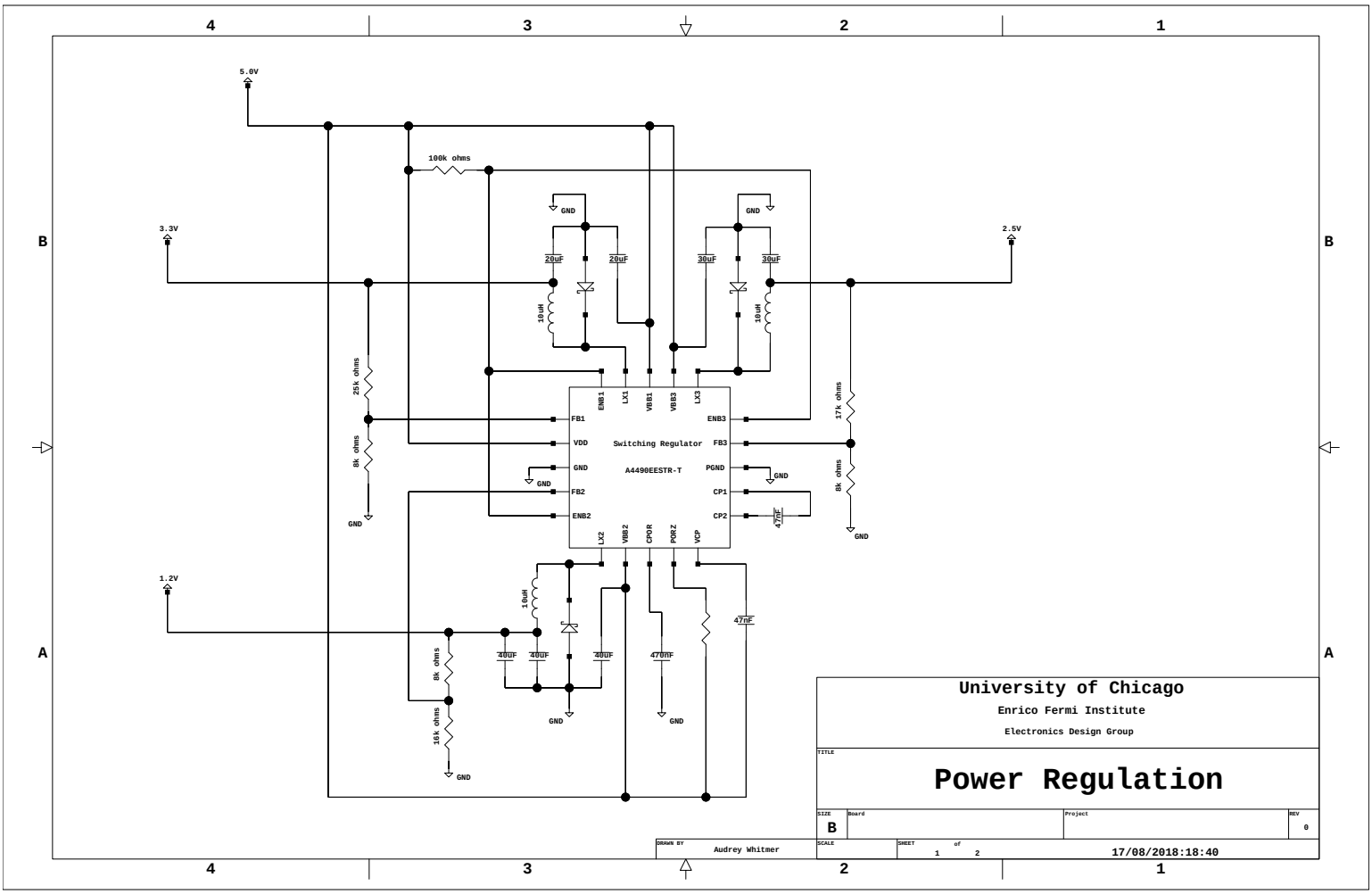

Figure 2: Supporting circuitry and values for the A4490 switching regulator.

A good choice is the Pericom PI6C10810 1:10 Clock Buffer.[7] If there are more than four outputs from the external chip, an additional clock signal may be sent to a test point on the board for diagnostic purposes. Each wire between the clock buffer and the PSEC4a chips should be made the same length to ensure minimal phase difference in clock signals. This way, specific offsets would not need to be determined and removed with programing.

2.2.2 DACs

The new PSEC4a chips have built in DACs to choose the trigger thresholds and various biases, but the pedestals will still need to be set externally. Therefore, all but one of the Linear Technology LTC2600 Octal DAC[8] will be removed from the board.

2.2.3 USB Port

The USB ports were added to the ACDC card to provide a different means of connection to the board, and to possibly allow the card to be used to test the PSEC4s. However, this feature has seldom, if ever, been used, so the USB port and supporting electronics will be removed from future board designs. An Evaluation Board can be used to test individual PSECs, making a possible testing feature redundant.

[7] www.diodes.com/assets/Datasheets/PI6C10810.pdf
[8] www.analog.com/media/en/technical-documentation/data-sheets/2600fe.pdf

3 Form Factor

Future designs of the board should be optimized to create an elegant unit of the detector tile and supporting electronics to minimize dead space and allow for true tiling.

To my knowledge, the form of the current ACDC board was not optimized for a particular layout. The setup of an LAPPD detector includes the detector tile, ACDC (or equivalent) electronics board, and a control card. The ACDC board measures 4 and 7/8 by 7 and 3/8 inches, while one LAPPD tile is 8.6 by 8.6 inches.

Each LAPPD tile will work in conjunction with either one or two supporting electronics boards. Connecting two boards to either side of the detector tile gives the option of double readout. This is not necessary, but is an option worth including in a board redesign.

To optimize the size of the electronics board for use with an LAPPD tile, the dimensions of the board could be changed to roughly 4 by 8 inches. This way, two boards could comfortably fit underneath one tile to create a compact unit capable of double sided readout.[9]

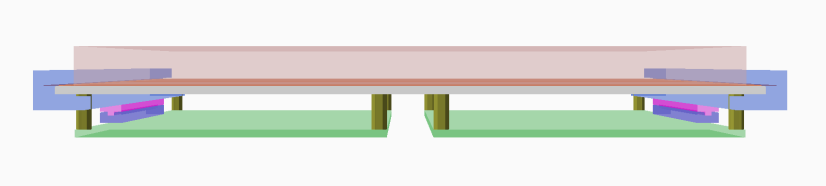

Figure 3: Resized electronics boards underneath the LAPPD tile, viewed from the side. The green plates represent the redesigned electronics boards, suspended underneath a tile.

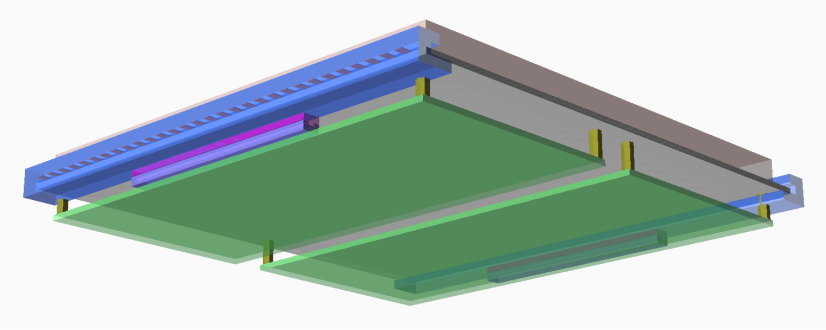

Figure 4: Resized boards underneath an LAPPD tile, viewed from below.

Moreover, wasted space could be further reduced if the Leibowitz board was able to plug directly into the bottom of the detector tile. This could be accomplished with a compact adapter that routed the ends of the capacitively coupled input leads to a 30-pin connector on the bottom of the tile. Leads ending on the bottom of the tile are not necessary, but could be beneficial, and should be considered in future designs of the tile base.

[9] I made the following models in OpenSCAD, a free CAD program.

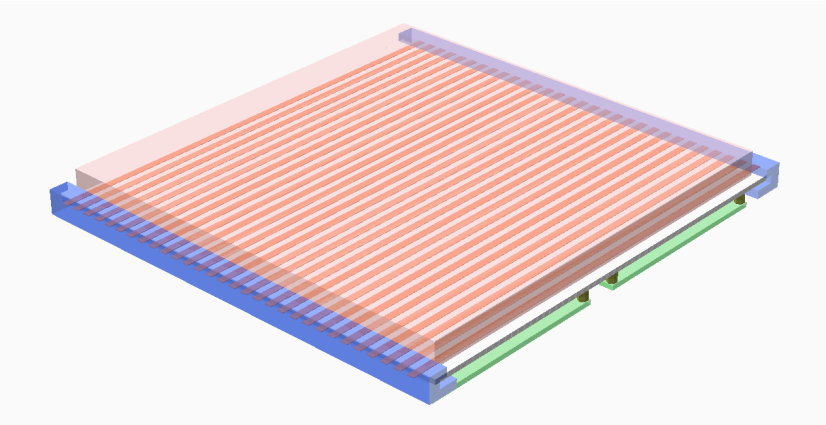

Figure 5: Redesigned boards underneath an LAPPD tile, viewed from above.

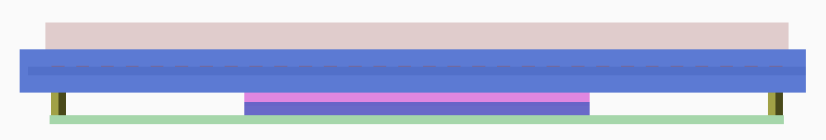

Figure 6: A demonstration of the idea of a plug adapter to connect the capacitated leads on top of the tile directly to the board(s) underneath. Dark blue represents the adapter. Pink and purple represent the male and female ends of the ribbon cable that fit together.

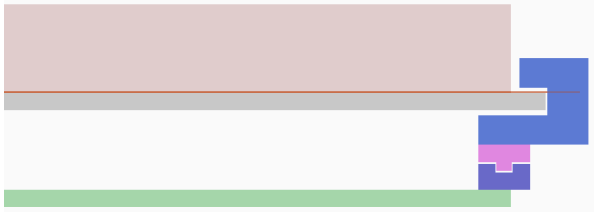

Figure 7: Head-on view of the plug demonstration.

4 Additional Comments

Two different existing ACDC boards, numbered 20 and 24, were tested with a switching regulator supplying the 1.2Va to the PSEC4 chips. I collected data on each chip of the two boards, but only show analysis for channel 3 on the modified and unmodified board 24. I chose channel 3 because it had fewer artifacts than other channels. Board 20 showed similar results to board 24. These comments relate to that testing.

4.1 Connection Issues

The most difficult part of testing modified and unmodified boards was establishing a connection between the Raspberry Pi and the ACDC boards. Establishing a connection with the boards took longer than running the actual test, making the process inefficient.

One suspicion is in the weakly connected USB port of the ACC. As seen in Figure 8, the USB port on the ACC is very weakly hanging onto the board. This is a potential source of connection and grounding issues, and it is a problem that can be seen on both ACC boards 3 and 4.

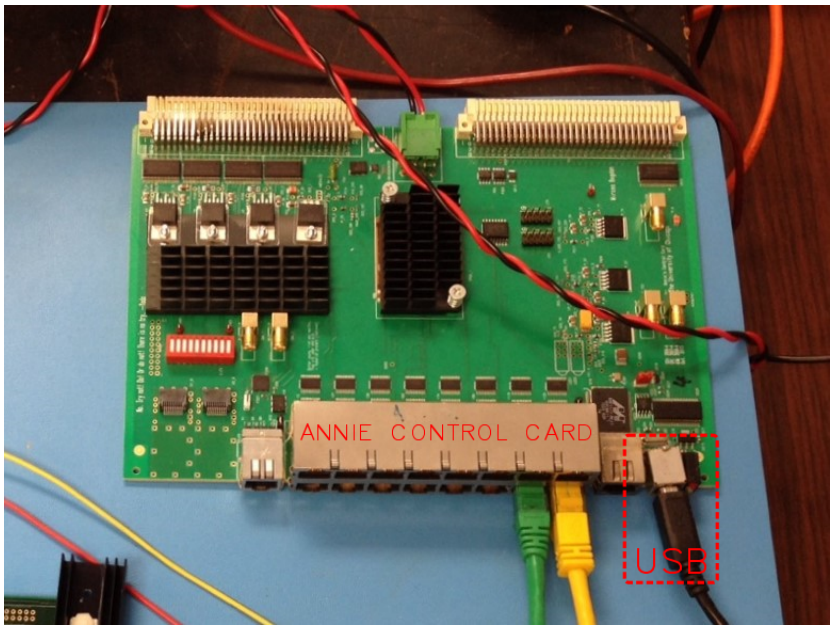

Figure 8: The loose USB connection to ACC board 4 can be seen at an angle.

Evan Angelico and Charles Whitmer attempted to help me solve these connection issues, but often the best solution was to wiggle the ends of the USB from the ACC board and Raspberry Pi, and the ends of the two ethernet cables from the ACC board to ACDC board until a connection was established.

When adjusting cables failed, we found that power cycling the whole system every few minutes would rather reliably fix connection issues. However, it is somewhat of a mystery why this should help. If connection problems were due to overheating, power cycling likely could not have helped much, because we did not leave the boards unpowered long enough to cool significantly.

4.2 Overheating

Overheating may contribute to the connection issues. After about ten minutes of operation, the power regulators and the ACDC board would become very warm to the touch. We typically experienced more connection issues when the board had been powered for longer. The problem of overheating may be addressed by the change to a switching regulator, which will dissipate significantly less power and contribute less to board heat.

4.3 Input Voltage

The A4490 has an input range of 4.5V to 34V. Currently, the ACDC board uses an input of 5V, but a large input range may be useful, as the idea of changing the input to 12V has been considered. Increasing the input voltage will not change the amount of noise introduced.[10]

4.4 Artifacts

When all triggers from one channel are plotted together, there was always an anomalous section in the middle of the waveform that flattened out. The inconsistency of the phase of the wave suggests that it is not a problem with the sample waveform, but the channel based consistency of the position of the flatness suggests it is a problem with hardware or in the programming of the FPGA.

[10] Noise is only dependent on current draw, switching frequency, and output capacitance.

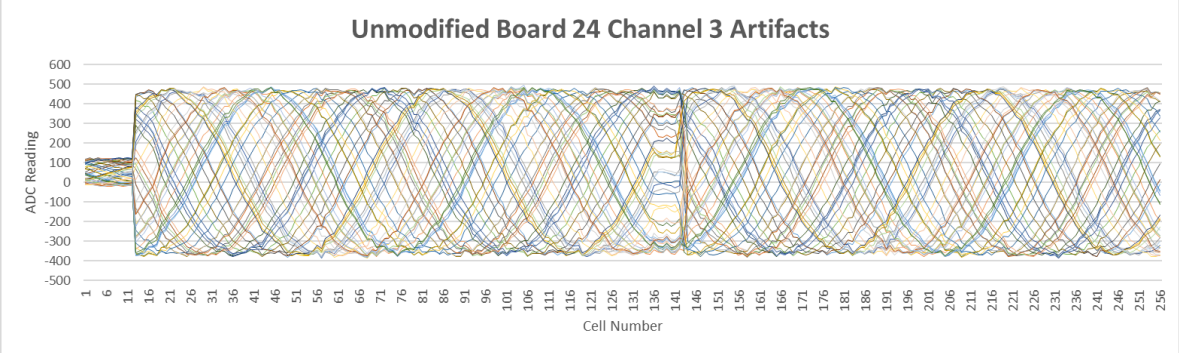

Figure 9: Artifacts on channel 3 of the unmodified ACDC board 24.

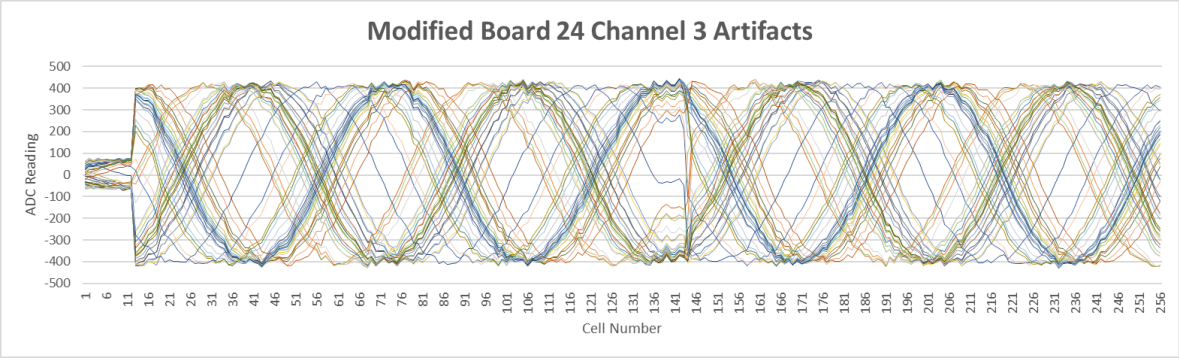

Figure 10: Artifacts on channel 3 of the modified ACDC board 24. These artifacts appear in the same location on board 24 in both the modified and unmodified states.

4.5 Testing and Results

The purpose of the tests was to determine how much noise a switching power supply would introduce into the signals collected by the PSEC chips, so the switching power supply was only used as a replacement to the PSEC-specific 1.2Va power supply.

I tested the A4490 with an evaluation board.[11]

The A4490 can handle an input voltage between 4.5 and 34 V, but requires a feedback setup for values less than 5.5 V. For an input of 5.0 V, the input must be connected to the inputs of VDD_IN and VBB, as shown below.

The evaluation board has multiple test points outside of each output to hang resistors to tune the output voltage. A resistor hung between two test points of the same REG block will add to one side of a feedback voltage divider, which compares the divided voltage to a preset V_FB (0.8 V) and adjusts the duty cycle to make the voltages equal. I found the default outputs of REG1, REG2, and REG3 were 5.0 V, 3.3 V, and 1.5 V, respectively. I chose to use REG3, and created a supply of 1.201V by hanging an 11 kOhm resistor off the test points.

To test the A4490 switching regulator with an existing ACDC board, the linear voltage regulator pin supplying power to the PSEC chips[12] was unsoldered and lifted, and a lead to the evaluation board was soldered in its place. This modification is shown in Figure 12.

Once the board was powered, I created a sample sine wave with a frequency of 100 MHz on the Arbitrary Waveform Generator (AWG), and fed it with an SMA cable to a single channel of a PSEC chip on the ACDC via the test detector board.

[11] The APEK4490EES-01-T-DK Evaluation Board, which I purchased at www.digikey.com/product-detail/en/allegro-microsystems-llc/APEK4490EES-01-T-DK/620-1388-ND/2514693

[12] The middle pin of chip LT3083 labeled "1.2Va" in Figure 1.

Figure 11: Test setup for the A4490. There is an 11 kOhm resistor hung between test points 16 and 17 of REG3 in the upper right.

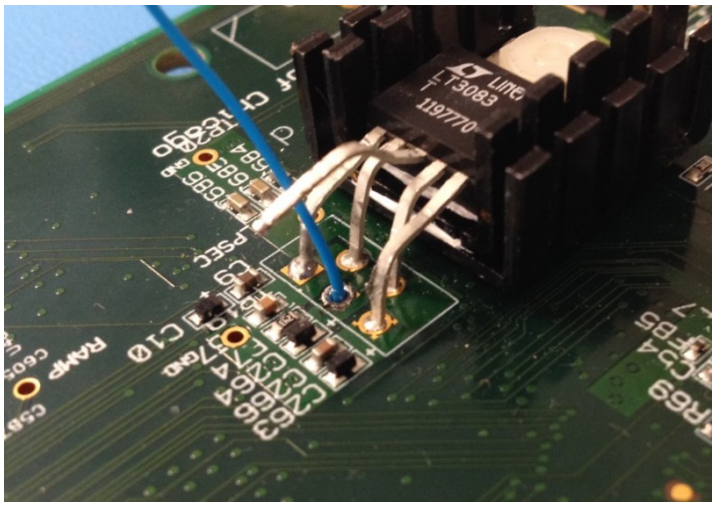

Figure 12: Lifted pin on the 1.2Va regulator, and a lead to the A4490.

To collect the data, I SSH-ed into Pi100[13], and used the command logData[14] for 50 events, with a software trigger[15]. I logged data on channels 20 and 24 of the boards I tested.

I then plotted the ADC readings for each trigger, created a best fit equation with Excel, and determined how much the data deviated from that curve, and the average amount of noise on top of the data.

I collected data on one channel of each PSEC4 chip on ACDC boards 20 and 24 in an unmodified

[13]The Raspberry Pi which was connected to the ACC.
[14]./bin/logData [name] [number of events] [trigger type]
[15]Software Trigger = 0

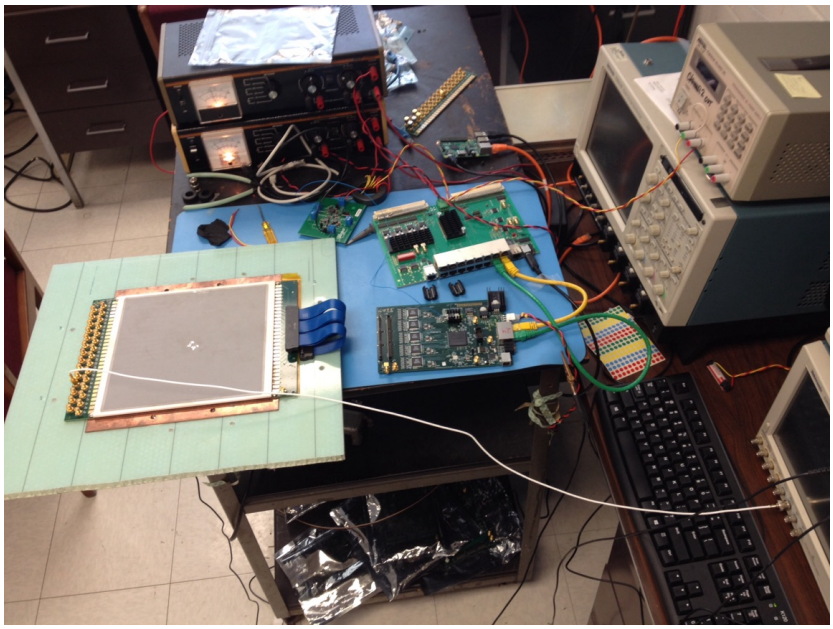

Figure 13: The test setup. The PSEC chips are powered by the A4490, a signal from the AWG is fed to a single PSEC channel, and data is collected via the Raspberry Pi.

and modified state. In the modified state, one pin of the "1.2Va" regulator was lifted, and the PSEC4 chips were receiving 1.2V from the switching regulator.

I fit each set of data with a wave of the form $Asin(Bt + \phi) + C$, where A, B, ϕ and C were free parameters, and used the Solver function in Excel to minimize the wave's deviation from the data. I then calculated the standard deviation of the residuals, excluding the time regions with artifacts at the beginning, middle and end of the waveform (see Section 4.4). I also converted the deviation to noise in mV. The anomalous portions excluded from the calculation are also excluded from the graphs.

Trigger	**Standard Deviation** (ADC Units)	**Noise** (mV)
1	12.60	3.69
2	10.95	3.21
3	11.61	3.40
4	11.99	3.51
AVG.	**11.79**	**3.46 ± 0.06**

Table 1: Noise results for Unmodified ACDC board (powered by linear regulators).

Trigger	**Standard Deviation** (ADC Units)	**Noise** (mV)
1	12.26	3.59
2	12.29	3.60
3	12.14	3.56
4	11.69	3.42
AVG.	**12.10**	**3.54 ± 0.06**

Table 2: Noise results for Modified ACDC board (powered with a switching regulator).

Figure 14: Fit waves for Triggers 1 through 4 from Channel 24 on Unmodified ACDC board 4.

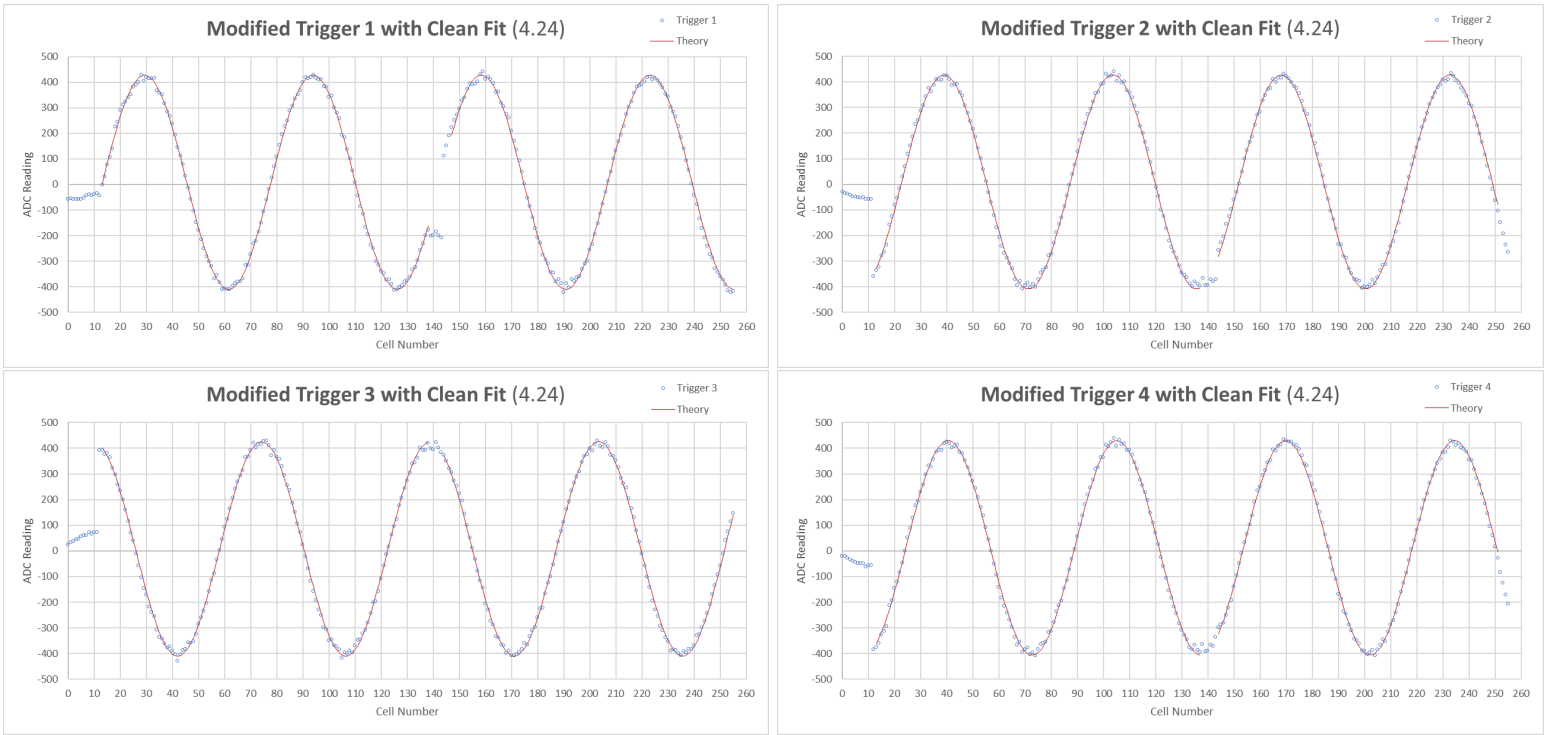

Figure 15: Fit waves for Triggers 1 through 4 from Channel 24 on Modified ACDC board 4.

This test suggests that powering the board with a switching regulator will not effect its function. The noise introduced by the switching regulator is not significantly different from the noise already observed with the linear regulators. The paper by Eric Oberla et al. "A 15Ga/s, 1.5 GHz Bandwidth Waveform Digitizing ASIC" reported 0.7 mV, but this was only after an extensive analysis of the time bins on each PSEC chip. I did not do any time bin calibration, which is why noise on the unmodified board seems so much larger. If I did the time bin calibration, the resulting noise would have been lower.

4.5.1 Noise Simulation

Before I received the A4490 evaluation board, I used a SPICE program[16] to simulate the output voltage of the regulator.

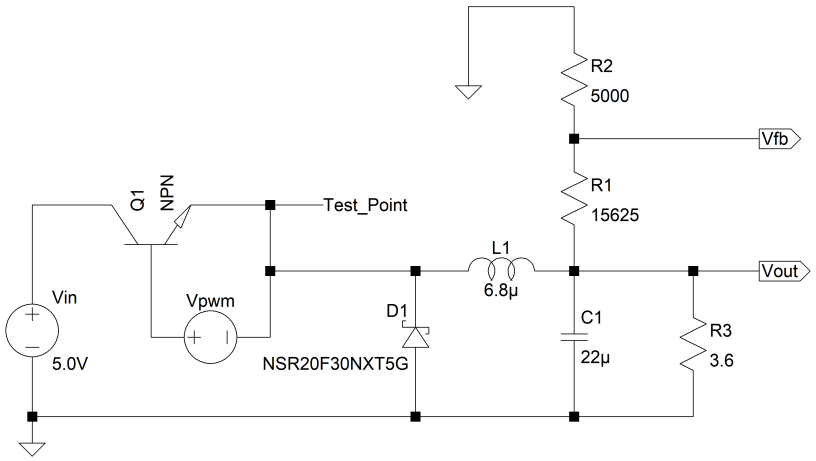

Figure 16: A simulated switching regulator. The 5 V power supply on the left represents the 5 V input to the ACDC board. The transistor on the upper left is used to simulate the switching component of the regulator. V_{pwm} is a small supply to power the transistor. The component values were calculated to create a V_{out} of 1.2 V.

Plotting the output voltage from this simulation gave me a rough idea of the amount of noise that would result. The fact that the noise is centered around 1.31 V rather than 1.2 V does not change the magnitude of the noise. It could have been adjusted with the switching frequency of the transistor.

[16] SPICE = Simulation Program with Integrated Circuit Emphasis. I used LTspice XVII, which is free.

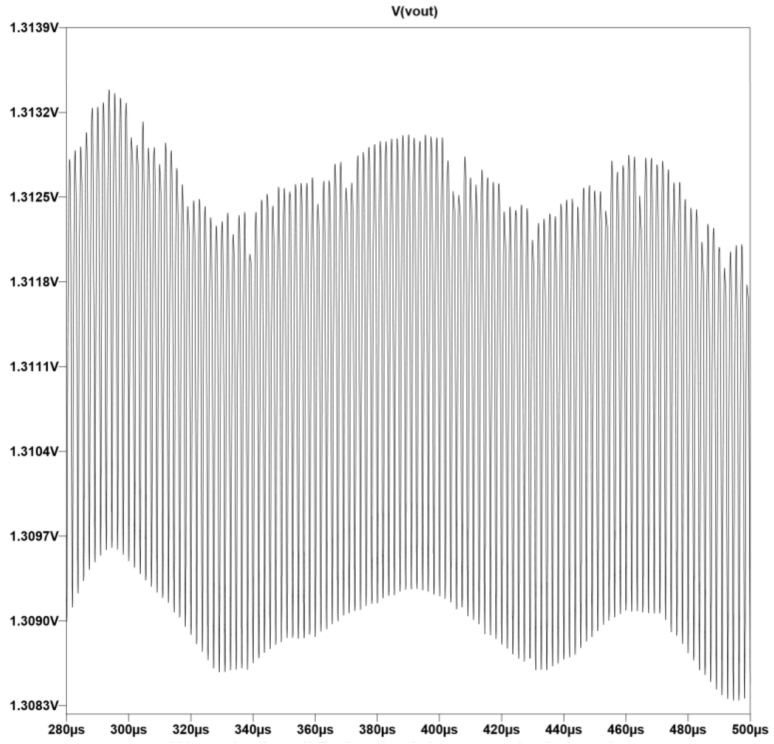

Figure 17: Output voltage graphed by LTspice. The magnitude of the noise is roughly 3.7 mV. (Note: Mircea Bogdan does not believe a simulation run in a finite amount of time can be accurate.)

5 Conclusion

To improve the function and optimize the form of the existing ACDC board, a future design should utilize switching voltage regulators (such as the A4490), remove redundant components, and optimize the dimensions and layout of the board to fit underneath an LAPPD detector tile, all while maintaining plug compatibility to continue to function with the current detector setup.

Testing ACDC boards with two different power regulation systems determined that the function of the board is not altered significantly by the use of a switching power supply, as the noise observed by the board with the two different regulators is comparable. The switching power regulator may have additional benefits, such as a lower operating temperature due to less power dissipation, and more free space on the board due to a smaller area of supporting electronics and no need for heat sinks.

6 Acknowledgments

Going into this project, I knew very little about electronics, and even less about the process of designing a board. I have to thank many people for helping me through the project. First of all, Eric Oberla for describing the problems with the current board and giving me hints along the way. John Podzcerwinski for explaining all the electronics, walking me through test procedures, and answering all my questions. Mircea Bogdan for the suggestion of lifting a pin on the board to test my regulator. Evan Angelico for helping me with data acquisition and solving pesky connection problems. Mark Zaskowski for the great soldering work to implement my test setup. Bernhard Adams for assistance in removing input noise, and for helping me tame the oscilloscope. Charles Whitmer, my dad, for teaching me electronics concepts, helping me run simulations and use Cygwin, and for jiggling all the cables until I could connect to the Pi. And finally, Henry Frisch, for giving me the opportunity to work with the PSEC group, and providing me with meaningful feedback on my ideas. It was truly a pleasure working with the PSEC group this summer.