# Transmission-Line Readout with Good Time and Space Resolution for Large-Area MCP-PMTs

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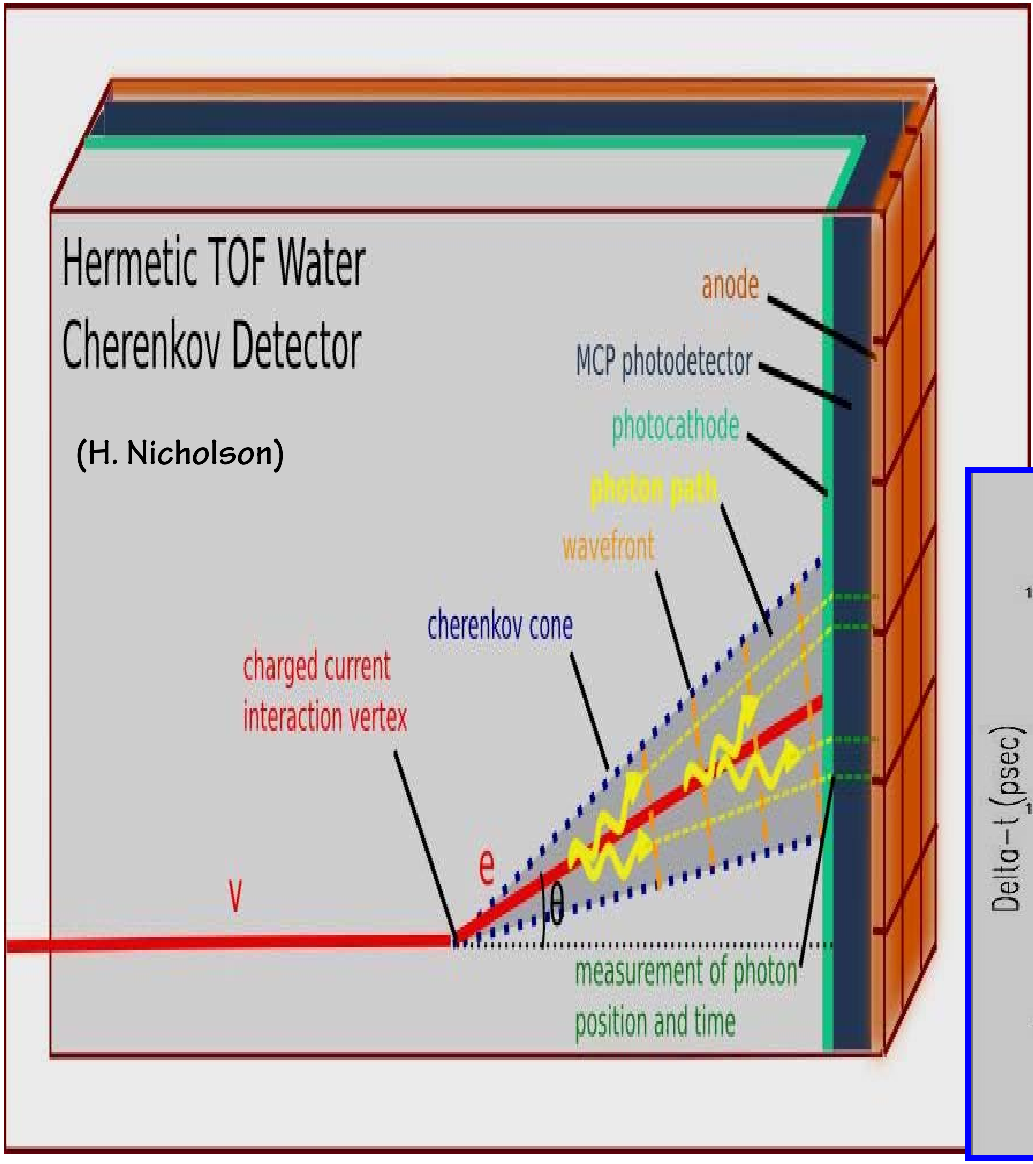
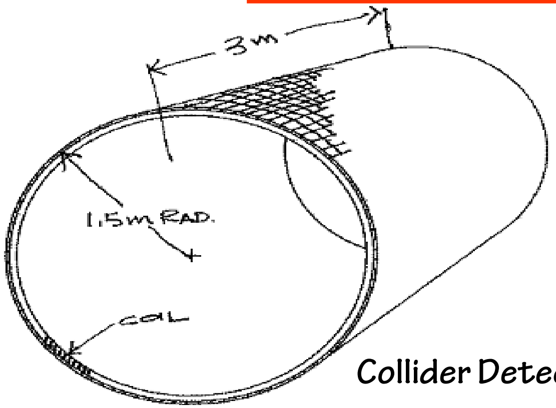
- Introduction
- Characteristics of MCP-PMT output signals
- Readout techniques for picoseconds timing measurements
- Transmission-line readout design and simulations
- 40Gsps fast sampling chip design
- Summary & plan

TWEPP 2008, Naxos, Greece, September 15-19 2008

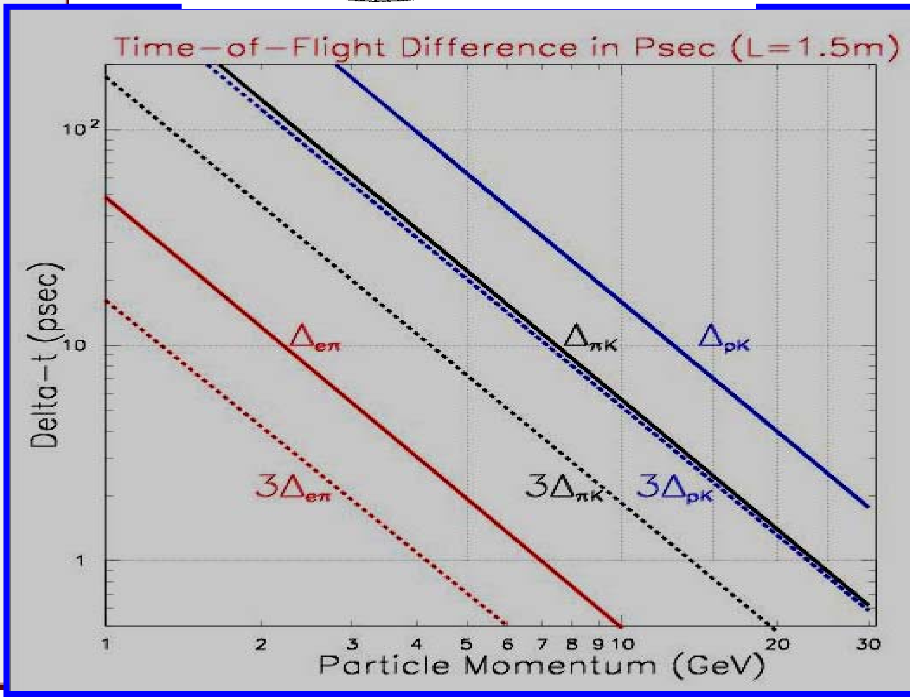
# Introduction: Applications of Time-of-Flight for HEP

Courtesy of H. Frisch



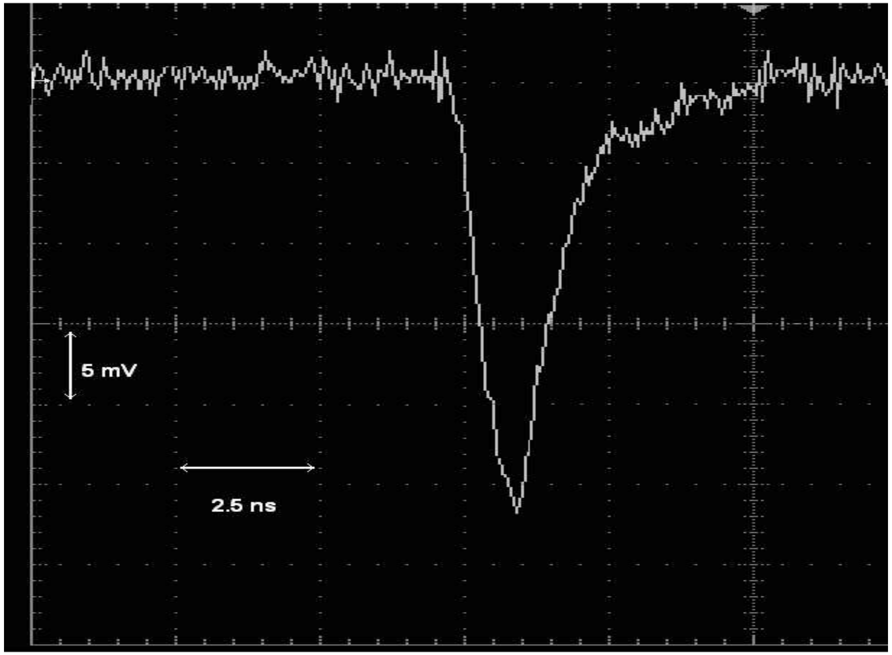



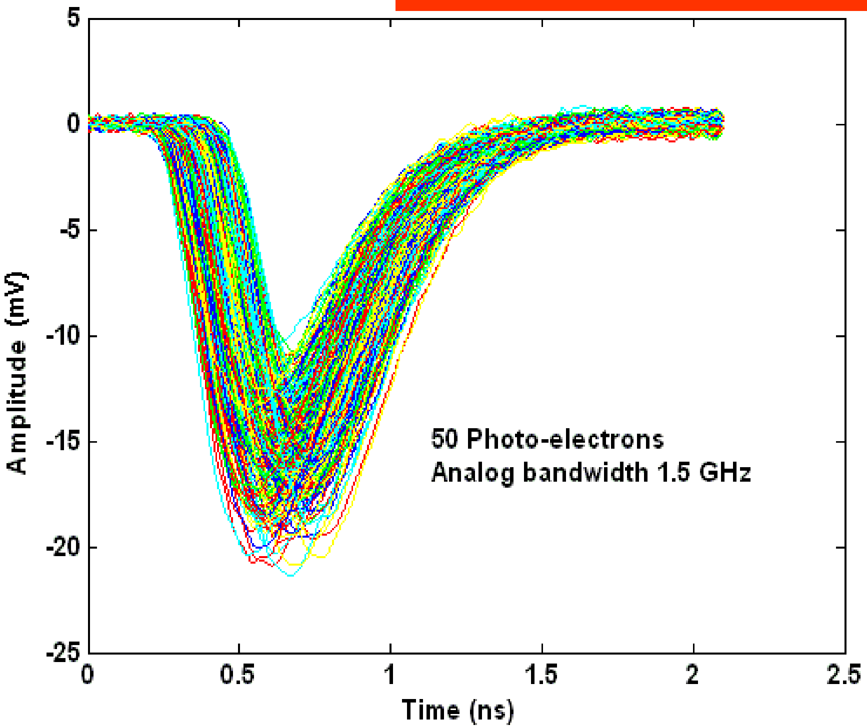

Collider Detector



# MCP signals

Courtesy of J-F. Genat



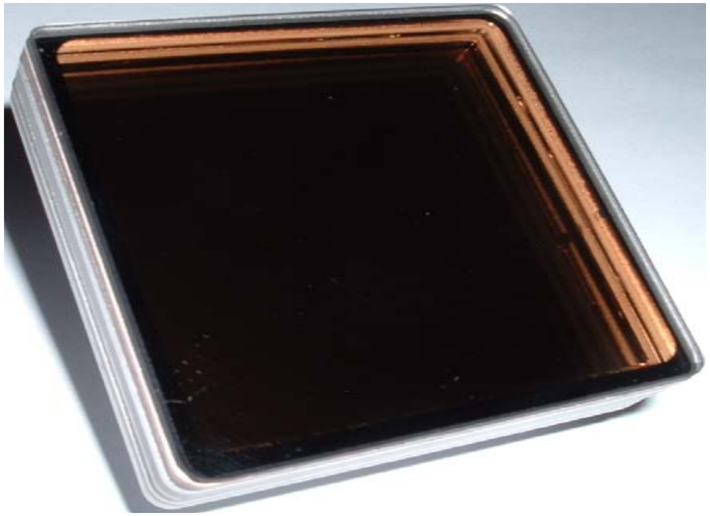



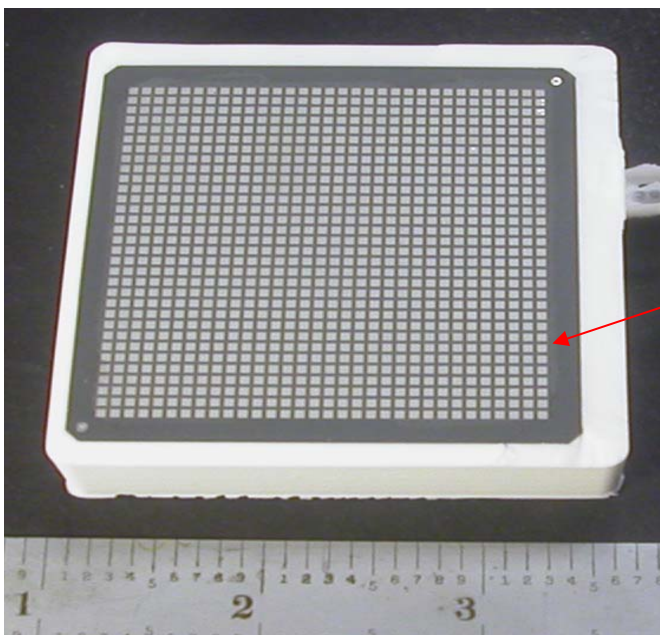

- Measured (beam-tests) :
- Rise-time: 380ps
- 25um pores

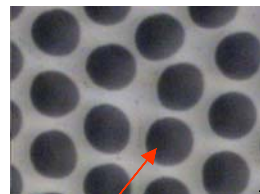
Simulation:

- Rise time 200ps (6um pores) →bw=1.75GHz
- Time spread: +/- 125ps, random
- Amplitude spread: 14%, normal

# Introduction: Planacon MCP-PMT Tube & Anode Array

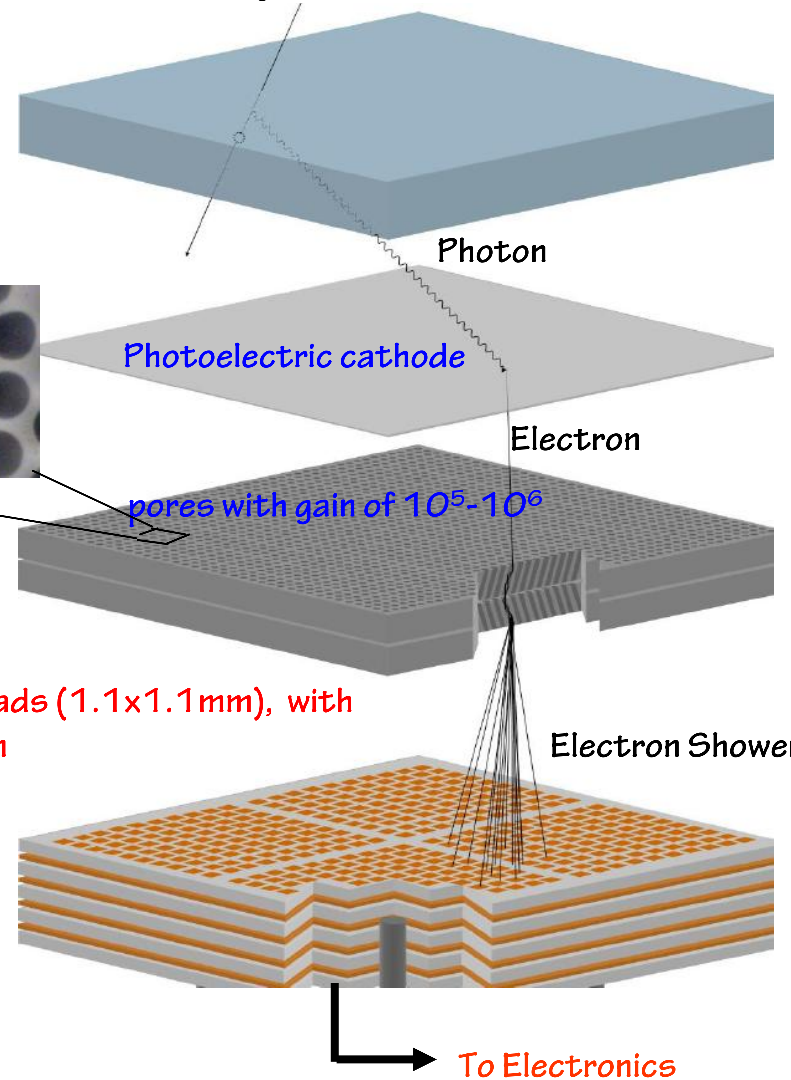




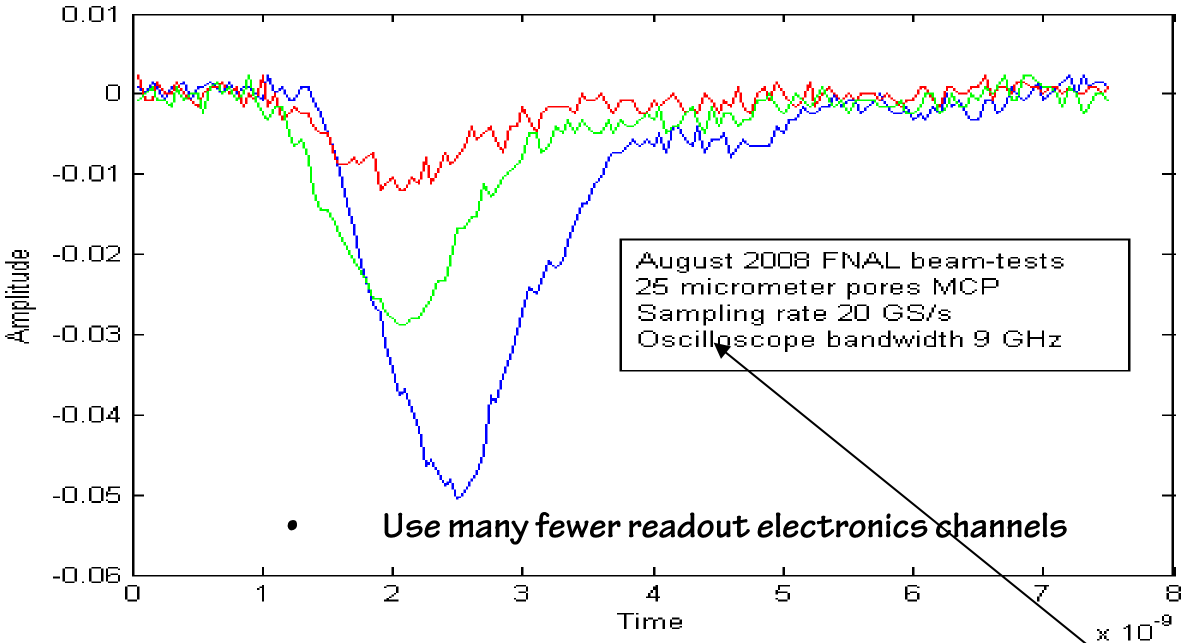


Pore Size 25u

1024 anode pads (1.1x1.1mm), with pitch of 1.6mm



# MCP signals (beam-test)




- Use many fewer readout electronics channels

25 um pores
Two stages MCP
Gain ~$10^6$

**As measured at Fermilab (beam-test, 10-50 PEs)**

I (1PE) = dQ/dt ~ $1.6\times10^{-19}$ x $5\times10^{5}$ / 250 ps = 320 uA
Expect: 16 mV @ 50 Ω

# Fast Timing Electronics

***Current techniques:***

- Leading edge + TDC/ADC
- Constant fraction + TDC/ADC
- Zero-crossing + TDC
- Double / multiple thresholds + TDC/ADC

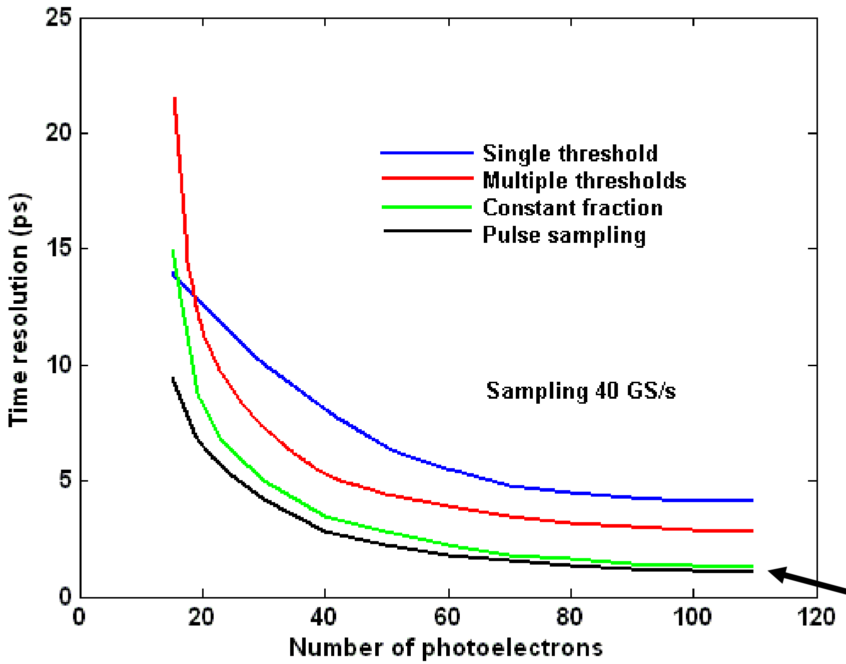
- *Pulse sampling and reconstruction*

The most favorable method is sampling, particularly in the case of few Photo-electrons. Samples as effective for timing as steep signal slope and large signal/noise ratio

Use today existing sampling chips in first step:
Hawaii, PSI, Saclay/Orsay (sampling rate @2-5 GHz, 10-13 bits)

- Derive accurate time and charge using digital signal processing
- Resolve pile-up, transmission line readout ambiguities

# Fast timing simulations




Monte-Carlo simulations

MCP signals
- 200ps rise time
- 400ps fall time
- 10-100 Photo-electrons
- MCP noise 50%
- White noise 50%
- S/N 10-100

Fast Sampling simulation
- Sampling frequency 40 Gsps

*Pulse sampling*

Assume 1.5 GHz analog bandwidth:
100 samples taken at 10-40 Gsps allow reconstructing time to a few picoseconds and charge to one per cent.

- Better time resolution compared to CFD particularly at low PEs,
- Records the full pulse information

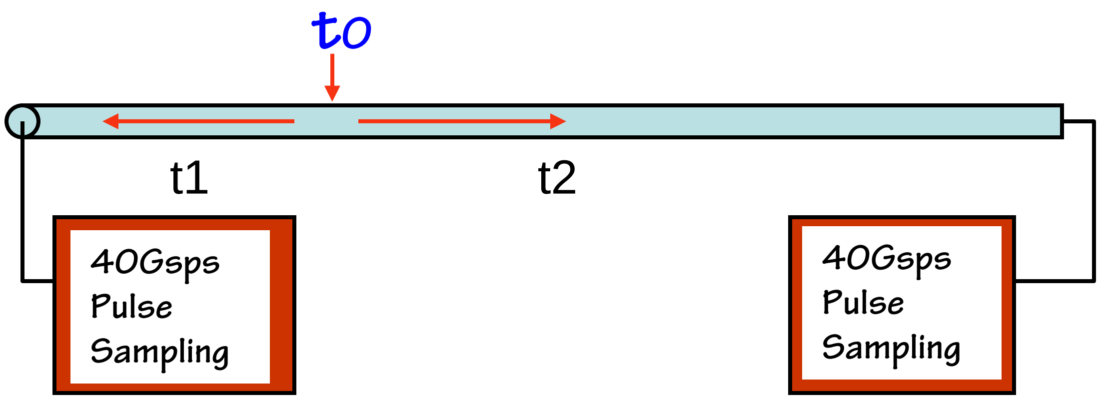
# Proposed Transmission –line and Fast Sampling Readout for Planacon MCP-PMT

## Why use transmission-line readout?

Advantages of transmission-line and fast sampling techniques:

- Use many fewer readout channels (1024 down to 64 channels)
- Readout timing, position and energy information
- Good transmission-line bandwidth (up to 3.5GHz )

# Principle of Transmission-line Anode Readout




**Timing:**

( Sampling over the peak)

$$t_0 = \frac{t_1 + t_2}{2}$$

**Position:**

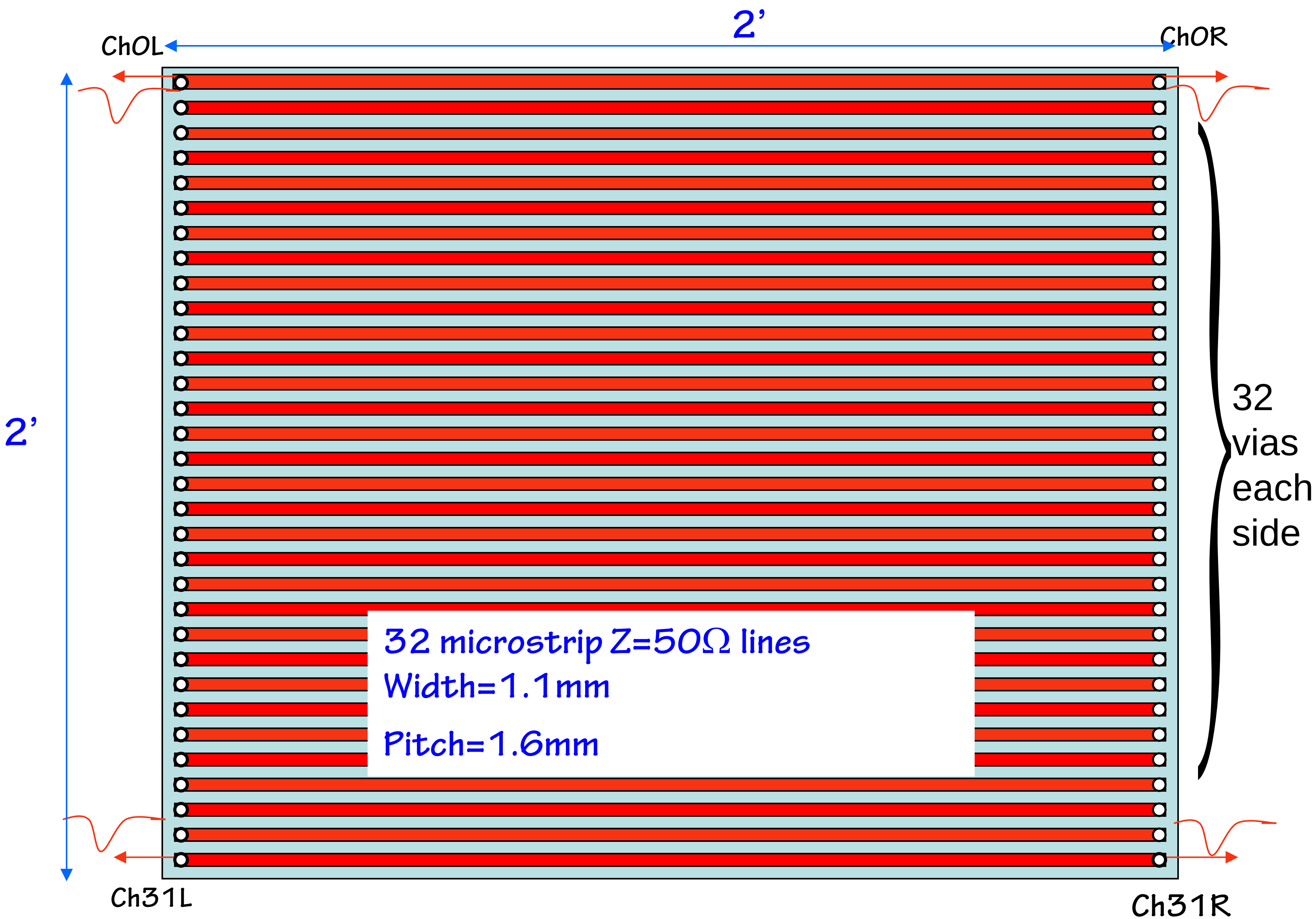
$$x_i = \frac{t_1 - t_2}{t_1 + t_2}$$

**Energy:**

(Full waveform sampling)

$$E_i = q_1 + q_2$$

# Proposed Transmission-line Anode Board (top view)



# Prototype Transmission-line Readout Board Design and Simulations Based on Commercial 2'x2' 1024-Anode Tube

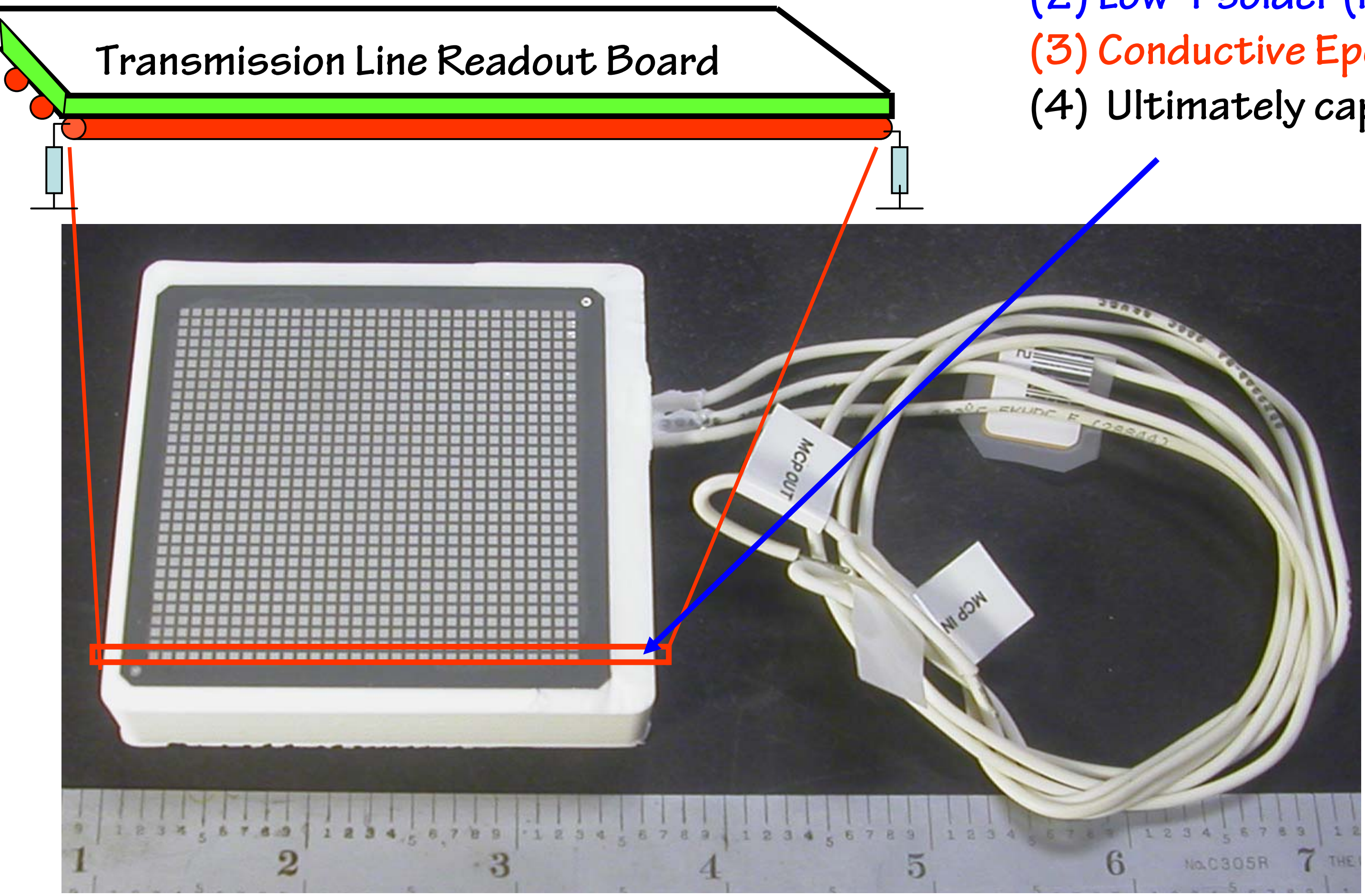
Interconnection:

(1) Elastomer

(2) Low-T solder (indium)

(3) Conductive Epoxy

(4) Ultimately capacitive coupling

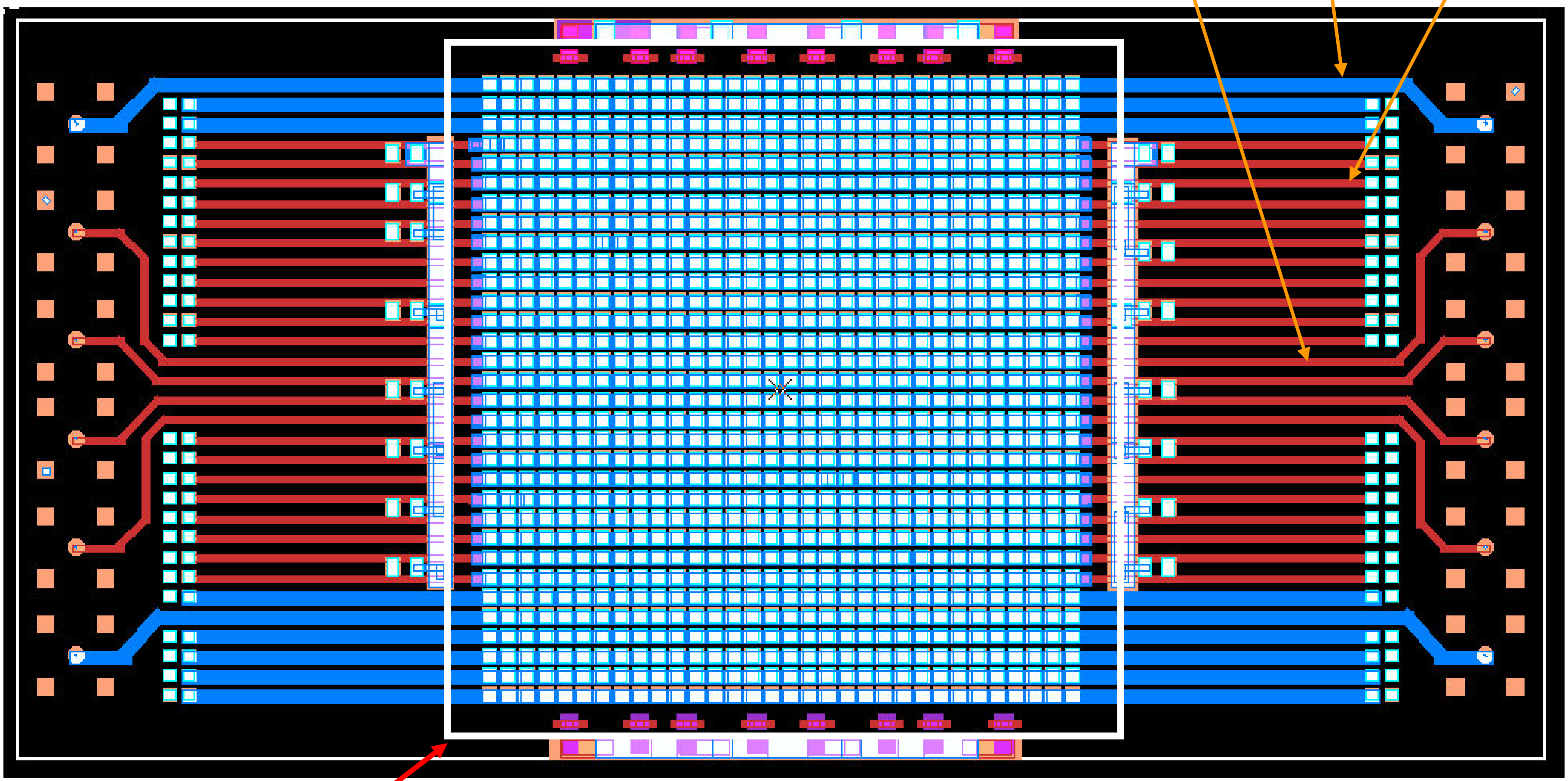


# Layout of Prototype Transmission-line Readout Board

Board Size: 130x60mm

Board Thickness: 1.2mm

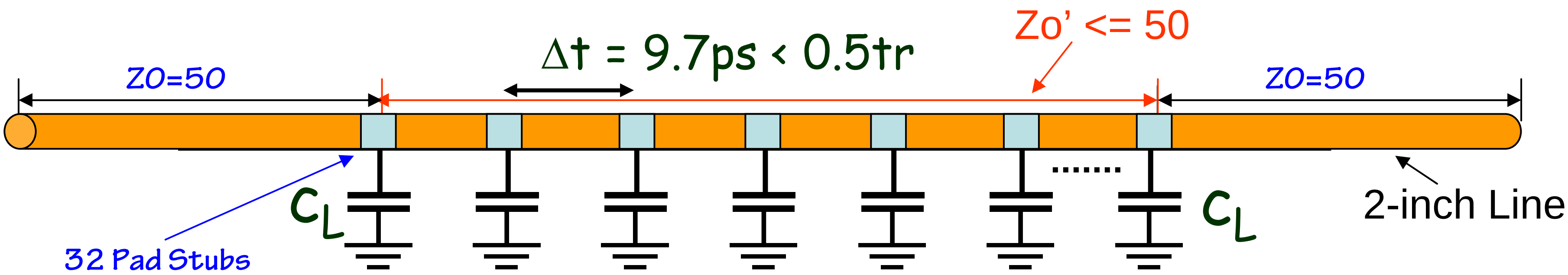
Trace length: 5.36', 4.83' , 3.97'



Tube Outline 58x58mm

# Bandwidth Analysis for Transmission-line Readout

Simplified model with the transmission-line readout board attached to MCP-PMT:




**Equal distributed 32 $C_L$=100f along 2-inch line, It reduces impedance to Zo', However, it also reduced the BW.**

$$Zo' = \sqrt{\frac{L}{C + \alpha C_L}}$$

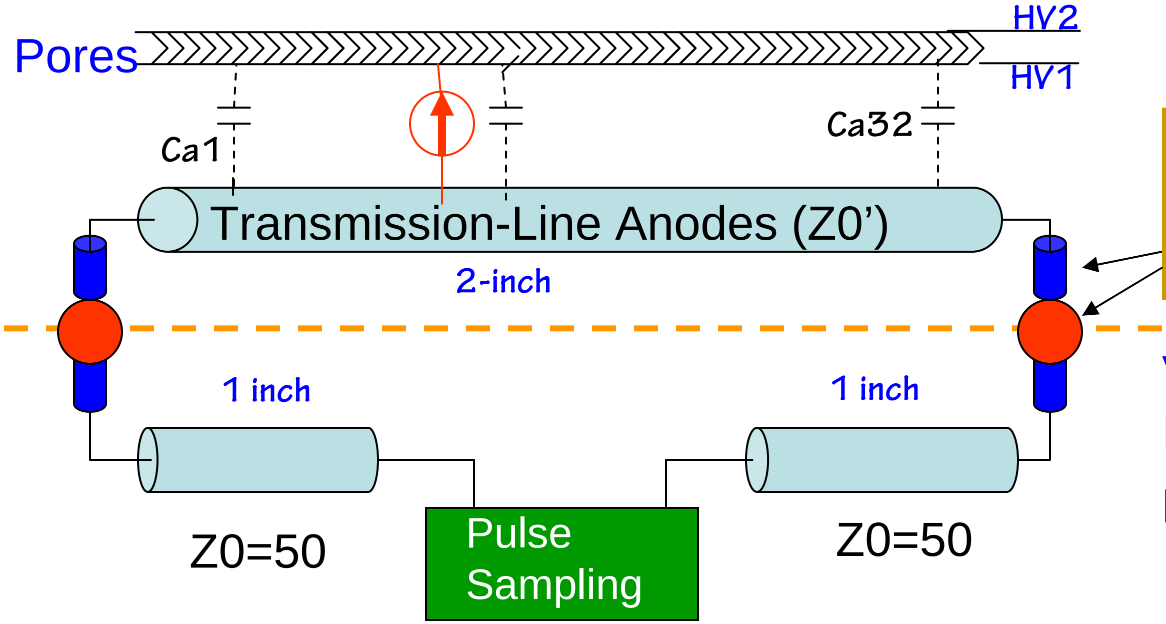
$$Tr = 2.2\tau = 2.2\frac{Z_0}{2}\alpha C_L \approx 100\,ps$$

$$\alpha = \frac{nC_L}{Length}$$

$$BW \approx 3.5GHz$$

$$\alpha C_L = 1.6\,p$$

# System Modeling for Transmission-line Readout Simulation



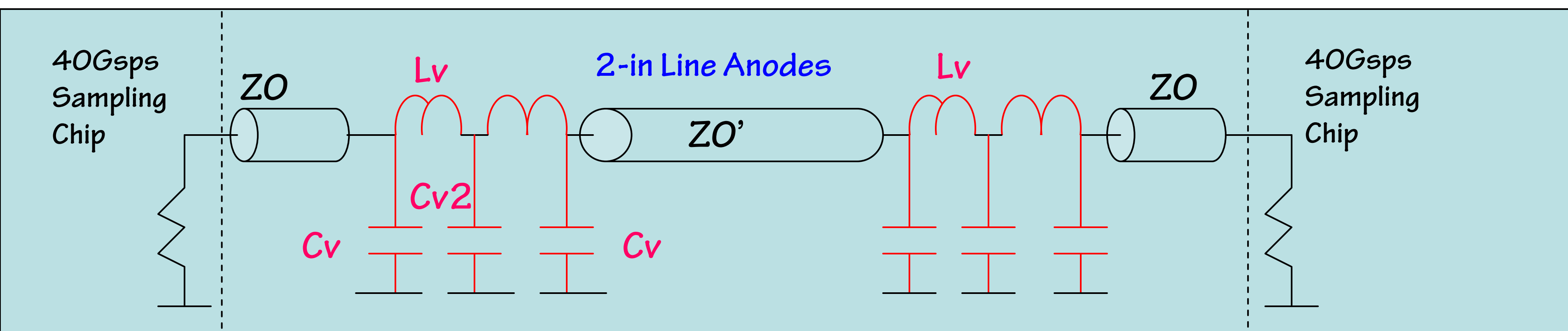

Impedance discontinuity caused by vias and ball contacts

Via size: 15x10x5 mils

Board Thickness: h=62mils

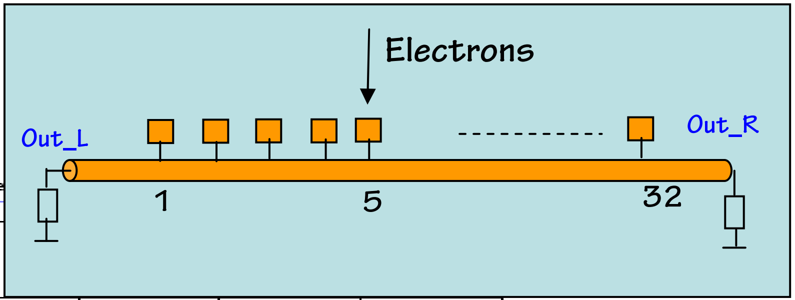
Lv=0.3n, Cv=150f

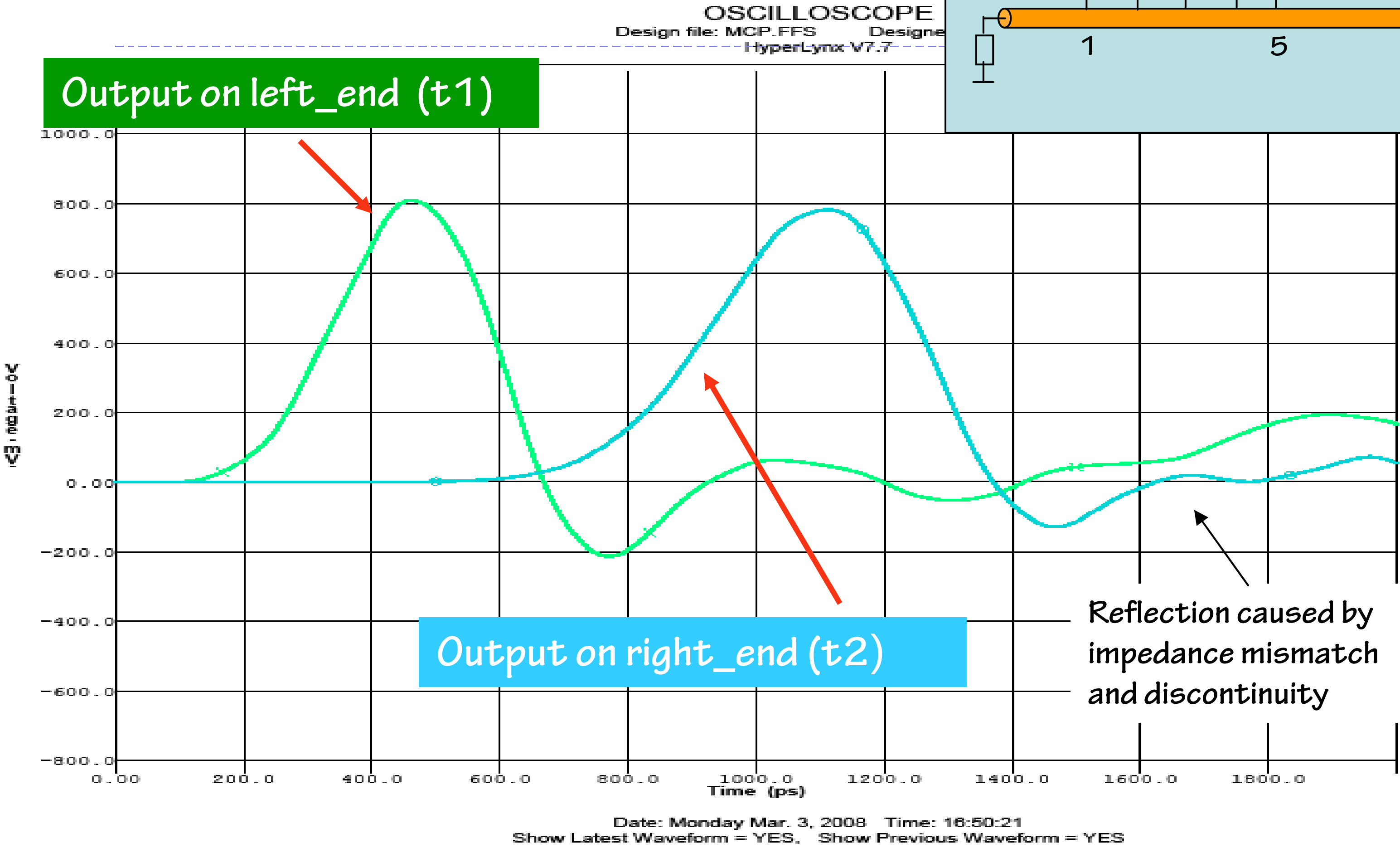
Zvia=31.6Ω



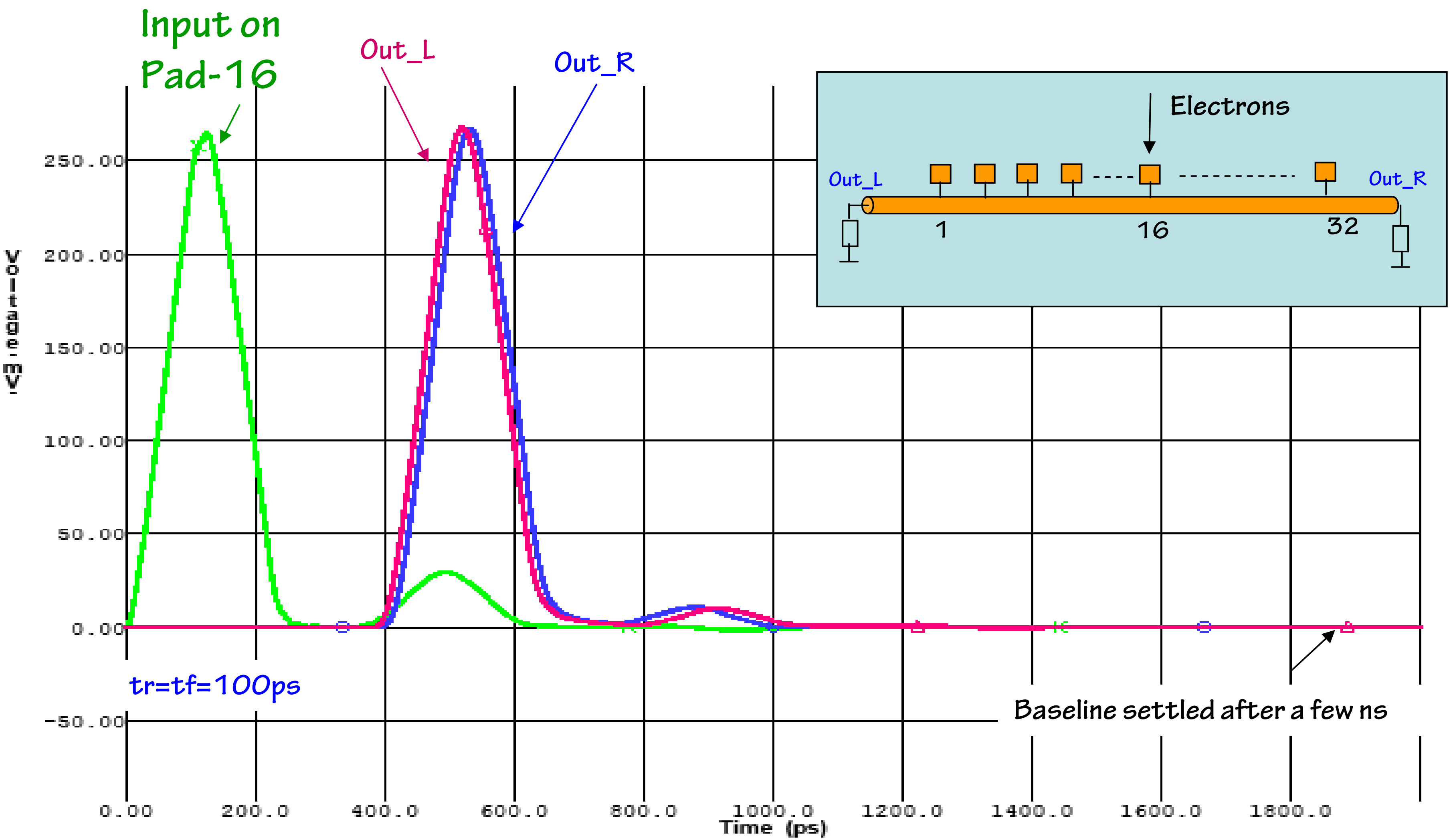
# Outputs on Each End of Transmission-line with Stub Anodes (hit at pad-5)

Input Force: Tr=tf=200ps

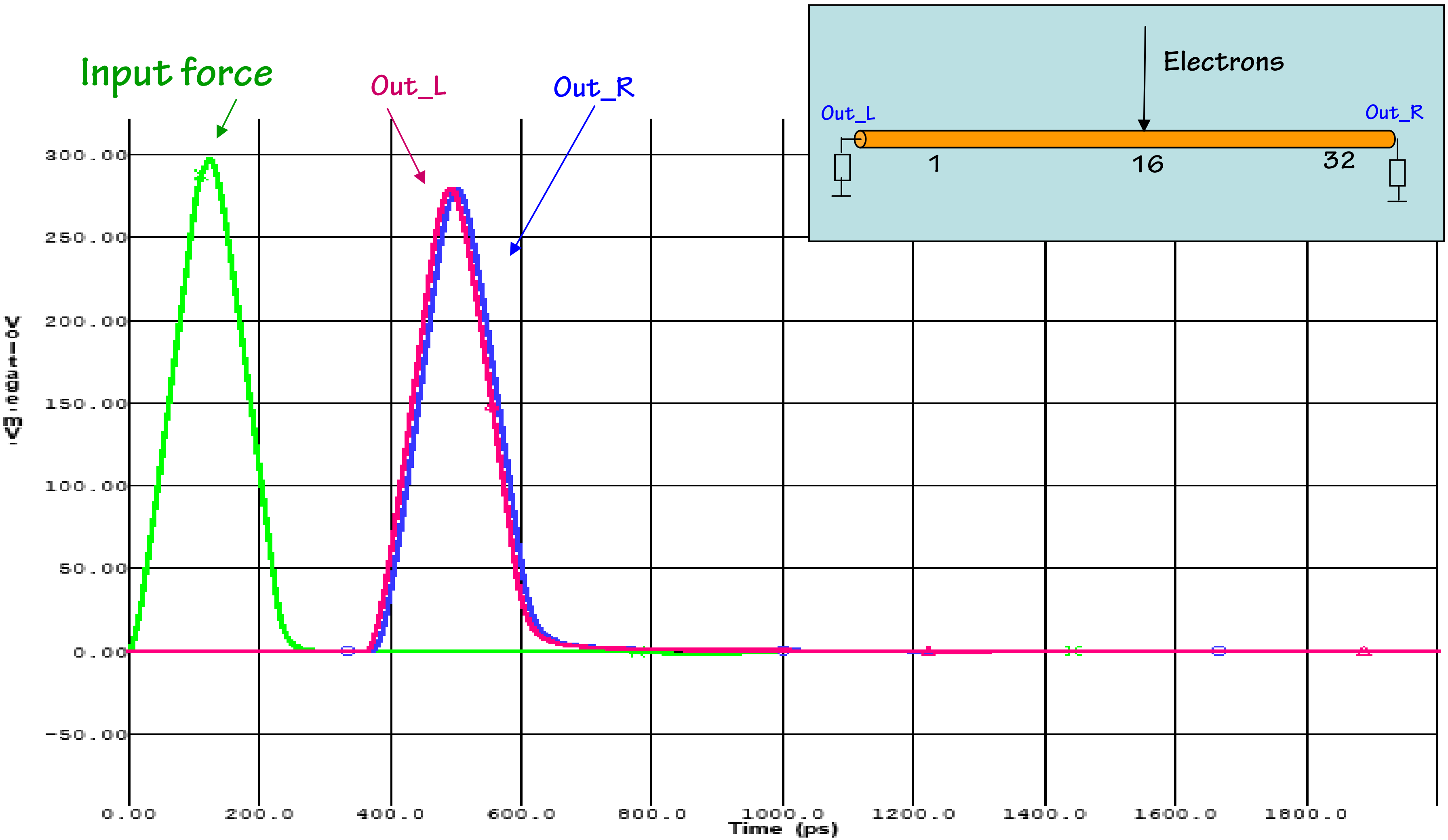


# Outputs on Each End of Transmission-line with Stub Anodes (hit at pad-16)



# Outputs on Each End of Transmission-line without Stub Anodes (hit at the same position as pad-16)



# Simulation with Transmission-Line Anode up to 48-inches

**Simulation Goal:**

To understand analog signal bandwidth vs. the length of transmission-line for MCP anode design.

**System Setup:**

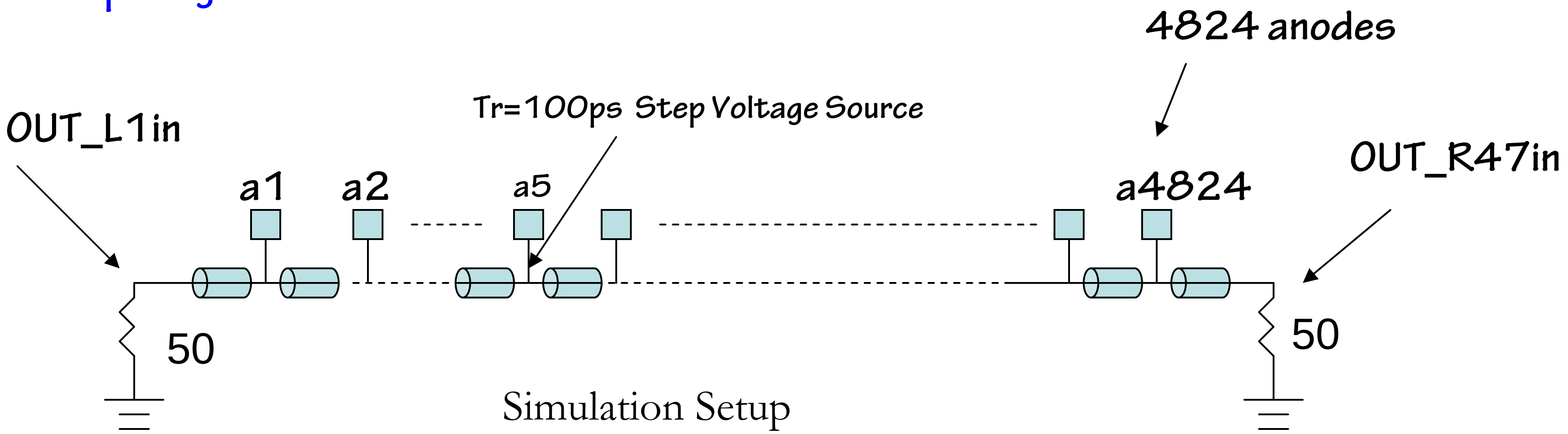
The simulation model is extracted from a board layout. The transmission-line impedance Z=50 ohms, the length is 48-inch with 4824 tapped anodes which induce 100f capacitance each.

**Input Force:**

A step voltage input force with a rise time of 100ps, an amplitude of 1.4V excites the line at the point 1-inch from the left end.

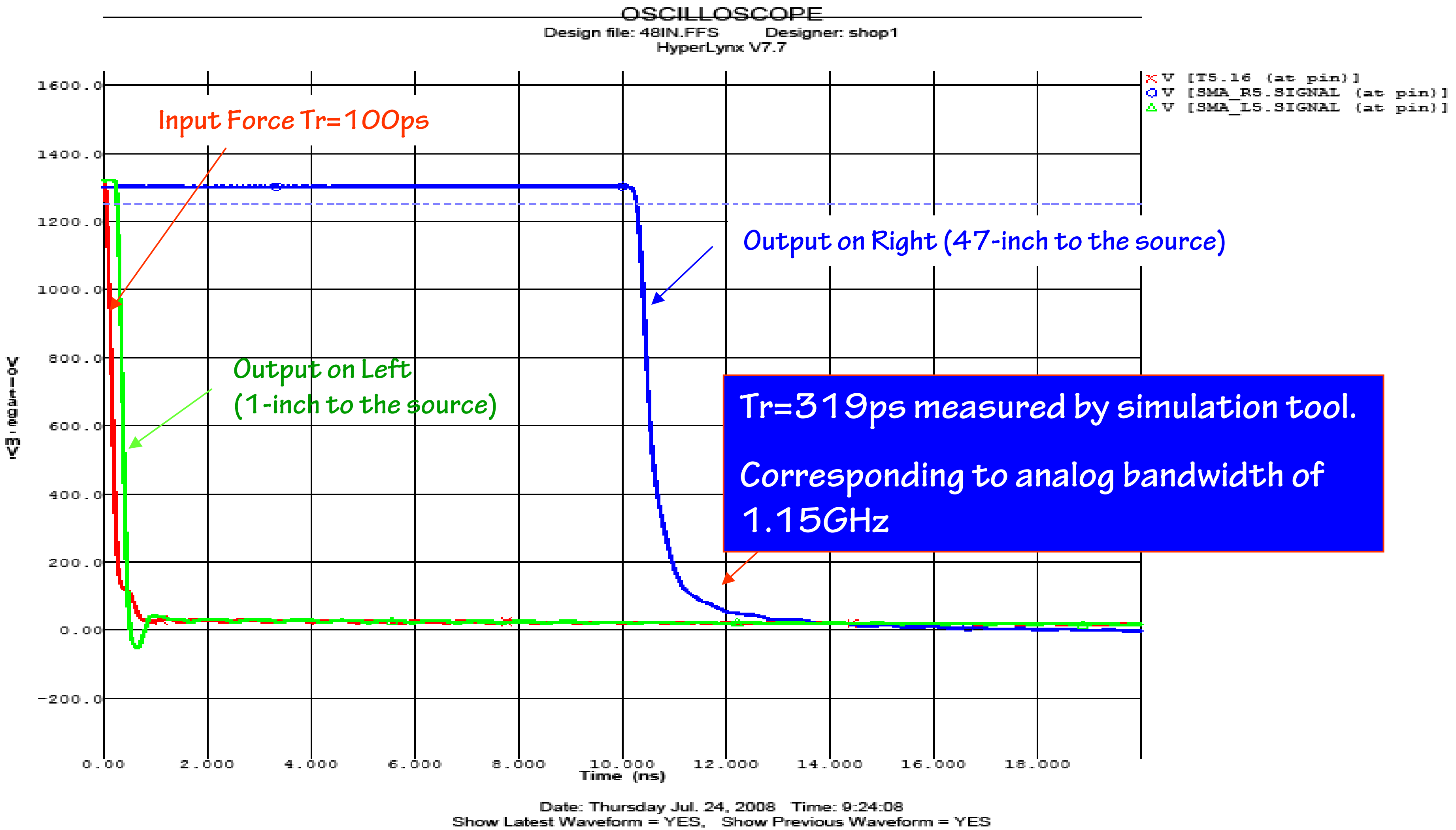
**Outputs:**

Comparing the rise time between both ends of the line.

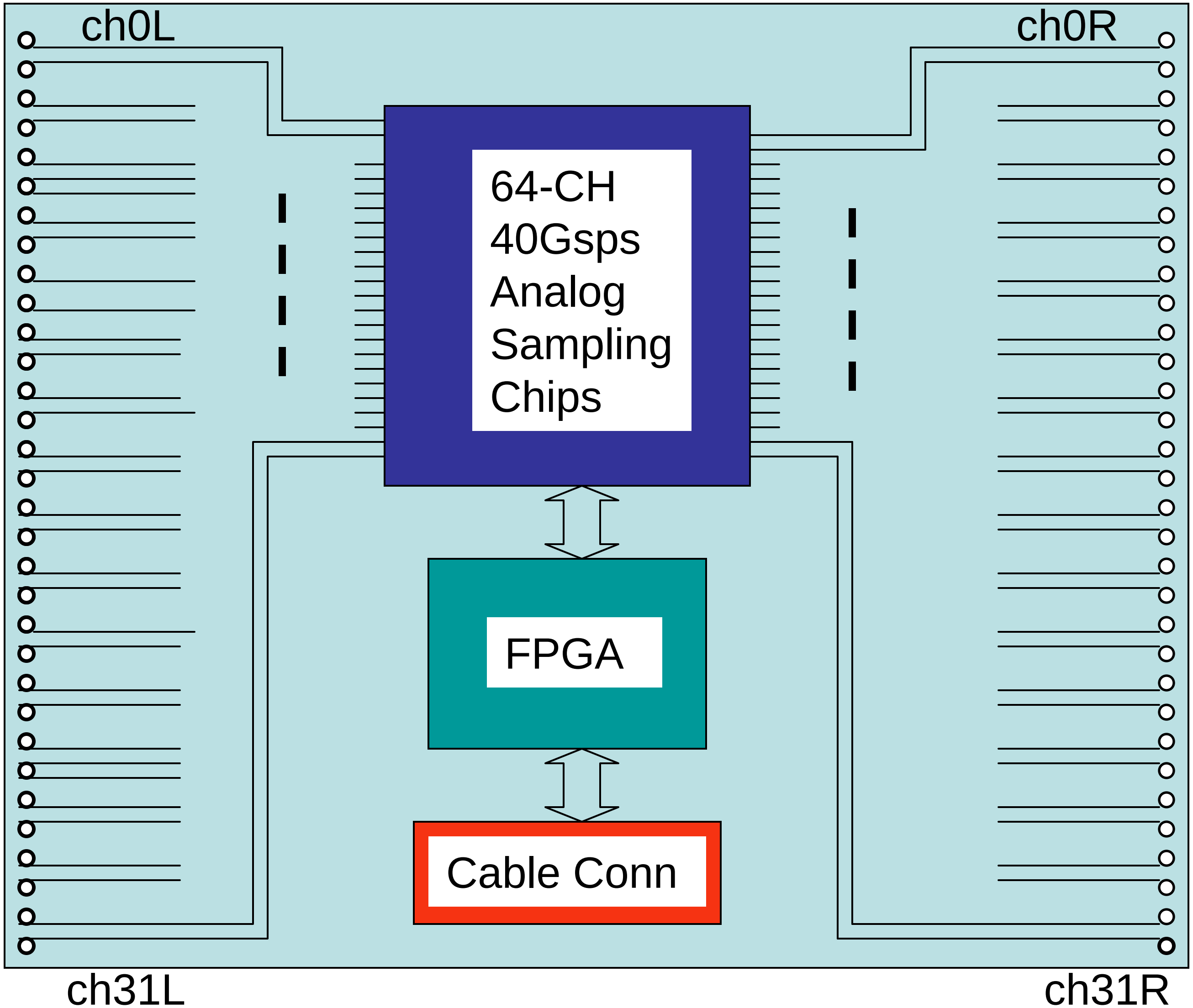



Simulation Setup

# Responses on each end of 48-inch transmission-line (Hit at the position 1-ch to the left)



# Conceptual Design of Transmission-line and Fast Sampling Readout Electronics




*Only 64-ch readout electronics needed!*

# Fast sampling chip at UChicago

- Technology:  IBM 8RF DM 130nm CMOS design kit from CERN
- Key numbers of UChicago Fast Sampling Chip
  - -- 40 GHz sampling
  - -- 1-2 GHz analog bandwidth
  - -- 8-10 bit ADCs
  - -- Self/Global trigger
  - -- Time Stamping
  - -- Readout protocols
- Work in Progress:
  - Unity gain input buffer design(1-2GHz BW)
  - Analog bandwidth is 1.6 GHz (-3dB) using current mode amplifier has been achieved (pre-layout).

To be improved:

Tuning input impedance of 200Ω to 50 Ω with the IBM130nm CMOS DM (analog RF) process when available.

--Extend analog bandwidth as far as possible, if input buffer can not meet the requirement.

-Sampling timing generator design

-Sampling cells and ADCs: Experience from Orsay/Saclay, Hawaii and PSI.

**Expect 2-3ps timing resolution with MCP signals**

# Summary

## Advantages:

- Use many fewer readout electronics channels
- Readout timing, position and energy information
- Good signal bandwidth
- Easy to match impedance all the way to the chip input

## Plans (short and long term)

- Prototyping transmission-line readout with laser stand and 40Gsps scope (in few weeks)
- Transmission-line readout with two LAB2 or two DRS4 Chips (possibly 2x interleaving?) (in few months)

- Development of 40Gsps sampling chip for large scale detectors
  ---2-ch demonstration chip with IBM 8RF 0.13u CMOS (year 1)
  --- 32/64-ch chip (year 2)
- Built-in transmission-line anode design and simulation (need to work with tube designers)