A data acquisition (DAQ) system using the 10 - 15 Gigasample/second (GSa/s) PSEC4 waveform recording Application Specific Integrated Circuit (ASIC) has been developed as part of the Large Area Picosecond Photo-Detector Collaboration (LAPPD). The PSEC4 chip, a 6-channel 0.13 μm CMOS waveform digitizer, was designed as a first generation readout ASIC for these large-area microchannel plate (MCP) photosensors. The full PSEC4 DAQ system architecture incorporates two levels of hardware, FPGA-embedded system control, and data processing. At the front-end is a 30 channel unit that holds five PSEC4 ASICs and a control FPGA that plugs directly into one terminal of the LAPPD MCP anode. The analog bandwidth of the signal input is 1.5 GHz. In order to record waveforms at both ends of the LAPPD anode, two of these cards are required to fully instrument an LAPPD MCP. The back-end card houses the system control FPGA, distributes the system clock, and manages up to four front-end units by means of eight 800 Mbps LVDS lines. This back-end card communicates to a PC using USB 2.0 or gigabit Ethernet.

System Hardware

Central Card
- Controls 4 front-end boards
- USB 2.0 or gigabit Ethernet PC connection
- Daisy chain or tree configurations to extend system channel count
- Clock fan-out

Front-end PSEC4 Card ("AC/DC Card")
- 30 channels PSEC4 waveform recording
- At 10GS/s, captures a 25 ns snapshot per waveform
- USB 2.0 standalone readout or 8x LVDS lines communication to Central Card

PSEC4 Evaluation Card

Photo-detector Integration

Both MCP detector configurations are equipped with a microstrip anode readout:

2x2 sq. in Planacon MCP
8x8 sq. in LAPPD MCP

References:
A 15 GSa/s, 1.5 GHz Waveform Digitizing ASIC, NIM A732, p452, Jan. 2014.
A test facility for large-area microchannel plate detector assemblies using a pulsed sub-picosecond laser, RSI, Volume 84, Issue 6.
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