PSEC4 waveform sampler
&
Large-Area Picosecond Photo-Detectors readout electronics

12-March 2014 : *Workshop on Picosecond Photon Sensors, Clermont-Ferrand*

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HIGH ENERGY PHYSICS

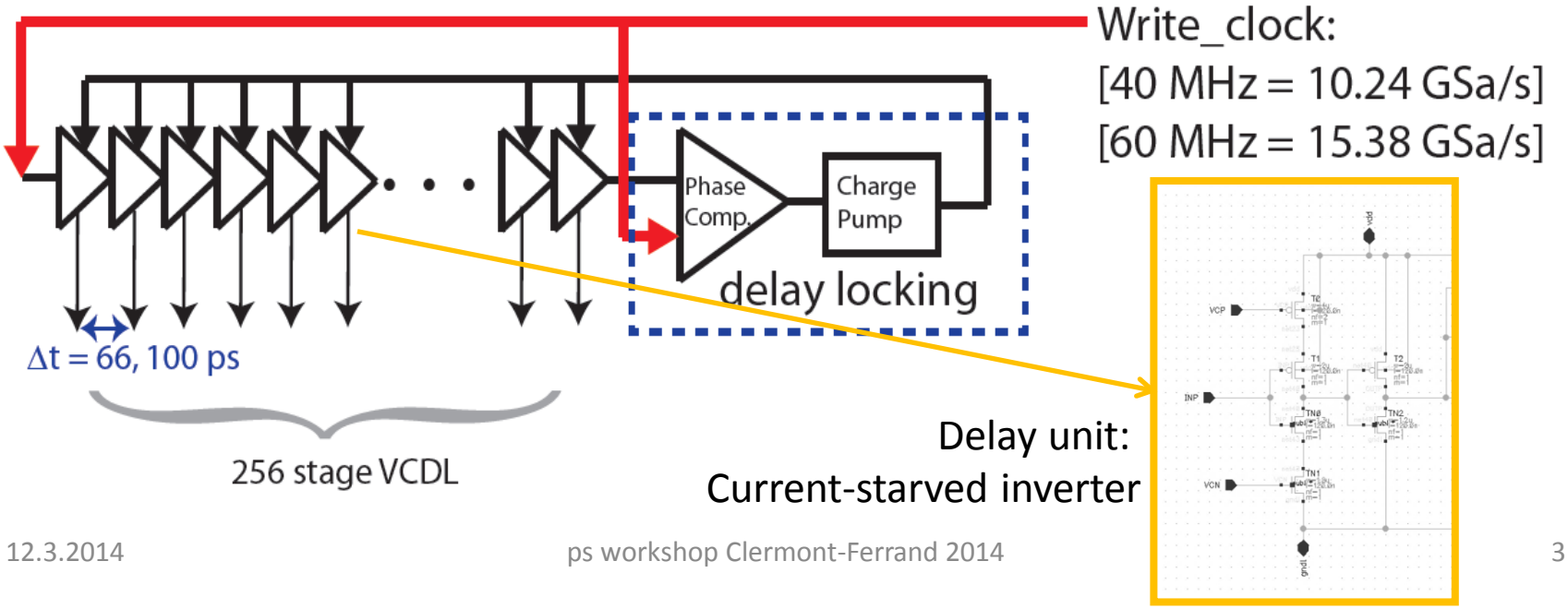
THE UNIVERSITY OF CHICAGO

Overview

- PSEC4 waveform sampler/digitizer
- The Large-Area Picosecond Photo-Detectors (LAPPD) **glass package**
- DAQ system : readout of large area micro-channel plates
- Plans for PSEC5

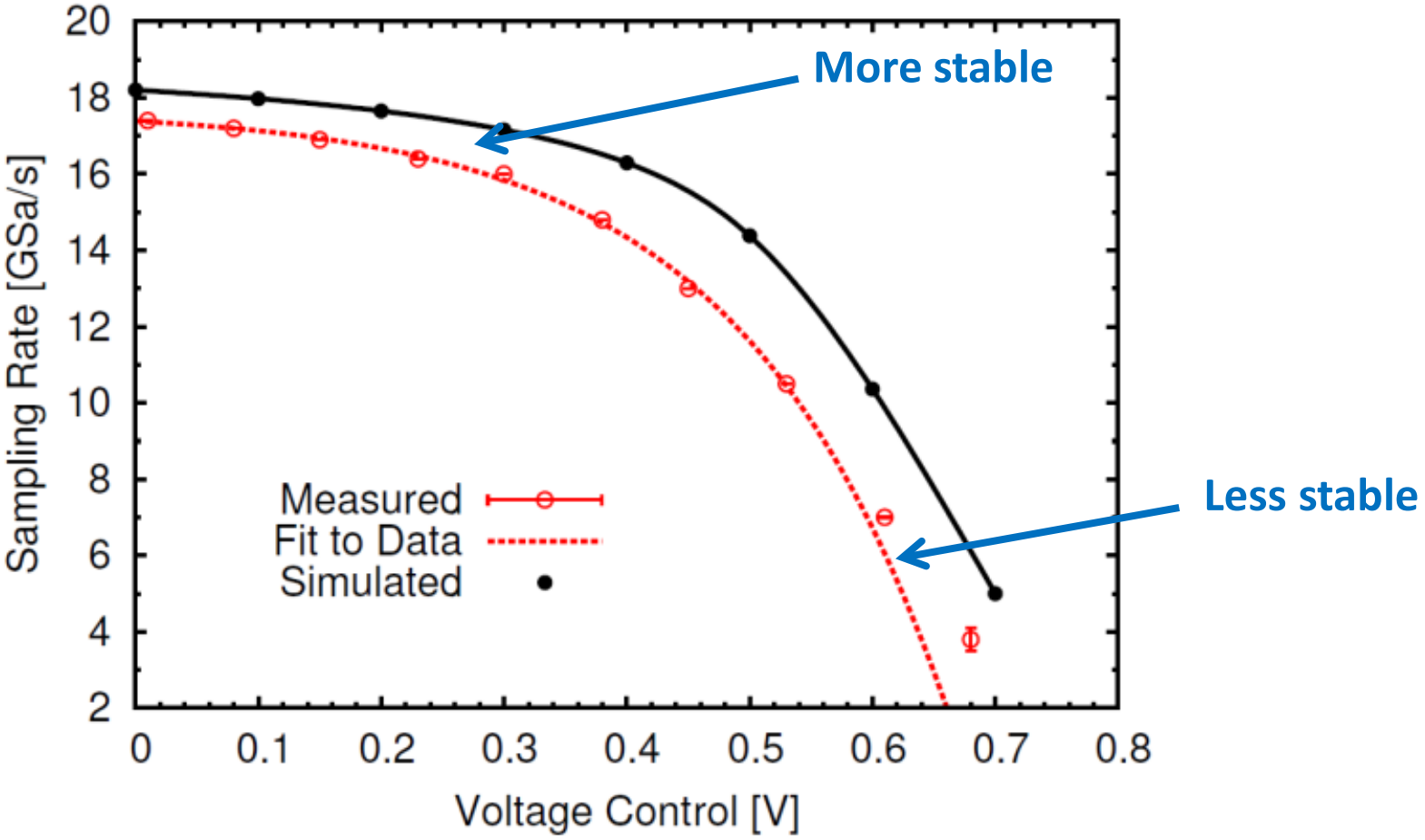
PSEC4 : 0.13 µm CMOS

- 10-15 GSa/s Switched Capacitor Array (SCA) sampling
- Up-convert low frequency (~10's MHz) clock to multi-GHz using tapped voltage-controlled delay line (VCDL):



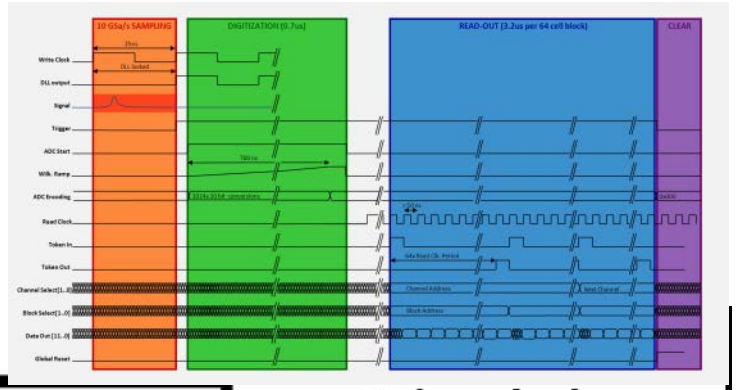
Sampling Rate

- Sampling rate locked on-chip
- ~Small recording window [25 ns when sampling at 10.24 GSa/s]

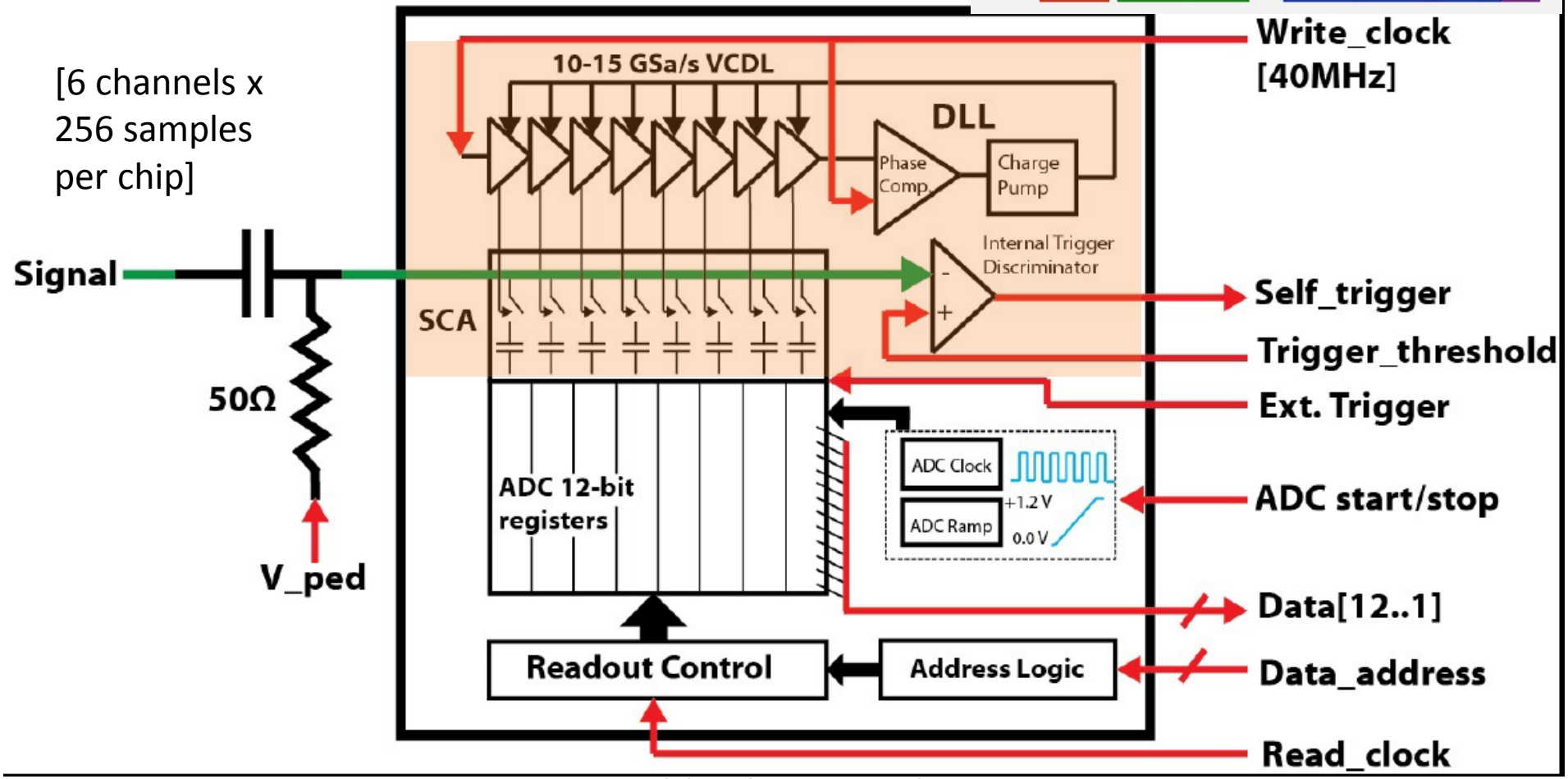


PSEC4 architecture

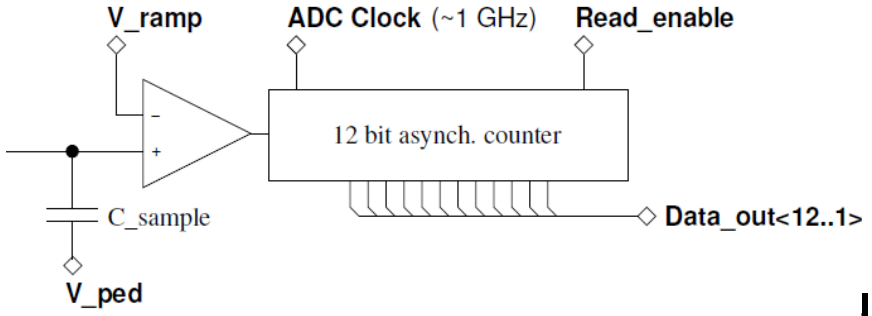
Sampling (continuous)



[6 channels x 256 samples per chip]

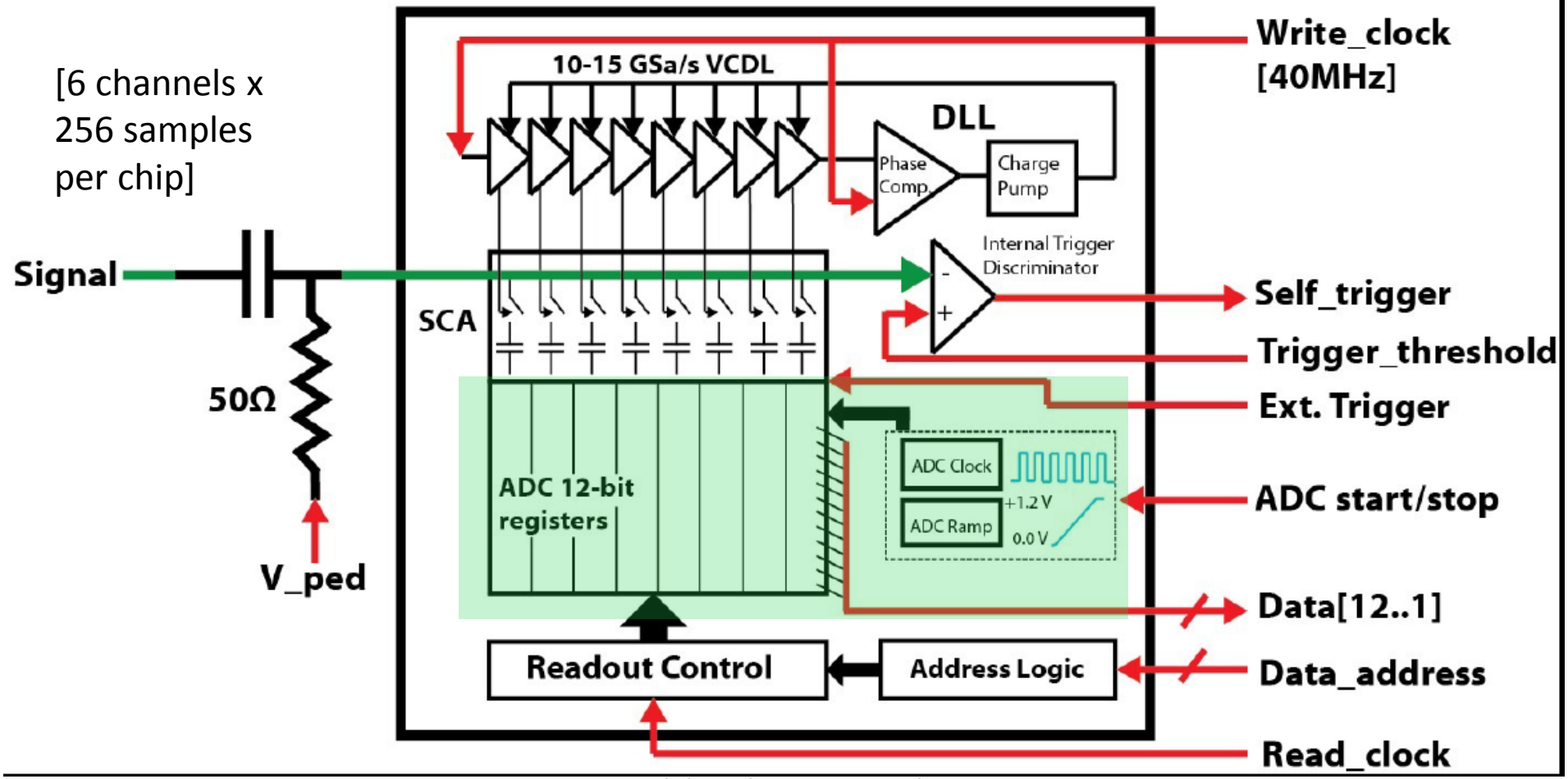


PSEC4 architecture

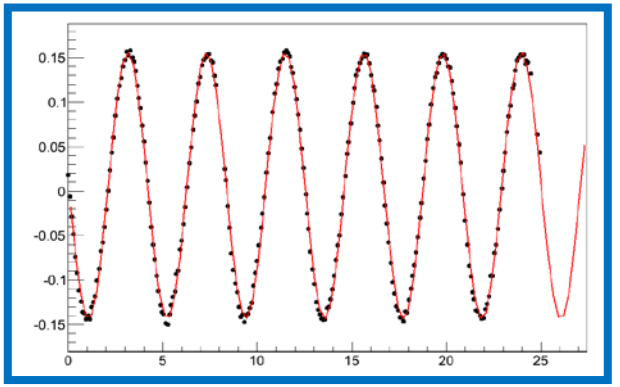


Triggered!
→ Digitization (parallel)

[6 channels x 256 samples per chip]

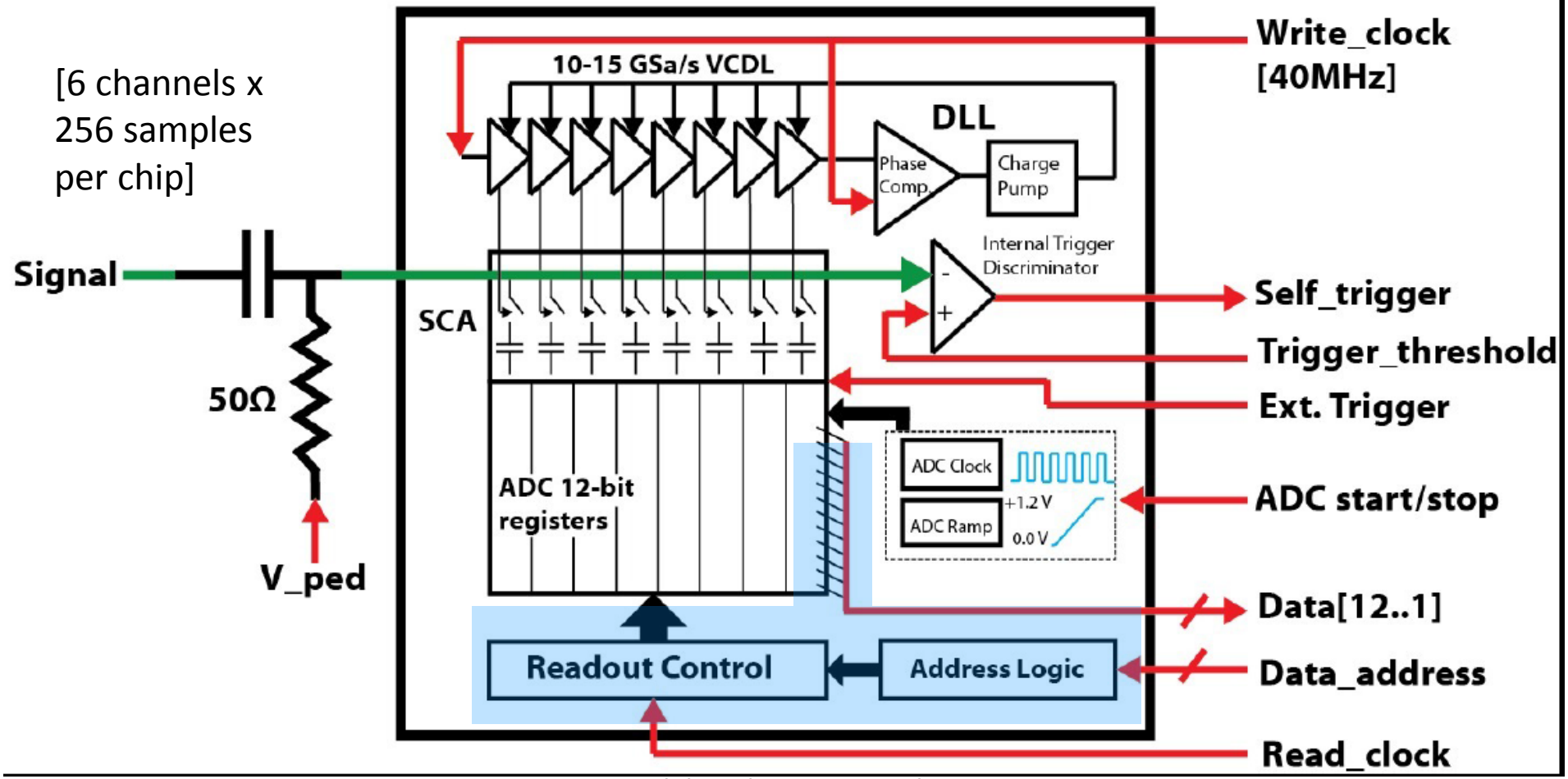


PSEC4 architecture



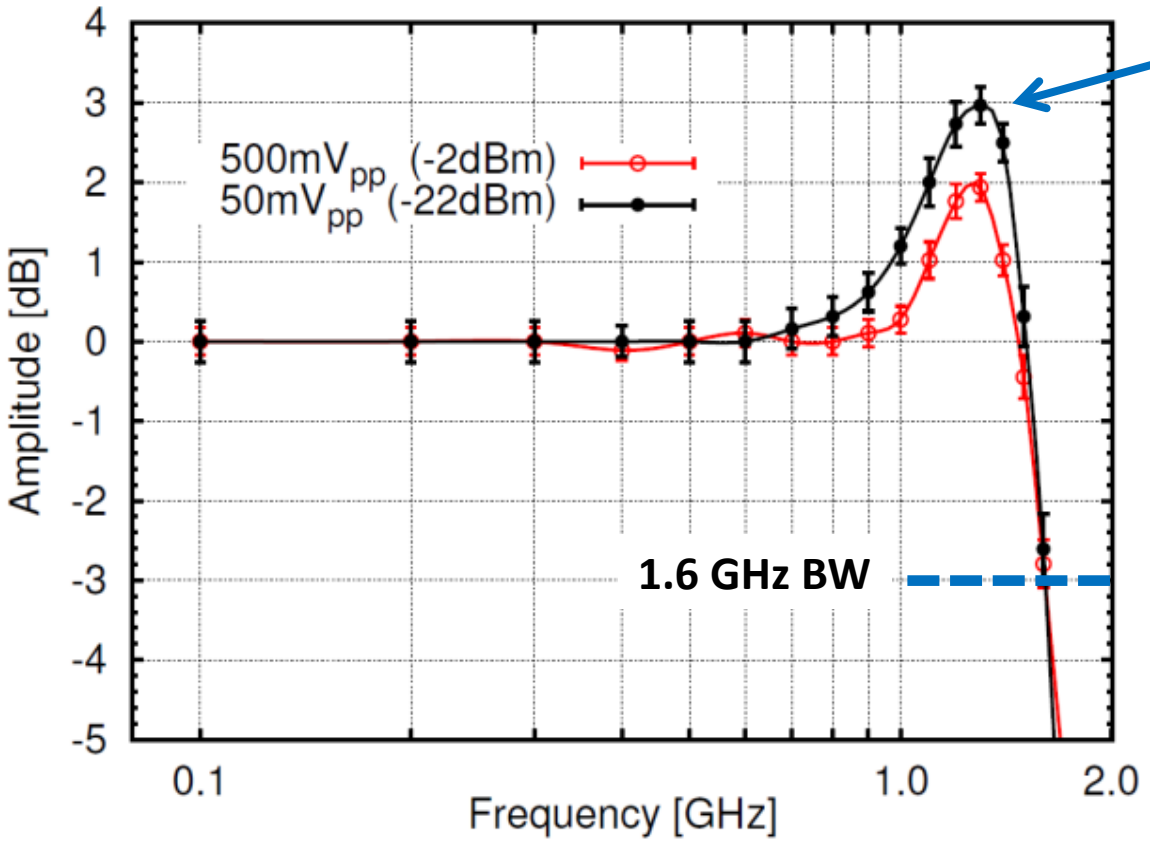
Readout (serial)

[6 channels x 256 samples per chip]



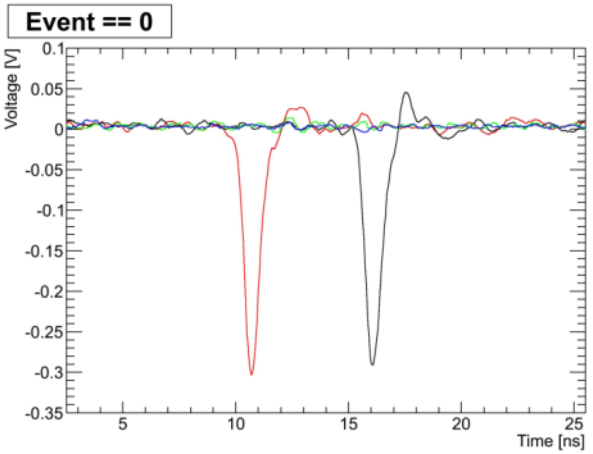
Analog Bandwidth

- Preserve the rise-times of fast (photo)detectors on chip: maximize analog bandwidth



IC Package bondwires' series inductance add resonance in combo with R_{term} + C_{par}

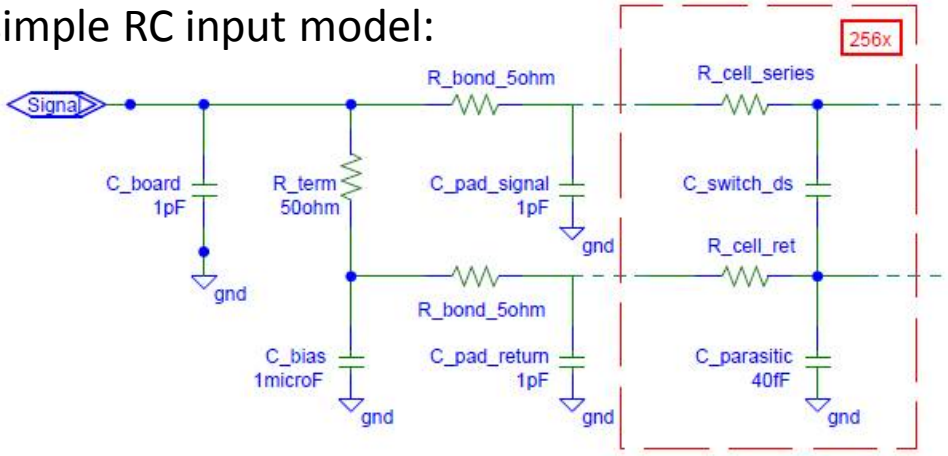
20x20 cm^2 LAPPD MCP pulses recorded by PSEC4 (≤ 1 ns FWHM):



Analog Bandwidth + xtalk

- Bandwidth limited by parasitic input capacitance (C_{in}), which drops the input impedance at high frequencies:

simple RC input model:

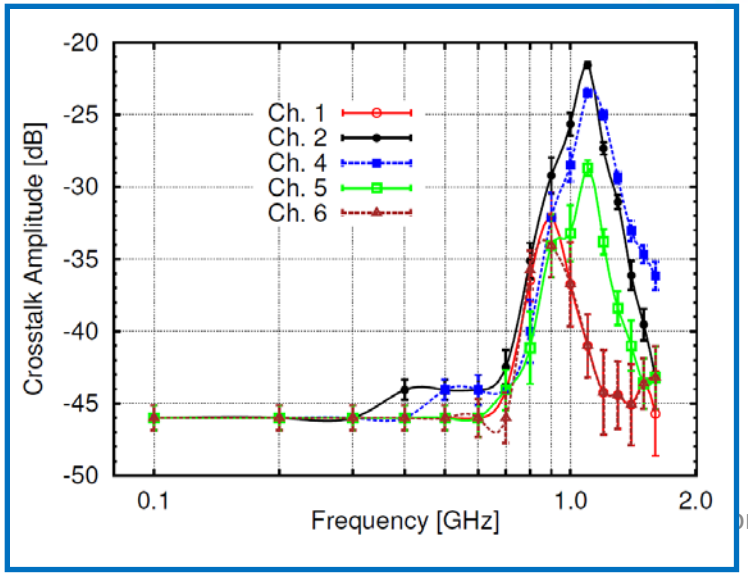


$$|Z_{in}| = \frac{R_{term}}{\sqrt{1+\omega^2\, R_{term}\, C_{in}}}$$

$$f_{3dB} = \frac{1}{2\pi\, R_{term}\, C_{in}}$$

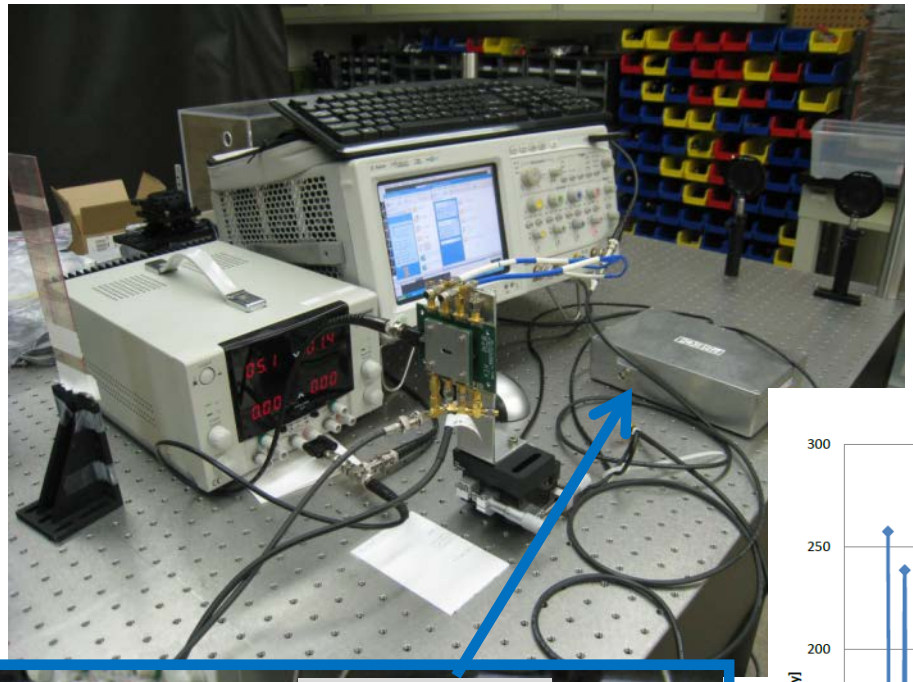
C_{in} ~ 2pF Rterm = 50Ω

bandwidth ~ 1.5 GHz

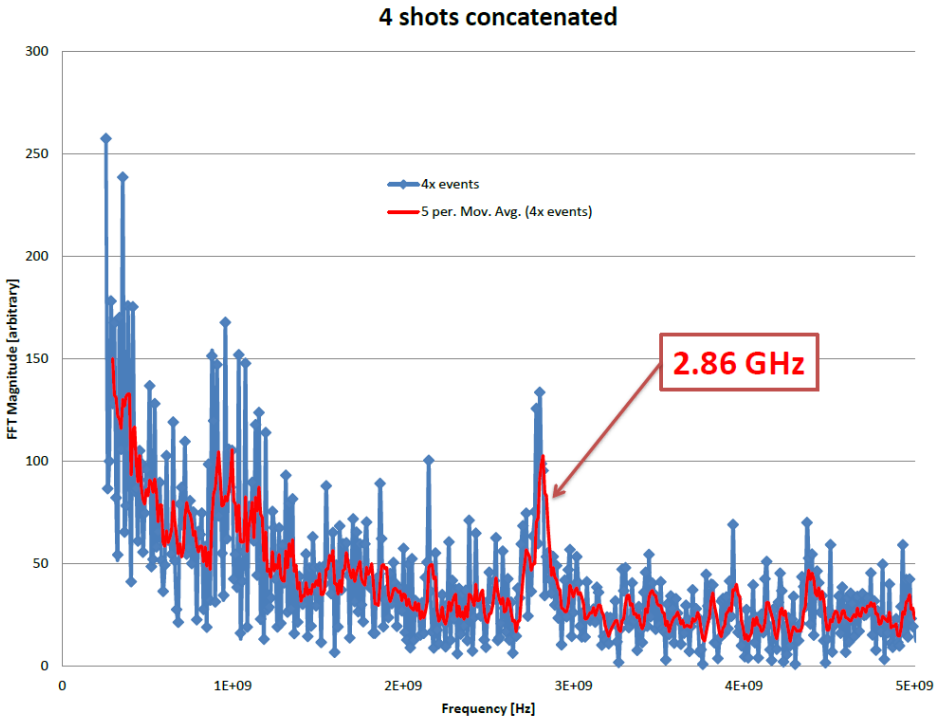


Cross-talk max 7% (!) at 1GHz.
Otherwise <1% for signals <800MHz

Analog Bandwidth

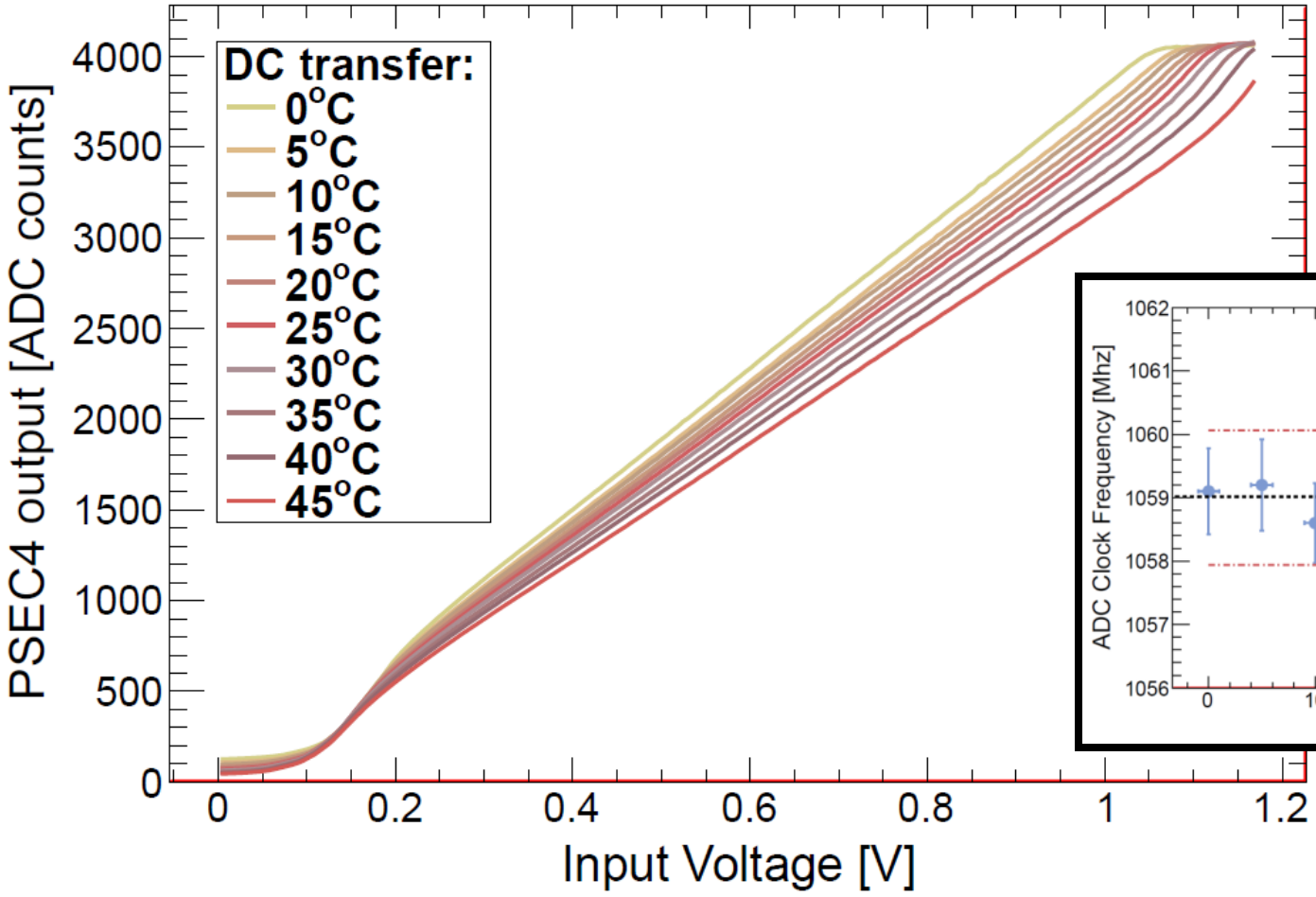


Results taken with the PSEC4:
Tests with a fast, InGaAs detector and 1ps FEL pulses (spaced 350ps apart).
credit: Gary Varner

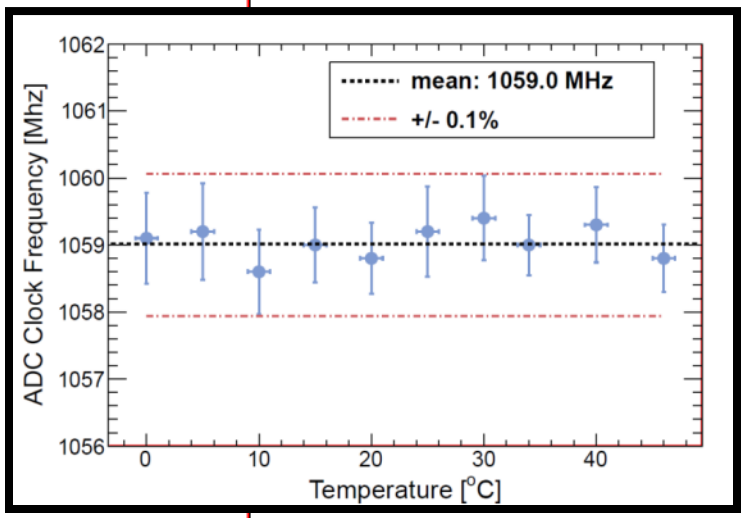


Ramp-compare ADC linearity + stability

- Un-calibrated integral non-linearity 0.15% over 750 mV range
- Full 1 V signal voltage range after calibration (DC noise RMS ~0.7 mV)
- Some temperature dependence observed:

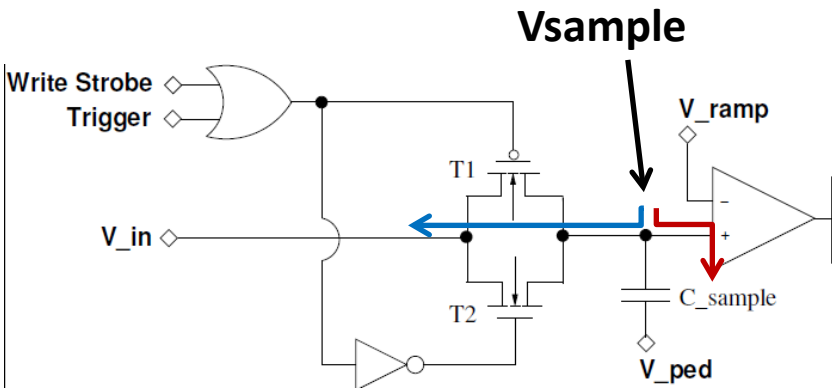


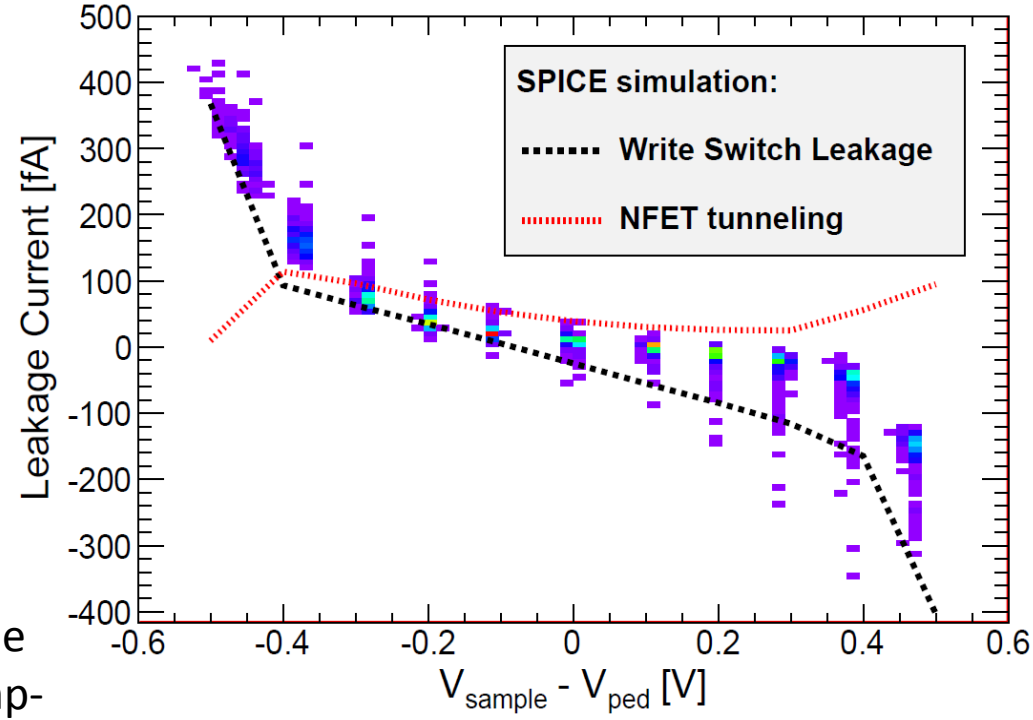
ADC clock rate kept stable to 0.1% over temperature using FPGA servo control:



Sample Leakage

- Sub-threshold conduction through write switch (T1/T2)
- Gate-oxide tunneling through NFET at comparator input





-Amplitude dependent!
-PSEC4 only stores analog data on sample capacitor for ~4 µs (max duration of ramp-compare ADC)

Timing calibration

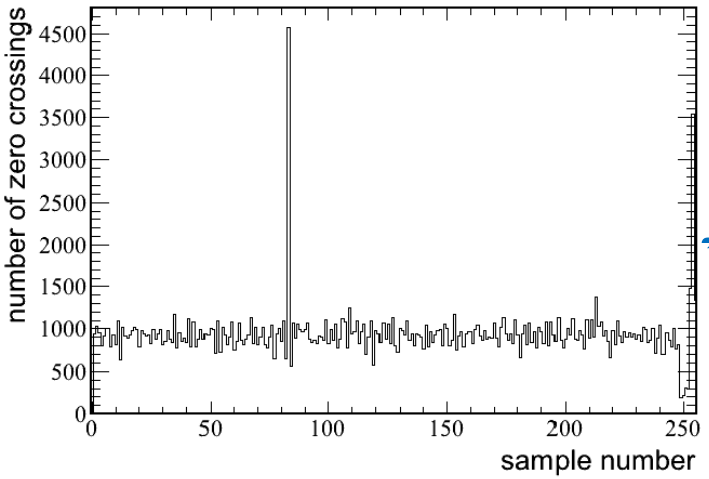
- Overall PSEC4 time-base locked on-chip
- Individual time-steps are not uniform due to process variations
- Employ a 'brute force' method for calibrating PSEC4's 256 sample time steps:
  - 1) Record ~100K sine waves with period T_{input}
  - 2) Measure average # of zero crossings per cell
  - 3) With enough statistics, can extract Δt for each time-step:

$$\langle \Delta t \rangle = T_{input} * \langle N_{zero} \rangle / (2 * N_{events})$$

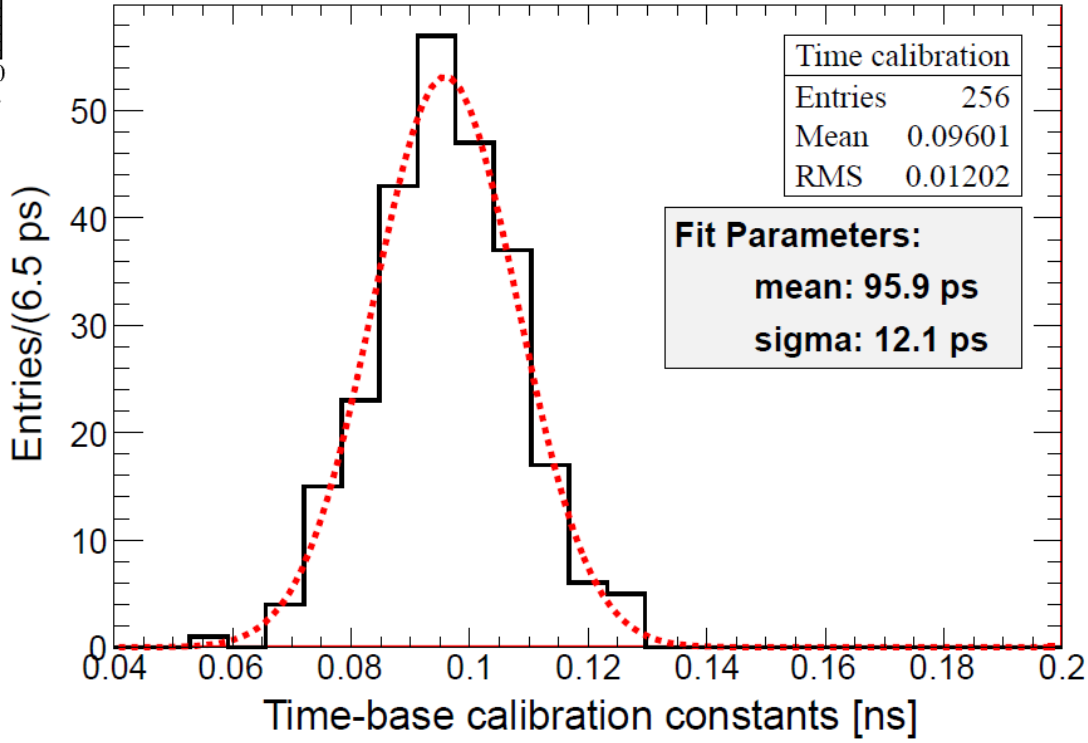
Also, a novel method that didn't quite work for PSEC4:

K. Nishimura, A. Romero-Wolf, "A Correlation-Based Timing Calibration & Diagnostic Technique for Fast Digitization ASICs", Physics Procedia 37 (2012) 1707-1714.

Timing calibration : example



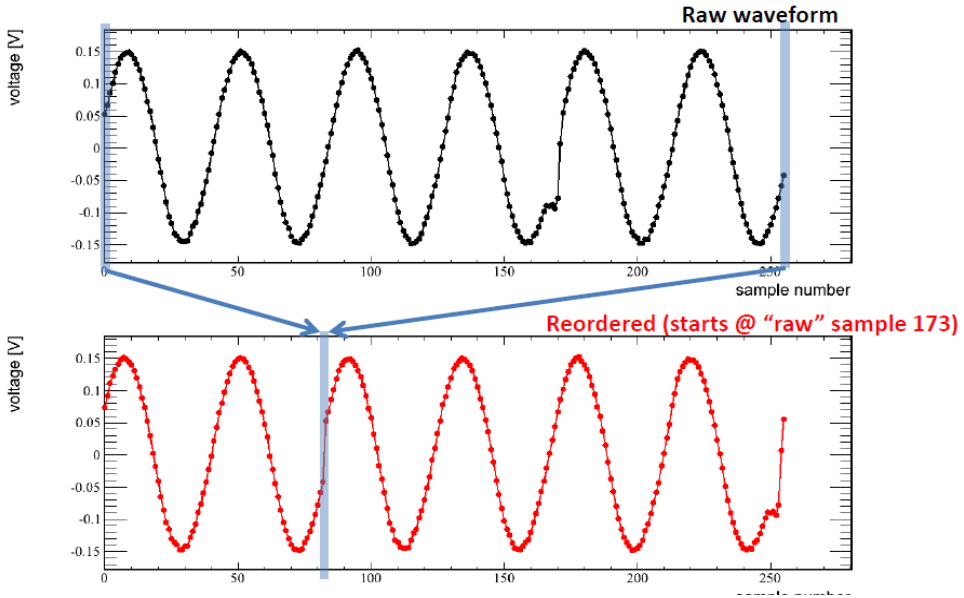
- PSEC4 running at 10.24 GSa/s
- 240 MHz calibration sine

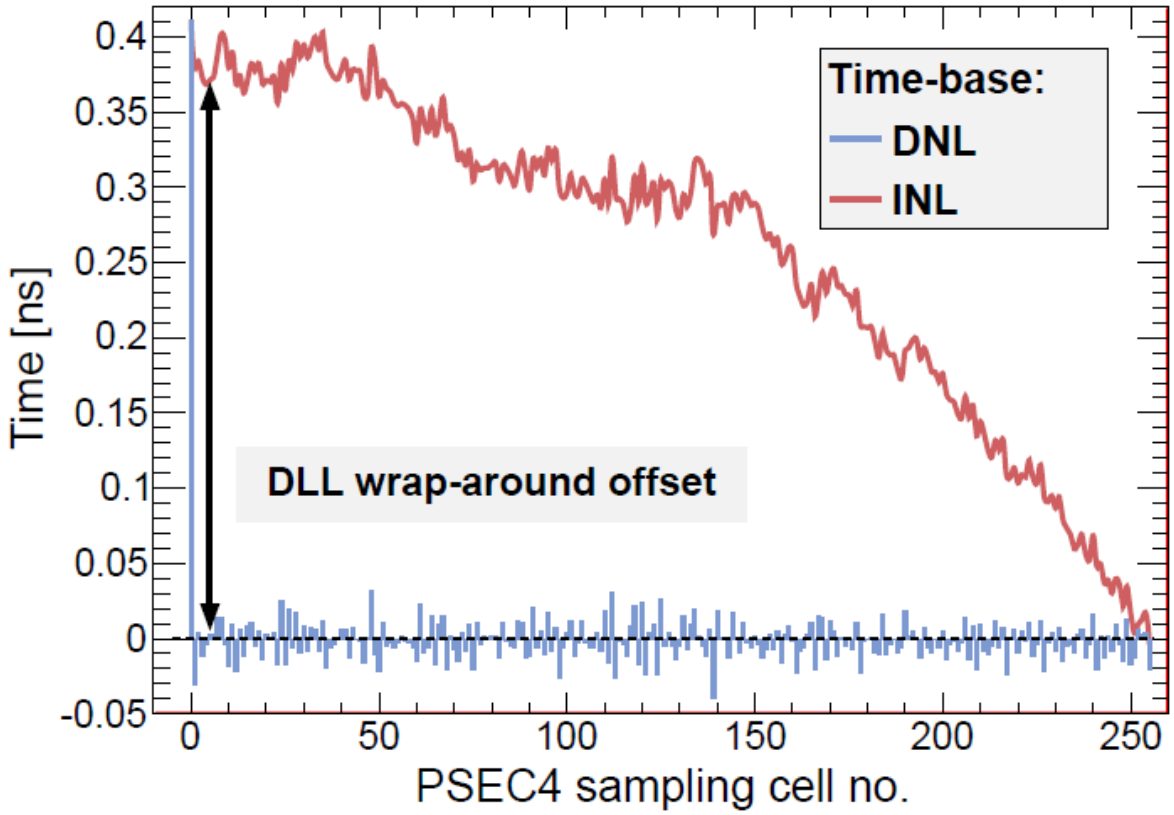


- 13% spread in Δt's
- Calibrations required for each channel (some interesting correlations observed…though not particularly useful)

Timebase DNL/INL

- PSEC4 ‘wraparound’ feature causes first time step to be ~400 ps

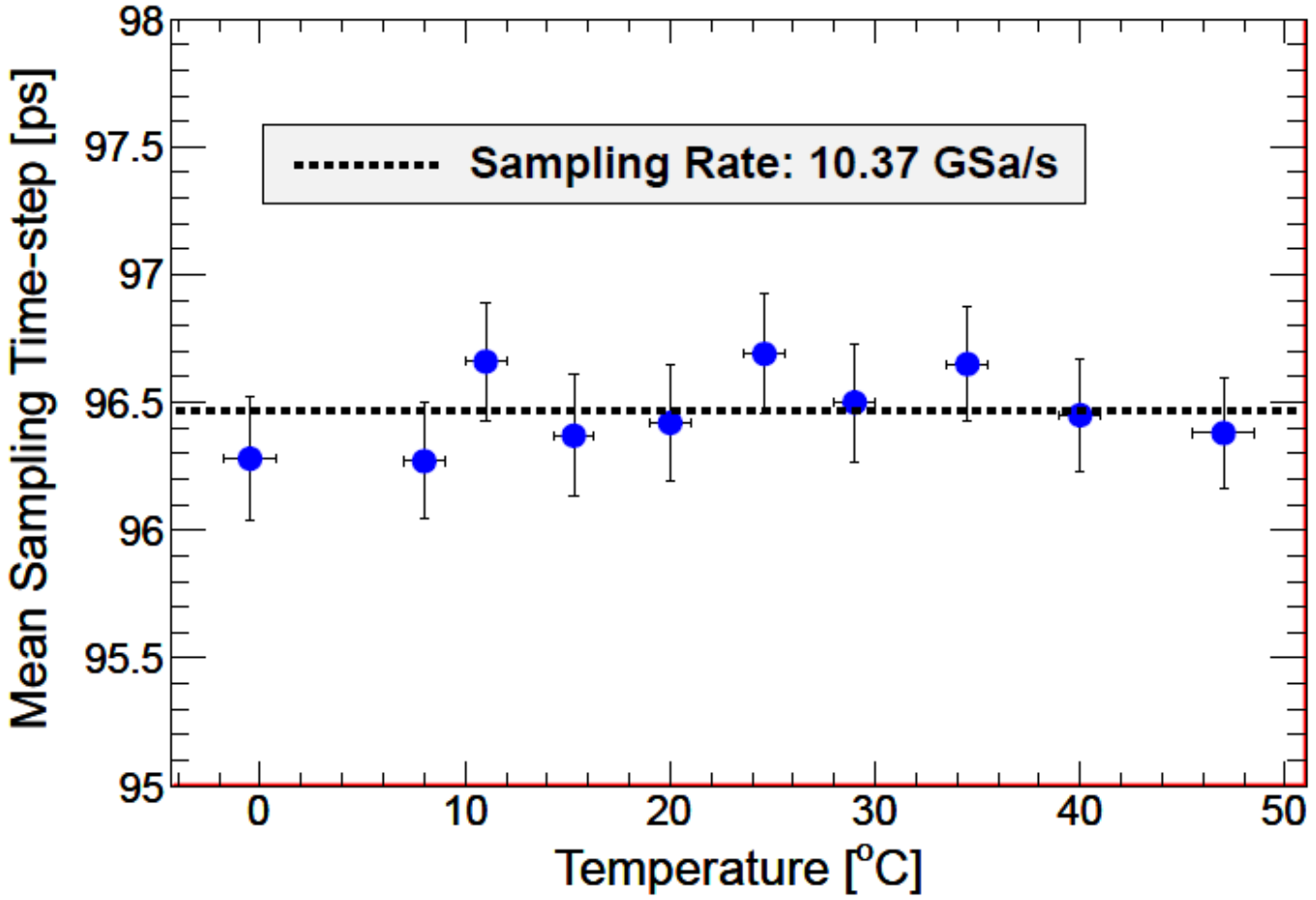




- known gap at wraparound point between samples 255 and 0
- necessary to reorder waveforms

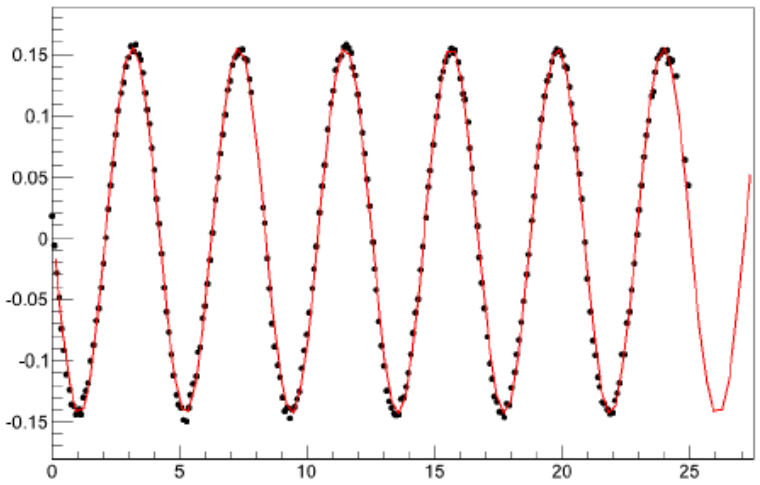
Temperature stability

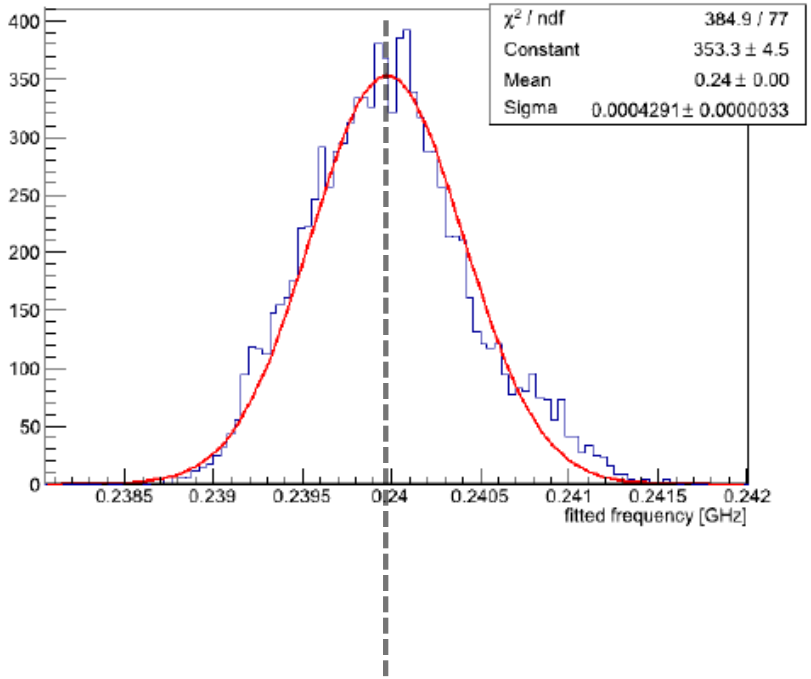
As expected, PSEC4 DLL keeps effective sampling rate fairly stable over temperature

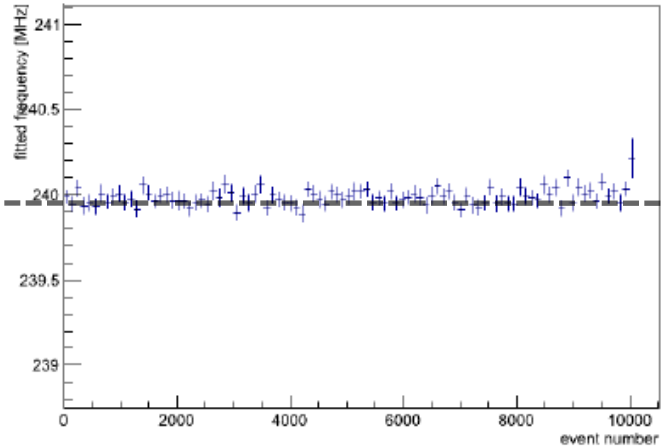


Timing calibration : verification

- (1) fitting for frequency
- Apply Δt values to another 240 MHz data set, fitting sine waves
- Good fit qualities and stable over events



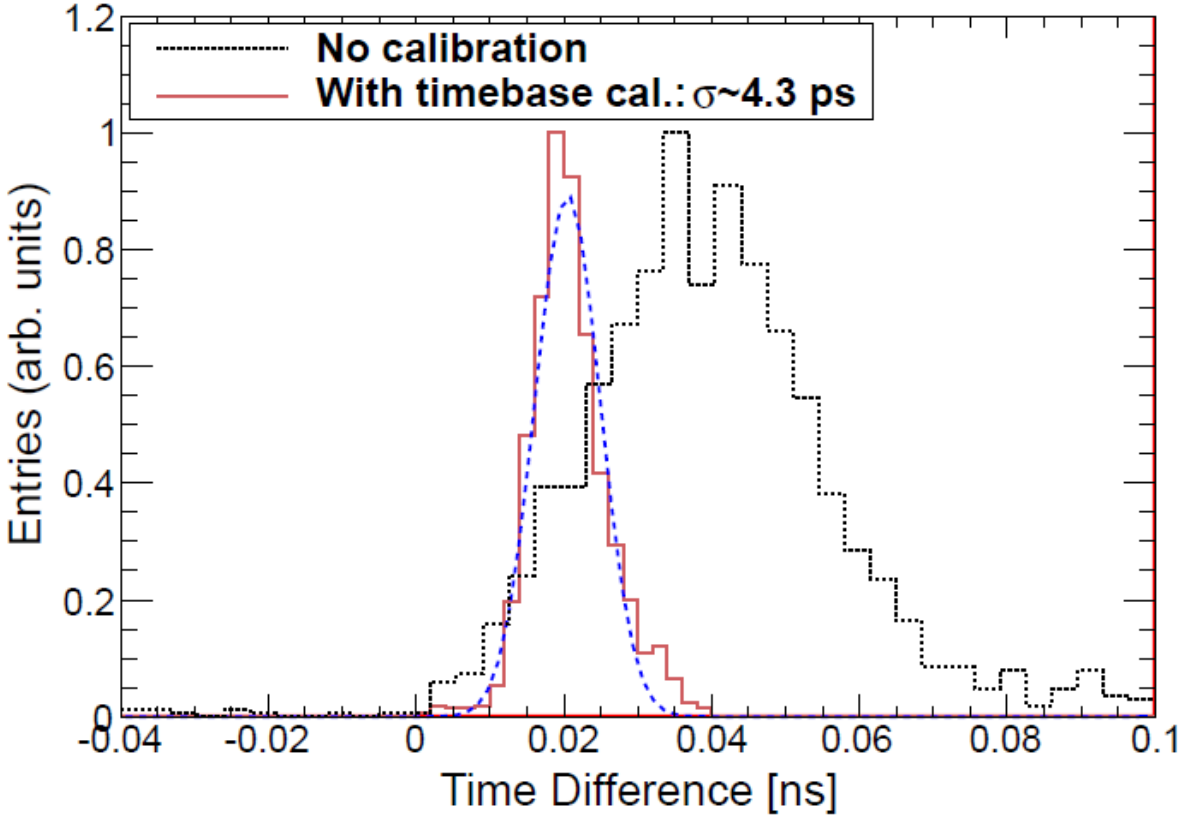




240.0 +/- 0.4 MHz

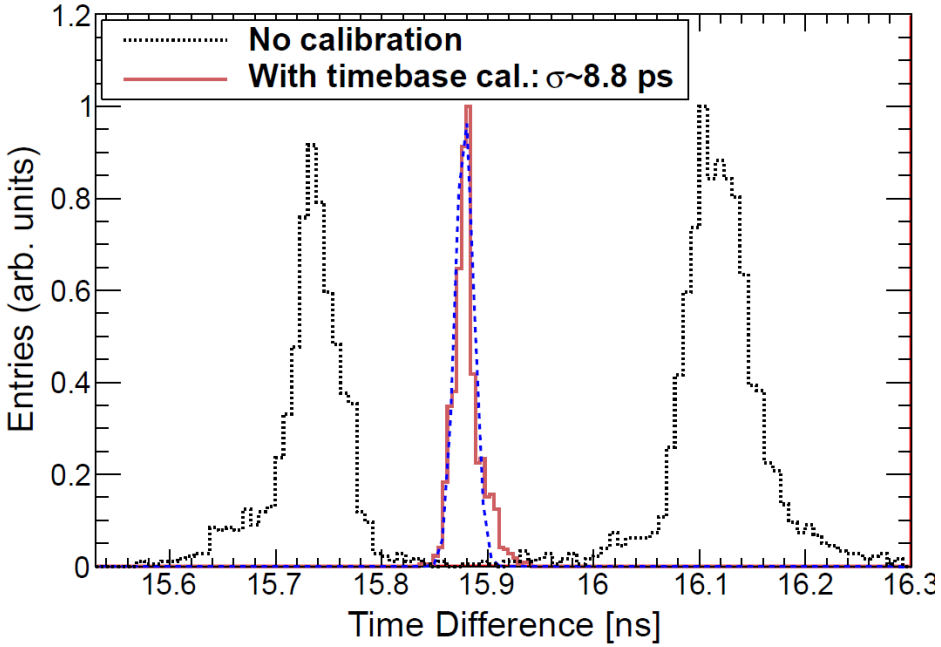
Timing calibration : verification

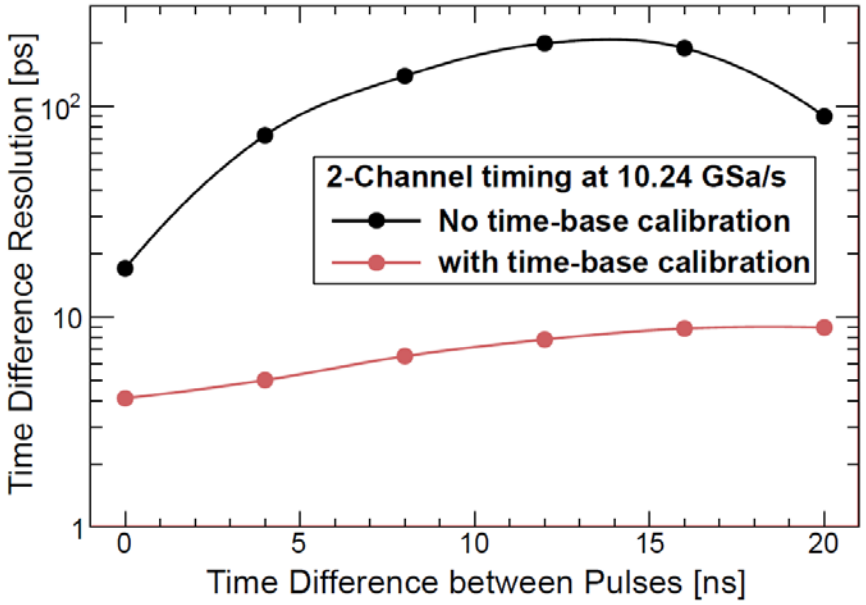
- (2) measure 2-channel timing
- Generate ~2 ns FWHM Gaussian pulse, split, and inject into 2 channels of PSEC4
- Apply voltage and time calibrations. Fit pulse rising edge (~10 points) and extract time difference. No other data processing



Timing calibration : verification

- (2) measure 2-channel timing
- Apply voltage and time calibrations. Fit pulse rising edge (~10 points) and extract time difference. No other data processing
- Measuring timing across PSEC4 recording window. Consistently better than 9 ps.

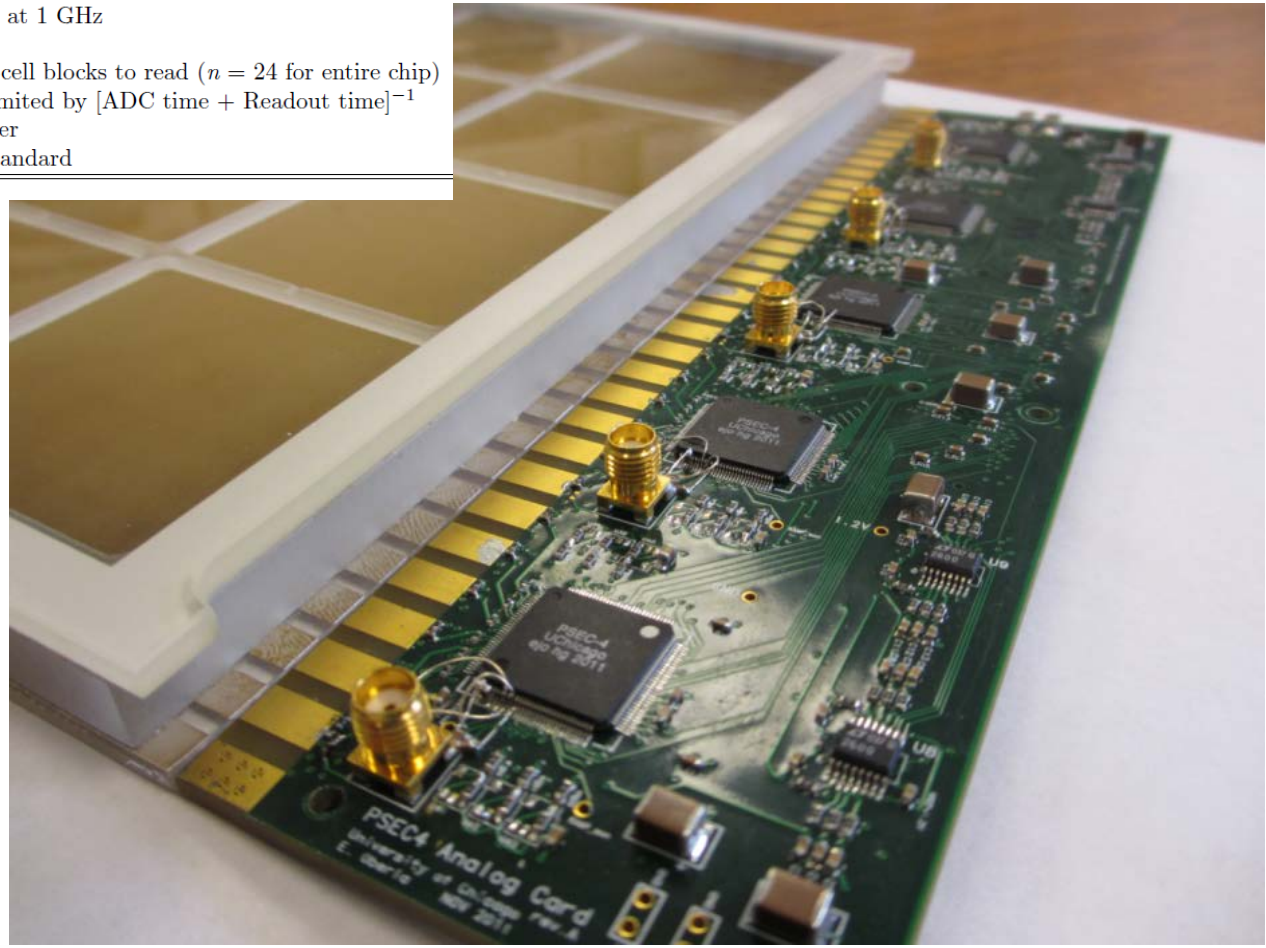




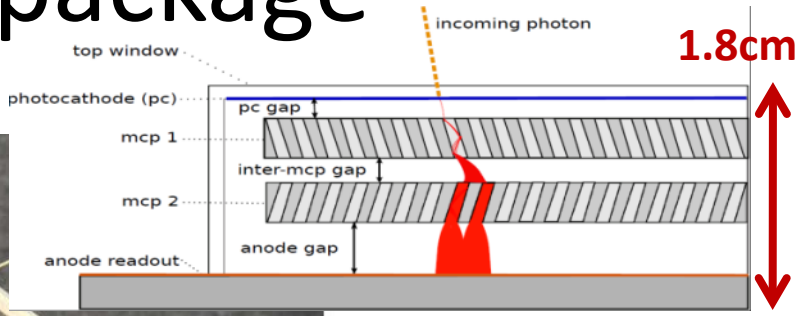
PSEC4-based DAQ

Parameter	Value	Comment
Channels	6	die size constraint
Sampling Rate	4-15 GSa/s	servo-locked on-chip
Samples/channel	256	249 samples effective
Recording Buffer Time	25 ns	at 10.24 GSa/s
Analog Bandwidth	1.5 GHz	
Crosstalk	7%	max. over bandwidth
	<1%	typical for signals <800 MHz
Noise	700 μV	RMS (typical). RF-shielded enclosure. After calibration.
DC RMS Dynamic Range	10.5 bits	12 bits logged. Linearity calibration for each cell.
Signal Voltage Range	1 V	after linearity correction
ADC conversion time	4 μs	max. 12 bits logged at 1 GHz clock speed
	250 ns	min. 8-bits logged at 1 GHz
ADC clock speed	1.4 GHz	max.
Readout time	$0.8n$ μs	n is number of 64-cell blocks to read ($n = 24$ for entire chip)
Sustained Trigger Rate	50 kHz	max. per chip. Limited by [ADC time + Readout time]$^{-1}$
Power Consumption	100 mW	max. average power
Core Voltage	1.2 V	0.13 μm CMOS standard

At the moment: PSEC4 is the baseline readout ASIC for the glass package LAPPD MCP



LAPPD 400 cm^2 glass package



Top Window

MCPs

Grid spacers

Anode microstrips

The Frugal Tile

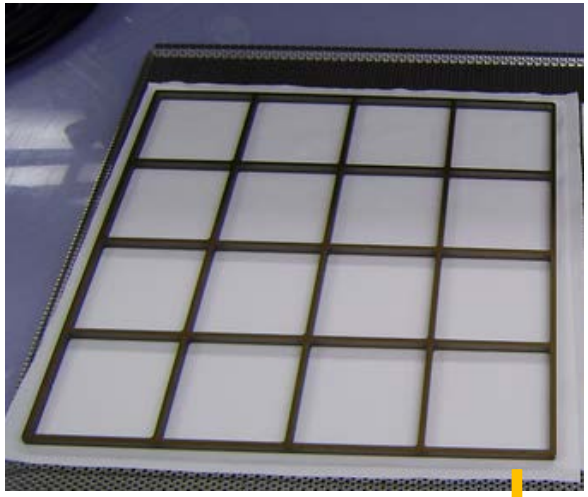
Ground Plane

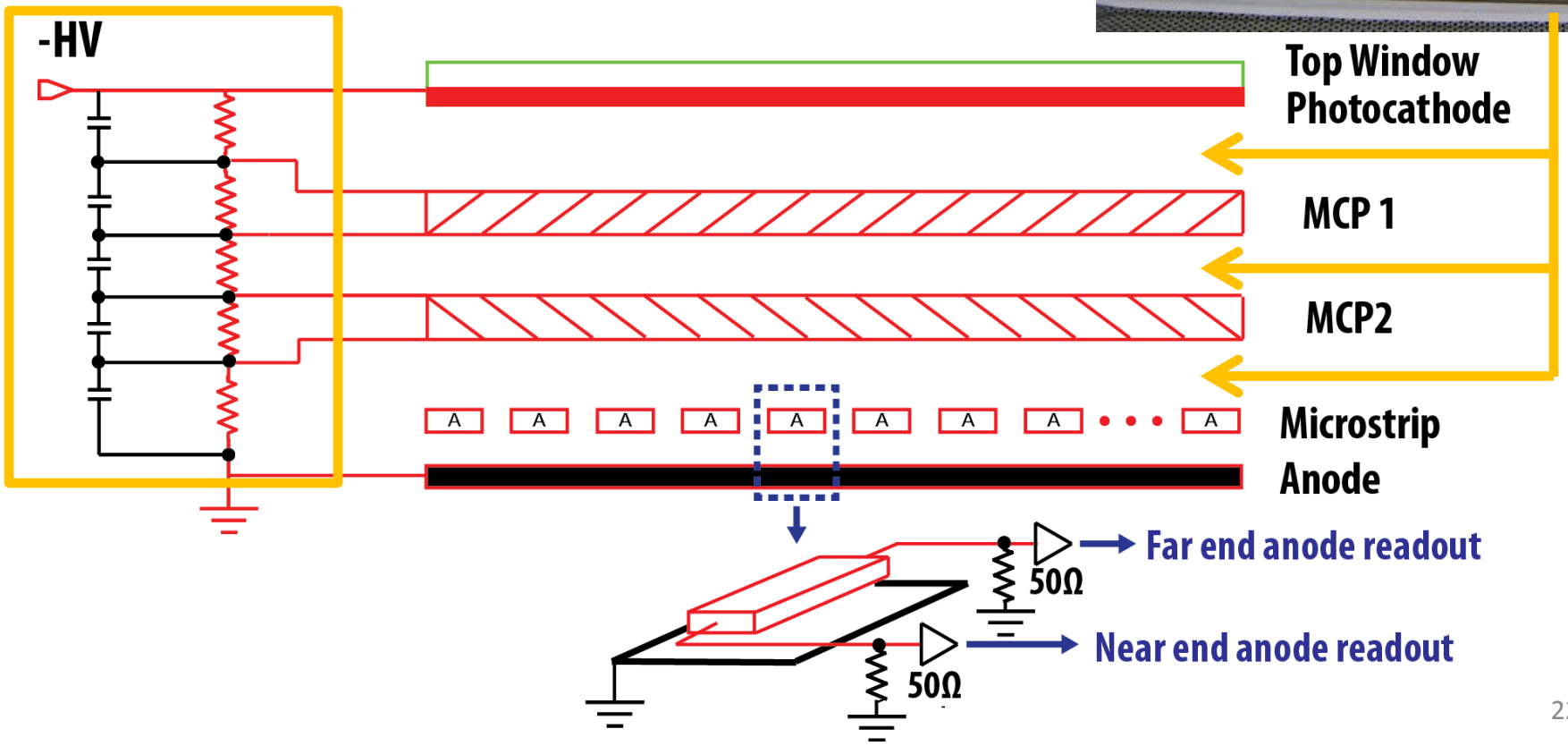
Readout Electronics

The Frugal Tile - Detector Assembly

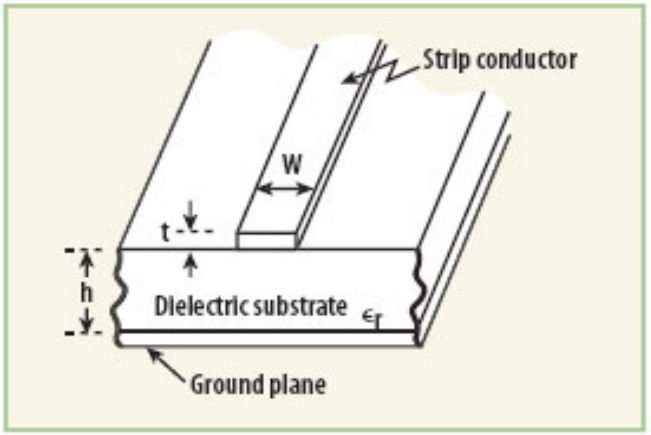
The 400 cm^2 glass package: **HV distribution**

High Voltage distribution is embedded in the internal stack-up using ALD grid spacers

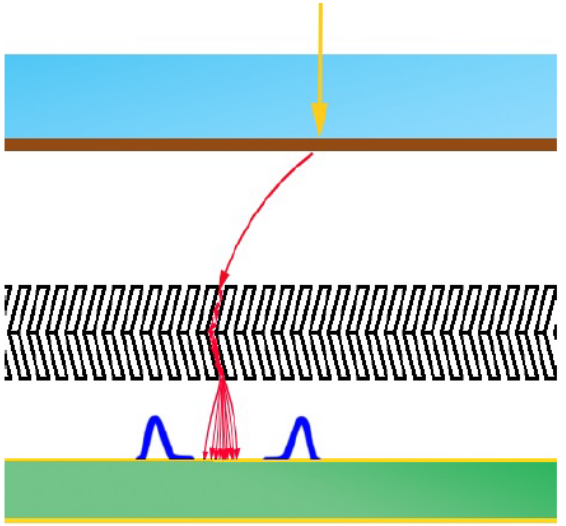




400 cm^2 glass package: Microstrip Anode



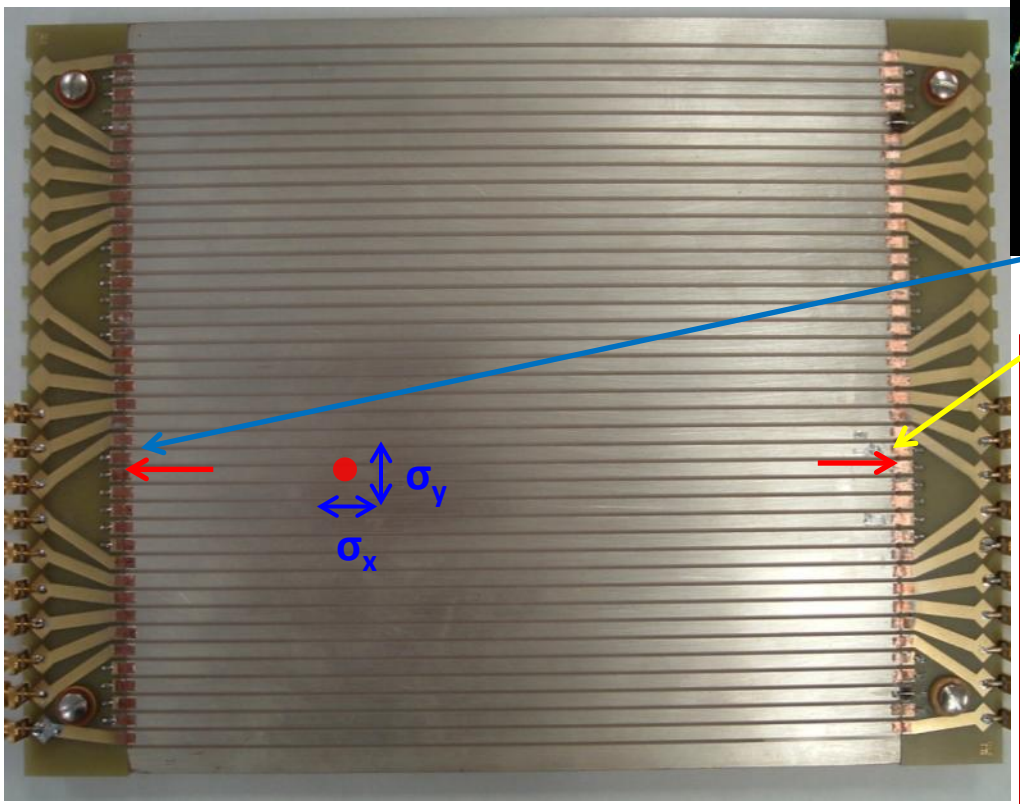
1. Microstrip transmission lines consist of a strip conductor and a ground metal plane separated by a dielectric medium.

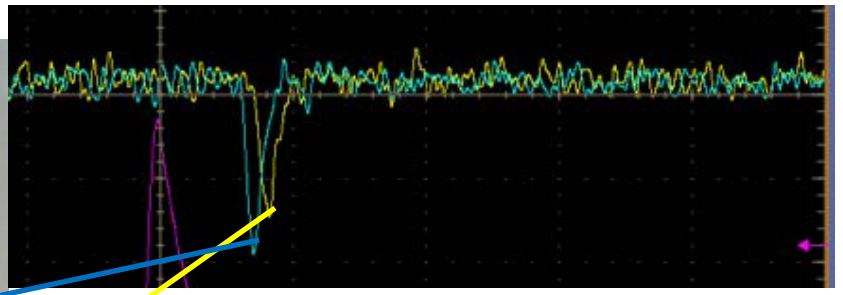


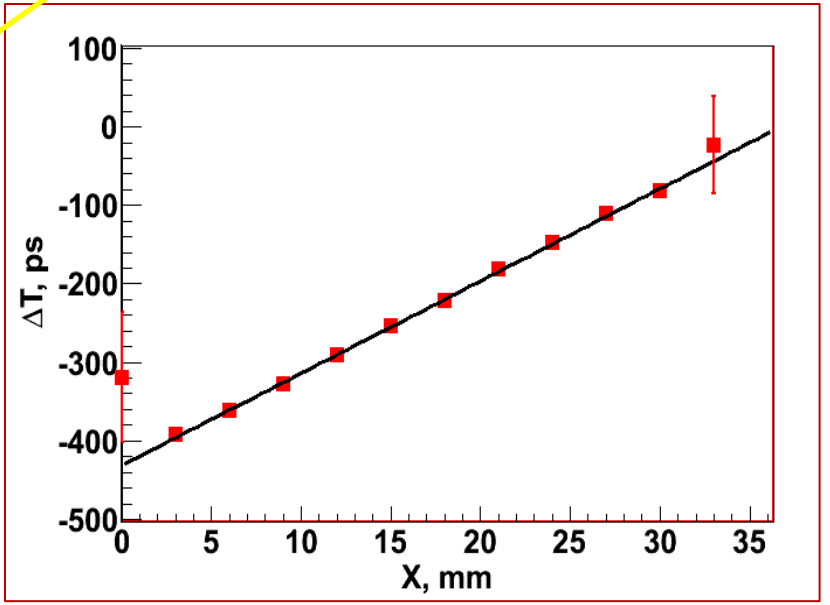
After final amplification, the electron cloud is accelerated towards the anode, inducing EM waves that propagate in both directions along transmission line.

NIMA 711, (2013) 124-131

400 cm^2 glass package: Microstrip Anode







- Location of event (x,y) determined by the time difference of signal on two ends (x) and the charge-centroid of adjacent strips (y).
- Efficient use of electronics channels.

33mm MCP position scan:
V_{prop} ~ 2/3c along stripline

PSEC4 DAQ Block Diagram

1 Central, 6 Front End (FE) Cards

LVDS Buffer - System Clock

FPGA

Clock

LVDS Buffer

Center Card

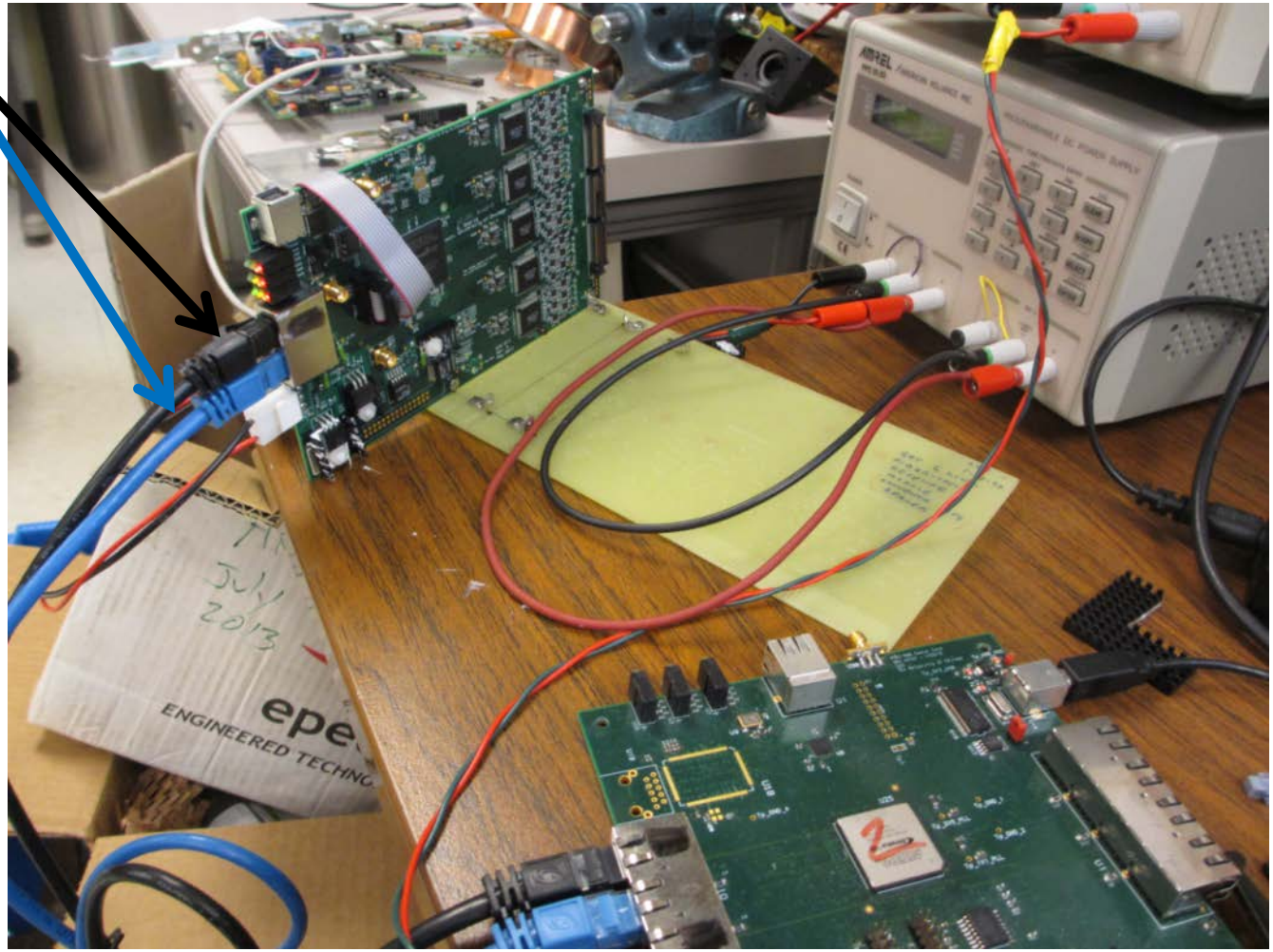
Clock

Detail next slide

PSEC4 DAQ: more detail

Central card <-> Front-end card communication

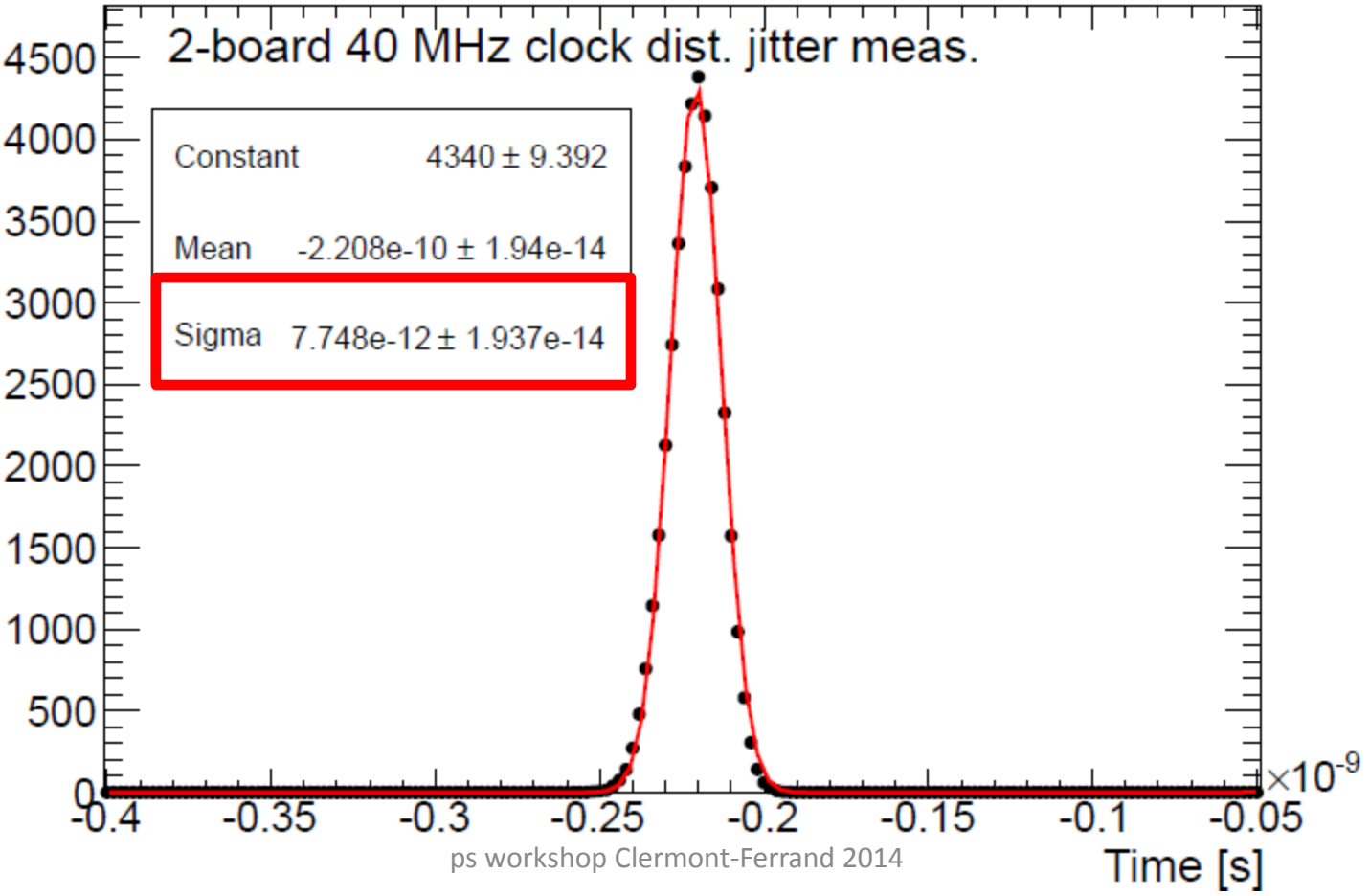
- Eight 800 Mbps LVDS pairs
- Data, clock , trigger, configuration
- Front-end card houses 5 PSEC4 chips (30 channels)
- Each front-end card houses jitter cleaner that cleans system clock and distributes to PSEC4s
- Newest board revision has optional mezzanine plug-in for adding a gain stage



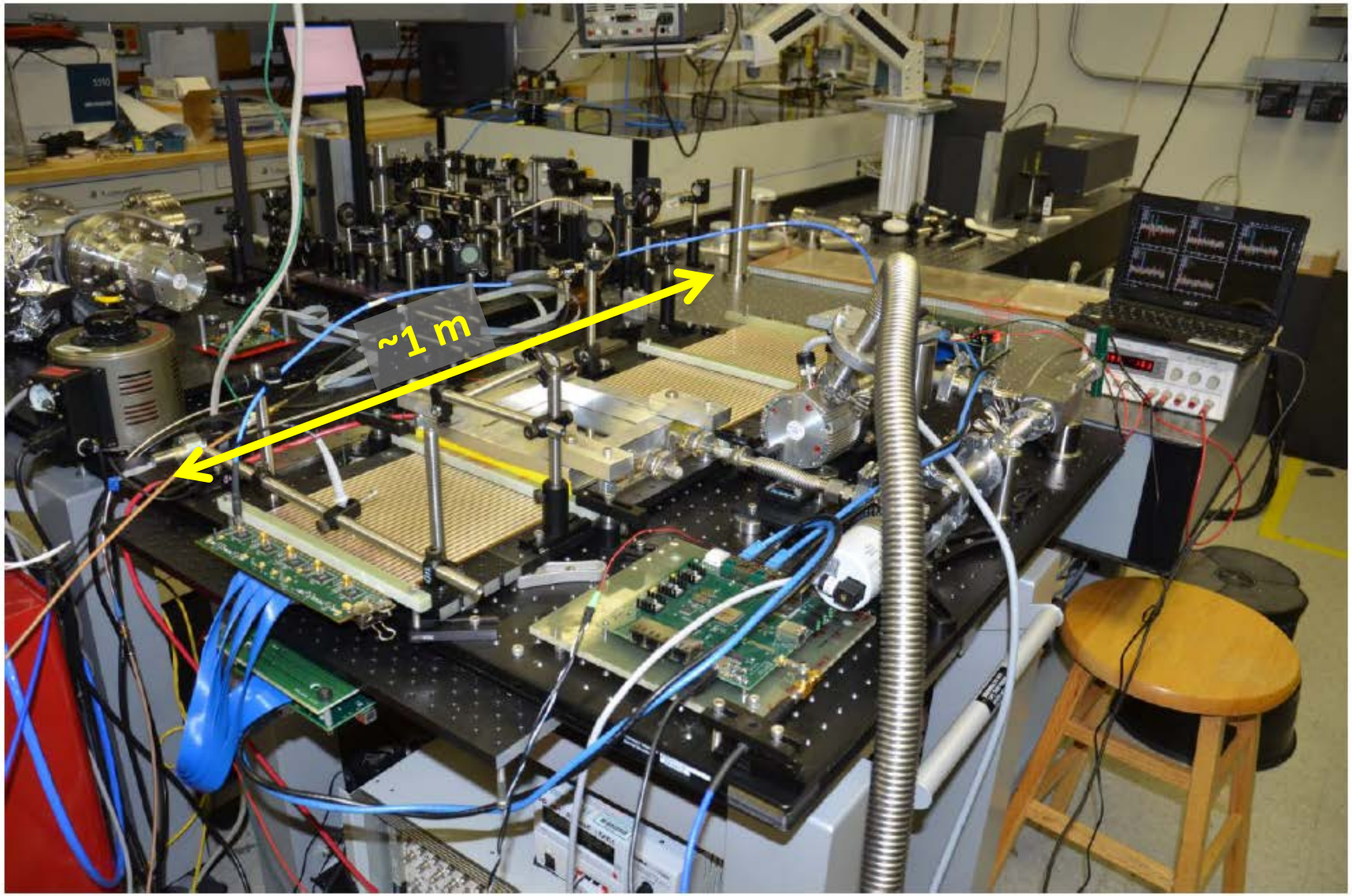
PSEC4 DAQ: more detail

Clock syncing between front-end boards

- Crucial system parameter: chip and system time resolution require precision clock
- ~7-8 ps clock jitter between boards 'out-of-box'
- Still much room to improve performance of jitter cleaner chip (TI CDCE62005)

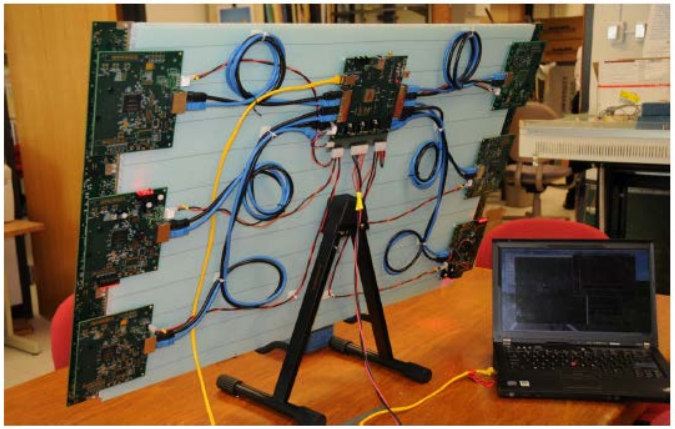


LAPPD Demountable System Testing @ APS



First generation LAPPD glass package readout

- *Fully integrated electronics*

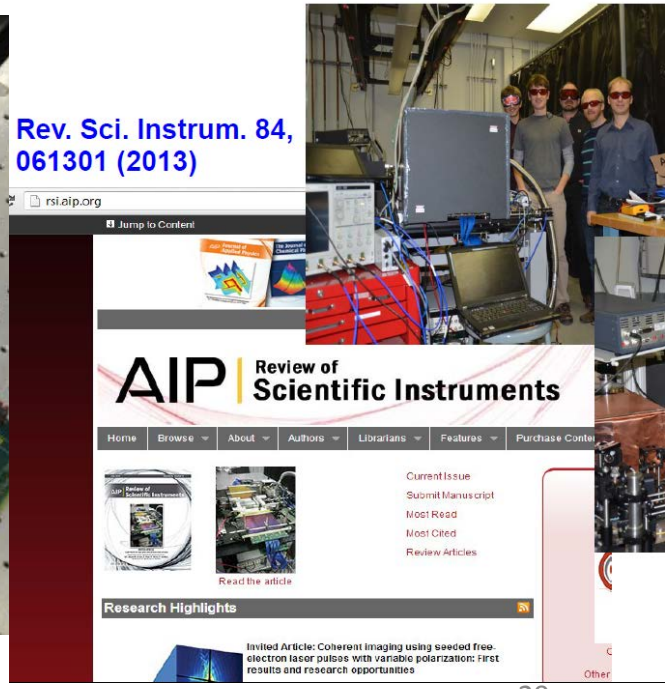


Analog Cards (60 channels PSEC4)

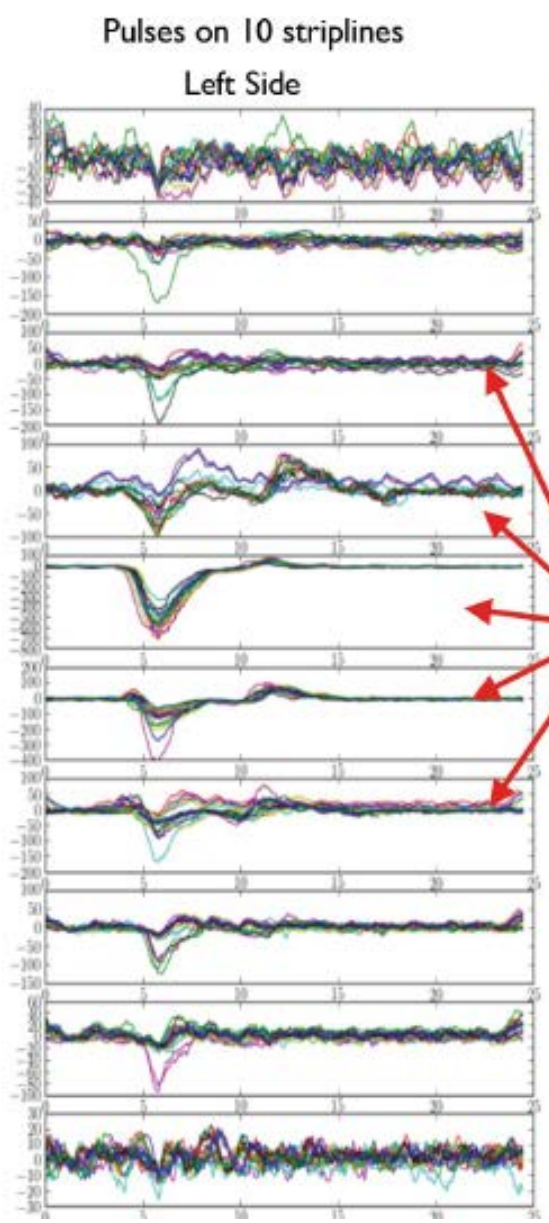
Central Card w/ USB 2.0 or Ethernet

Digital Cards

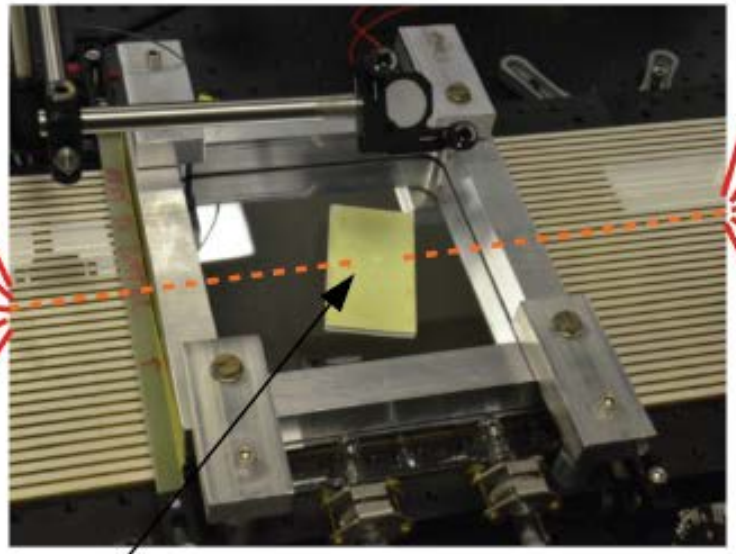
Rev. Sci. Instrum. 84, 061301 (2013)



Position and time reconstruction using PSEC4 pulse recording

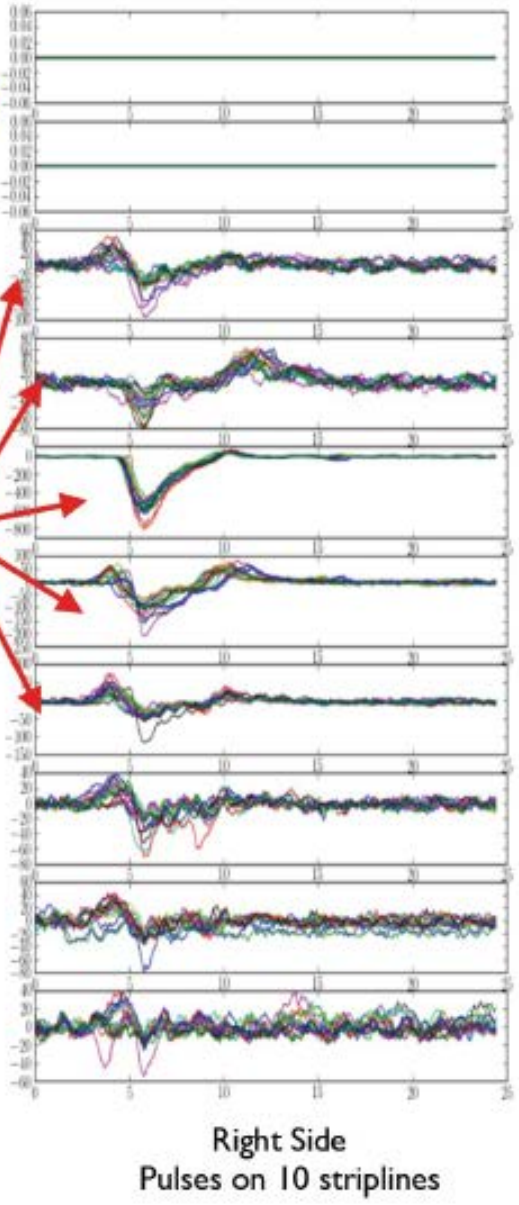


Transverse position is determined by centroid of integrated signal on a cluster of striplines

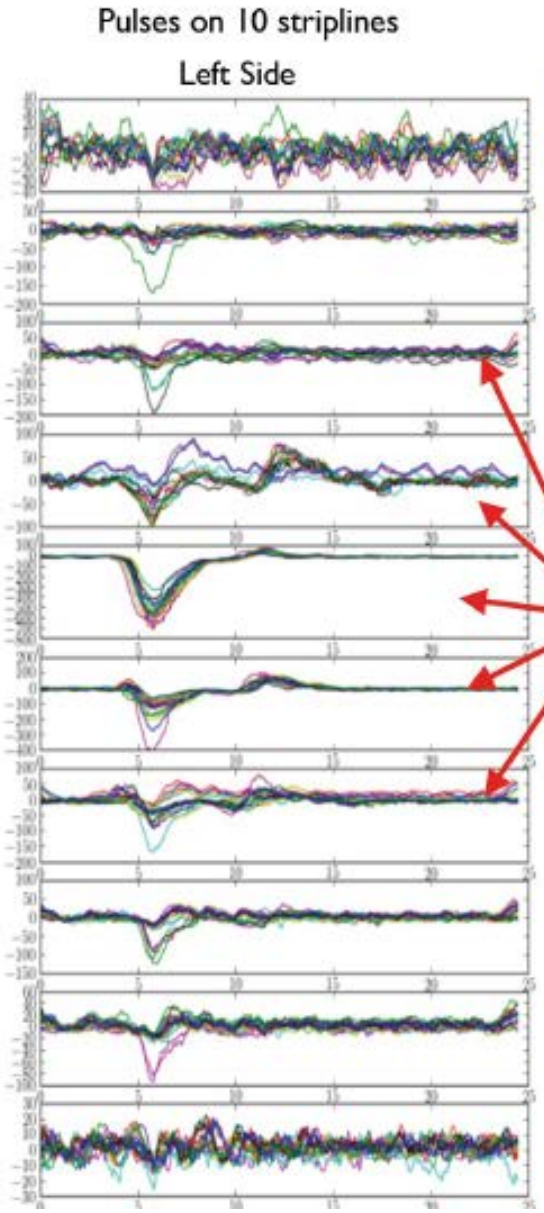


Laser beam spot

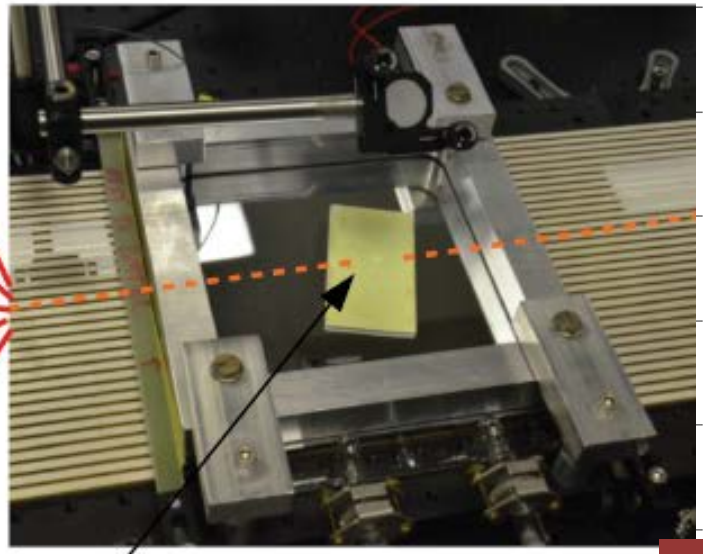
Spatial resolution across the striplines **~0.7mm**



Position and time reconstruction using PSEC4 pulse recording

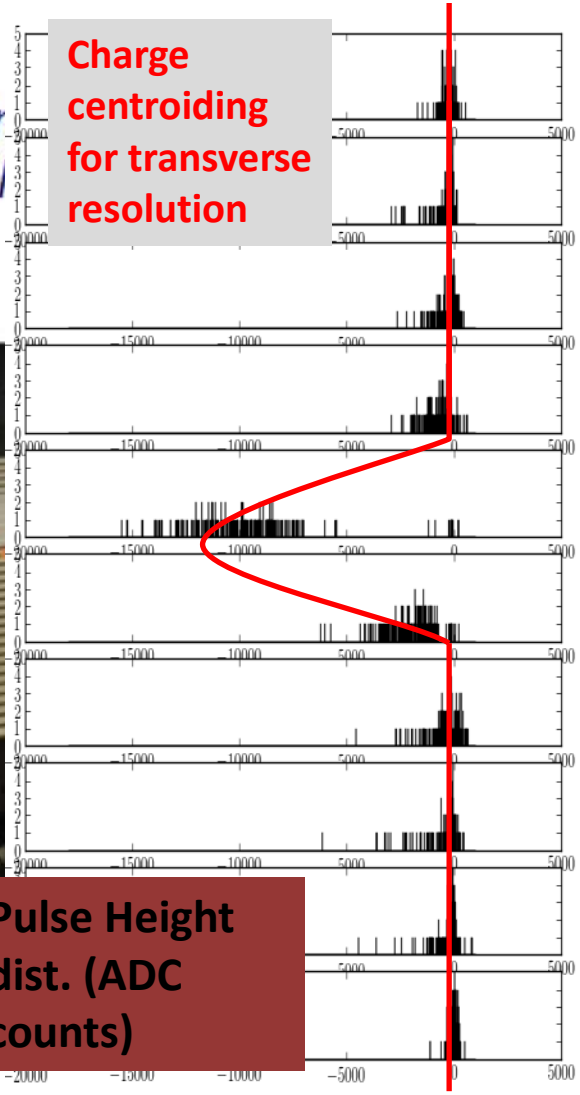


Transverse position is determir
by centroid of integrated signal
on a cluster of striplines



Laser beam spot

Charge centroiding for transverse resolution

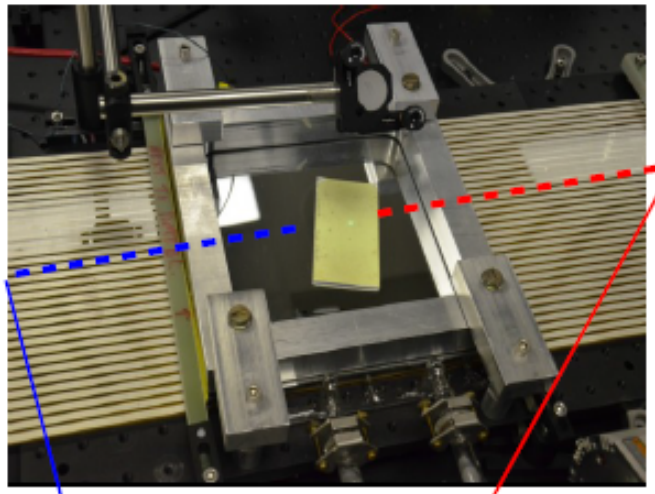


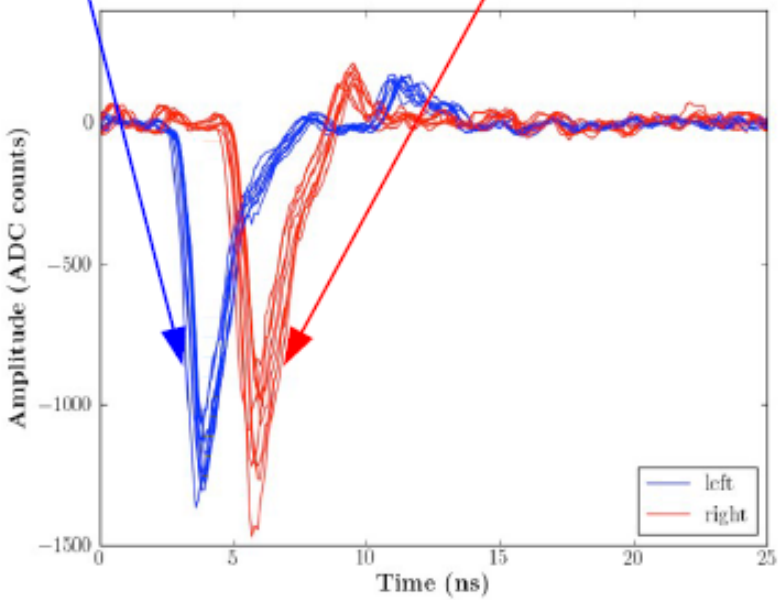
Pulse Height dist. (ADC counts)

Spatial resolution across the striplines **~0.7mm**

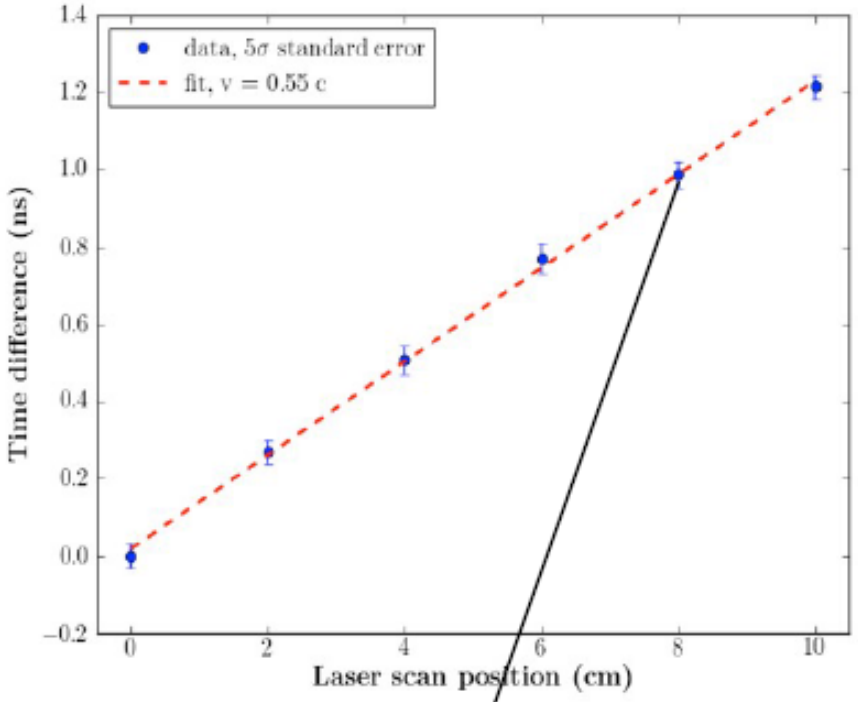
Right Side
Pulses on 10 striplines

Position and time reconstruction using PSEC4 pulse recording





Position in the direction parallel to the striplines is determined by differential transit time to the opposite ends of the anode



4 tiles (90-cm anode): ΔT=~18ps → **ΔX=~1.8mm**

1 tile (20-cm anode): ΔT=~5ps → **ΔX=~0.5mm**

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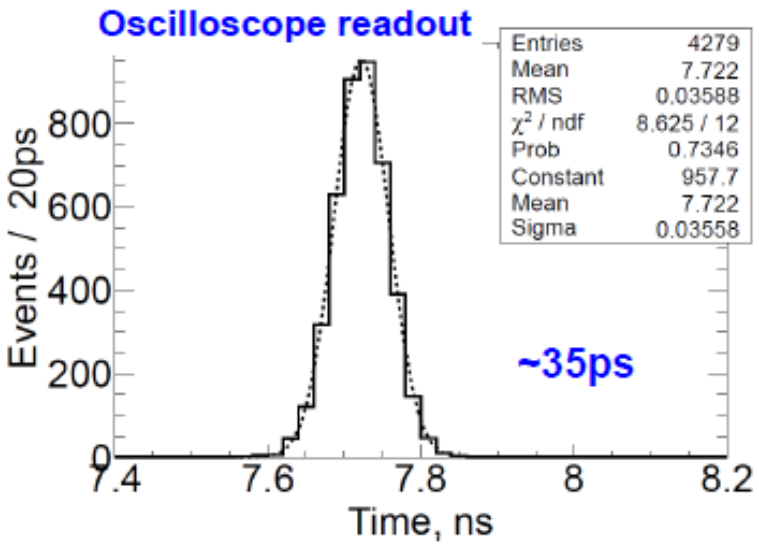
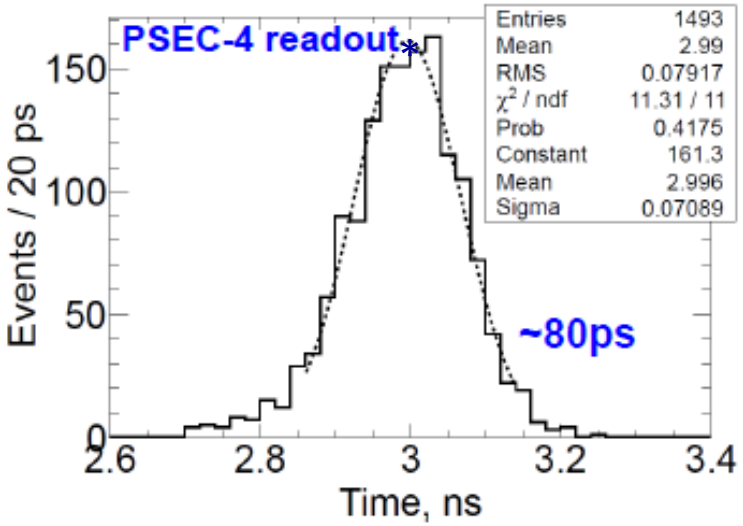
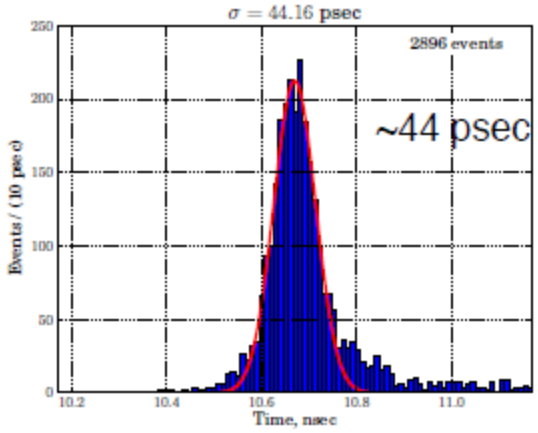
B. Adams, A. Elagin, H. Frisch, R. Obaid, E. Oberla, A. Vostrikov, R. Wagner, M. Wetstein, "Measurements of the Gain, Time Resolution, and Spatial Resolution of a 20x20 cm^2 MCP-based Picosecond Photo-Detector", Nucl. Instr. Meth. A (2013), http://dx.doi.org/10.1016/j.nima.2013.07.091.

Time-of-flight resolution

90-cm long anode!







Single photon Gain~2e7

*using first generation readout board. Newer boards fix some stability issues = better timing

Lastly: PSEC4 → PSEC5

- PSEC5 design (10 Gsa/s & 3.3 microsecond buffer depth) in initial design and simulation stages

Parameter	PSEC4	PSEC5
Channels	6	4
Sampling Rate	4-15 GSa/s	5-15 GSa/s
Primary Samples/channel	256	256
Total Samples/channel	256	32768
Recording Buffer Time at 10 GSa/s	25.6 ns	3.3 μs
Analog Bandwidth	1.5 GHz	1.5 - 2 GHz
RMS Voltage Noise	700 μV	<1 mV
DC RMS Dynamic Range	10.5 bits	10 - 11 bits
Signal Voltage Range	1 V	1 V
ADC on-chip	yes	yes
ADC Clock Speed	1.4 GHz	1.5 - 2 GHz
Readout Protocol	12-bit parallel	serial LVDS: one per channel
Readout Clock Rate	40 MHz	500 MHz
Average Power Consumption	100 mW	300-500 mW
Core Voltage	1.2 V	1.2 V

Add 128x buffer depth