Design of a Deep Buffer for the 0.13um CMOS PSEC5 Waveform Sampling ASIC

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Abstract

We present a design for increasing the buffer length from 25.6ns to 3.3us in a 2-channel prototype of PSEC5, a custom integrated circuit designed for analog-to-digital conversion of fast analog signals at a sampling rate between 5 and 15 Gigasamples/second. The prototype is being designed in the same 0.13um IBM-8RF CMOS process as the PSEC4 ASIC [1]. The major improvements are the increase of the storage buffer from 256 cells to 32,768 cells per channel, allowing a trigger latency of ~3.3us at 10GS/sec, and an increased readout rate. The input signal is continuously sampled into a Primary Array with 256 capacitors which, for a 100ns sampling rate, is rewritten every 25.6ns. The sampling pulses are generated by a Voltage-Controlled Delay Line in 256 stages, run as a Delay-Locked Loop (DLL). The deep Storage Array is organized as two arrays, each 128 capacitors wide by 128 deep. The contents of each half of the Primary Array are transferred into the Storage Array at fixed time intervals in an alternate fashion. The writing and reading of the Storage Array is done with full external control. The design allows uninterrupted writing of the Storage Array after a trigger by selecting a region-of-interest for read-out and temporarily removing it from the recording chain. Depending on the size of the region-of-interest window, the dead time can be greatly reduced or eliminated. The sampled signals are digitized on-chip, and read out serially. The design status and simulation results will be presented.

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References

1. NIM A735, p452; Jan. 2014