Deeper Sampling CMOS Transient Waveform Recording ASICs

The IRS and BLAB3 Deep Storage ASICs for UHE Radio Neutrino and Next Generation Collider Particle Identification

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University of Hawai‘i, and the
Large Area Picosecond PhotoDetector Collaboration

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Why Waveform Sampling?

- Traditional “crate based” electronics
  - Gated Analog-to-Digital Converters
  - Referenced “triggered” Time-to-Digital Converters

- High-rate applications
  - “pipelined operation”
  - Low-speed, low-resolution sampling

- High channel counts
  - Motivation to reduce cabling
  - Integrate electronics onto detector elements

Issues: cost, power, resolution, data volume
Switched Capacitor Array Sampling

- Write pointer is ~few switches closed @ once

Tiny charge: 1mV ~ 100e⁻
“Oscilloscope on a chip”

PMT pulse comparison

- 2 GSa/s, 1GHz ABW Tektronics Scope
- 2.56 GSa/s LAB
Easy access to Waveform sampling

<table>
<thead>
<tr>
<th></th>
<th>WFS ASIC</th>
<th>Commercial</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Sampling speed</strong></td>
<td>0.1-6 GSa/s</td>
<td>3 GSa/s</td>
</tr>
<tr>
<td><strong>Bits/ENOBs</strong></td>
<td>16/9-13+</td>
<td>8/7.4</td>
</tr>
<tr>
<td><strong>Power/Chan.</strong></td>
<td>&lt;= 0.05W</td>
<td>Few W</td>
</tr>
<tr>
<td><strong>Cost/Ch.</strong></td>
<td>&lt; $10 (vol)</td>
<td>&gt; 100$</td>
</tr>
</tbody>
</table>
An Intrinsic Limitation

No power (performance savings) for continuous digitization

We aren’t going to put Analog Devices out of business

“analog down conversion”

→ For most “triggered” ‘event’ applications, not a serious drawback
Gigasamples/s, but Nyquist?

Difficult to couple in Large BW (input C is deadly)

\[ f_{3dB} = \frac{1}{2\pi ZC} \]

- More than 3pF input (ESD protection alone often more) limits ABW < 1GHz
- As a result, first generation WFS ASICs a few hundred to 1k samples (ATWD, SAM, DRS, LABRADOR…)
- Is this an fundamental limitation?
Why Deeper sampling?

Askaryan Radio Array

CLEAN AIR SECTOR

South Pole Operation zone

QUIET CIRCLE

QUIET SECTOR

Runway

Legend:
- Power/comms cable
- Power/comms/calib. station
- Testbed station
- Production Station

10^{18} \, \text{eV} \ \nu_{\mu}

~ 1.33 \, \text{km}

~ \text{km}

primary vertex

secondary showers

~2850 \, \text{mm}

Belle II
Deeper storage: Buffered LABRADOR (BLAB1) ASIC

- Single channel
- 64k samples deep, same SCA technique as LAB, no ripple pointer
- Multi-MSa/s to Multi-GSa/s
- 12-64us to form Global trigger

3mm x 2.8mm, TSMC 0.25um

Arranged as 128 x 512 samples Simultaneous Write/Read
BLAB1 High speed Waveform sampling

- Comparable performance to best CFD + HPTDC
- MUCH lower power, no need for huge cable plant!
- Using full samples reduces the impact of noise
- Photodetector limited

NIM A602 (2009) 438
Ice Radio Sampler (IRS) / Buffered LABRADOR 3 (BLAB3) Specifications

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>32768</td>
<td>samples/chan (8-32us trig latency)</td>
</tr>
<tr>
<td>8</td>
<td>channels/IRS ASIC</td>
</tr>
<tr>
<td>8</td>
<td>Trigger channels</td>
</tr>
<tr>
<td>~9</td>
<td>bits resolution (12-bits logging)</td>
</tr>
<tr>
<td>64</td>
<td>samples convert window (~16-64ns)</td>
</tr>
<tr>
<td>1-4</td>
<td>GSa/s</td>
</tr>
<tr>
<td>1</td>
<td>word (RAM) chan, sample readout</td>
</tr>
<tr>
<td>16</td>
<td>us to read all samples</td>
</tr>
<tr>
<td>100's</td>
<td>Hz sustained readout (multibuffer)</td>
</tr>
</tbody>
</table>

- **Difference between IRS/BLAB**
  - BLAB has input amplifier
  - IRS doesn’t really use internal trigger capability
IRS/BLAB3
Single Channel

- **Sampling:** 128 (2x 64) separate transfer lanes
  
  Recording in one set 64, transferring other ("ping-pong" → "2 stage sampling")

- **Storage:** 64 x 512 (512 = 8 * 64)

- **Wilkinson (32x2):**
  64 conv/channel
IRS/BLAB Die photo

8x RF inputs (die upside down)

32k storage cells per channel (512 groups of 64)

5.82mm

7.62mm
Analog bandwidth

ADC Frequency response

Analog BW
~1GHz
Input coupling simulation (35fF sample)

Magnitude [dB]

Frequency (Hz)

Onto chip (flip chip)

~1 GHz stored
Wilkinson ADC – easy to integrate on-chip

- No missing codes
- Linearity as good as can make ramp
- Can bracket range of interest

12-bit ADC

Labrador ADC Performance

\[ y = 1606.8x + 105.26 \]

\[ R^2 = 0.9999 \]

- Excellent linearity
- Basically as good as can make current source/comparator

Modified! (on-chip clock/counter) [\(~0.7 \text{ GHz}\)]
Storage Cell - compact

Storage Base Cell (IRS_store_cell)

Capacitance = 201 * 141 ~ 4.032 um^2 * ~4.8fF/um^2 =~20fF

- Diff. Pair as comparator
  - Density ~ 25k storage cells/mm^2 (0.25um)
On chip Wilkinson Clock

~1us to 9-10 bits
~4us to 12 bits
512 ADC in parallel
Linearity Calibration

<table>
<thead>
<tr>
<th>ADC Counts vs. Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ADC value (counts)</strong></td>
</tr>
<tr>
<td>4000</td>
</tr>
<tr>
<td>0</td>
</tr>
</tbody>
</table>

| **Chi-Square** | 3951 / 155 |
| **Parameters** | **Values** |
| p0 | 8106 ± 70.4 |
| p1 | -3.608e+04 ± 363 |
| p2 | 7.159e+04 ± 731 |
| p3 | -6.721e+04 ± 717 |
| p4 | 3.127e+04 ± 344 |
| p5 | -5671 ± 64.5 |

CAM and/or LUT in FPGA
Example: 100 MHz sine wave input

- Need dT calibrations – but only 128 per channel
- Any way to automate? (see K. Nishimura talk)
Not a small effect

More like 10% effect at 3.2GSa/s
## Now a variety of options...

<table>
<thead>
<tr>
<th>ASIC</th>
<th>Amplification?</th>
<th># chan</th>
<th>Depth/chan</th>
<th>Sampling [GSa/s]</th>
<th>Vendor</th>
<th>Size [nm]</th>
<th>Ext ADC?</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRS4</td>
<td>no.</td>
<td>8</td>
<td>1024</td>
<td>1-5</td>
<td>IBM</td>
<td>250</td>
<td>yes.</td>
</tr>
<tr>
<td>SAM</td>
<td>no.</td>
<td>2</td>
<td>1024</td>
<td>1-3</td>
<td>AMS</td>
<td>350</td>
<td>yes.</td>
</tr>
<tr>
<td>IRS2</td>
<td>no.</td>
<td>8</td>
<td>32536</td>
<td>1-4</td>
<td>TSMC</td>
<td>250</td>
<td>no.</td>
</tr>
<tr>
<td>BLAB3A</td>
<td>yes.</td>
<td>8</td>
<td>32536</td>
<td>1-4</td>
<td>TSMC</td>
<td>250</td>
<td>no.</td>
</tr>
<tr>
<td>TARGET</td>
<td>no.</td>
<td>16</td>
<td>4192</td>
<td>1-2.5</td>
<td>TSMC</td>
<td>250</td>
<td>no.</td>
</tr>
<tr>
<td>TARGET2</td>
<td>yes.</td>
<td>16</td>
<td>16384</td>
<td>1-2.5</td>
<td>TSMC</td>
<td>250</td>
<td>no.</td>
</tr>
<tr>
<td>TARGET3</td>
<td>no.</td>
<td>16</td>
<td>16384</td>
<td>1-2.5</td>
<td>TSMC</td>
<td>250</td>
<td>no.</td>
</tr>
<tr>
<td>PSEC3</td>
<td>no.</td>
<td>4</td>
<td>256</td>
<td>1-16</td>
<td>IBM</td>
<td>130</td>
<td>no.</td>
</tr>
<tr>
<td>PSEC4</td>
<td>no.</td>
<td>6</td>
<td>256</td>
<td>1-16</td>
<td>IBM</td>
<td>130</td>
<td>no.</td>
</tr>
</tbody>
</table>

→ **Success of PSEC3: proof-of-concept of moving toward smaller feature sizes.**
- Next DRS plans to use 110nm; next SAM plans to use 180 nm.
Future Prospects

• Expect many other designs in future
  – Barriers to entry are low
  – Many different reference designs out there

• Challenges (R&D continues):
  – Fine timing (~ 1ps)
  – Larger dynamic range
  – Deeper (continuous) sampling
  – Faster, sparsified readout
  – Calibration

• Key enabling technology
  – Large telescope arrays (CTA)
  – > 100km³ neutrino detectors
  – PID, Fast x-ray detectors
Back-up slides
Underlying Technology

- **Track and Hold (T/H)**

- **Pipelined storage** = array of T/H elements, with output buffering

![Diagram of T/H circuit and pipelined storage](image)
Real MCP-PMT Signals (with BLAB2)

Residual Time Walk

Rather robust for amplitude invariant signals, TOF still hard, but can shape extract.

7-8 psRMS

BLAB1
Entries 10000
Mean 4.381
RMS 2.56

BLAB1
Entries 9764
Mean 3.958
Mean y 0.0001665
RMS 1.73
RMS y 0.007667
Simulated Performance vs. SNR

Time Difference Dependence on Signal-Noise Ratio (SNR)

\[ \sqrt{kT \Delta \nu} \]

Signal Noise Ratio

Time Difference Resolution [ps]

300MHz ABW, 5.9GSa/s
IRS Input Coupling

• Input bandwidth depends on 2x terms
  – \( f_{3\text{dB}[\text{input}]} = \left(2\pi Z C_{\text{tot}}\right)^{-1} \)
  – \( f_{3\text{dB}[\text{storage}]} = \left(2\pi R_{\text{on}} C_{\text{store}}\right)^{-1} \)
Wilkinson Clock Generation

IRS Wilk PRO Strb (IRS_WilkPRO)

- Strictly only 5 channels necessary
  - 4x antenna, 1x reference channels
  - Could interleave for twice depth, or multiple reference channels
Wilkinson Recording

Start = start 0.5-1.5GHz Clock

Ripple counter (run as fast as can)
Triggering

IRS Trigger 1 (IRS_trig1)

- Need 9\textsuperscript{th} channel for monitoring

\[ 4.38\text{um} \times 3.84\text{um} = 16\text{um}^2 \approx 100\text{fF} \]

\[ dQ = C \Delta V = (100\text{fF}) (1.5\text{V}) \quad \text{dt} \approx 5\text{ns} \]

\[ I = \frac{dQ}{dt} = \frac{(150\text{fC})}{(50\text{ns})} \approx 30\text{uA} \]
Triggering – same as previous results

- Monitor 9\textsuperscript{th} channel (uses Ch.1 threshold) to compensate for temperature dependence
**Hit Processing numbers**

Assume:
- 100kHz charged track hits on each bar
- ~32 p.e./track (1% of 100ns windows)
- 30kHz trigger rate
- Each PMT pair sees <8> hits
- 240k hits/s
- Each BLAB3 has an average occupancy <1 hit (assume 1)
- 400ns to convert 256 samples
- 16ns/sample to transfer
- At least 16 deep buffering
  (Markov overflow probability est. < 10^{-38})

Each hit = 64 samples * 8 bits = 512 bits
\(\Rightarrow\) ~125 Mbits/s
(link is 3.0 Gb/s \(\sim\) x30 margin)

**BLAB3 ASIC**

- Trans-Imp Amps
- 512 x 64 samples
- Per channel
- BLAB3 sampling
- Fast conversion Matrix (x256)

**Improvements based upon**

**Lessons learned from BLAB2**

Plan to model in standard queuing simulator, but looks like no problem
(CF have done same exercise with Jerry Va’vra for 150kHz L1 of SuperB and can handle rate)
Front-end Electronics studies

1GHz analog bandwidth, 5GSa/s

Simulation includes detector response

G. Varner and L. Ruckman

J-F Genat, G. Varner, F. Tang, H. Frisch
Ice Radio Sampler (IRS)

RF input coupling (S11)

P. Gorham -- measurement
Ice Radio Sampler (IRS)

P. Gorham -- measurement
WFS Evolution and Philosophy

• **SAM**
  1. Maximize dynamic range and minimize signal distortion.
  3. Minimize costs (both for development & production)

• **DRS family**
  – Get a solid, general design working
  – Something that can work, in volume, for many apps

• **LAB and siblings (6→8 generations)**
  – Continue to explore parameter space
  – Concentrate on applications where more general solutions above many not be best choice

Approaches very complementary
References

• PSI activities (DRS)
  – IEEE/NSS 2008, TIPPo9
  – http://midas.psi.ch/drs

• DAPNIA activities

• Hawaii activities
  – STURM: EPAC08-TUOCM02, June, 2008.