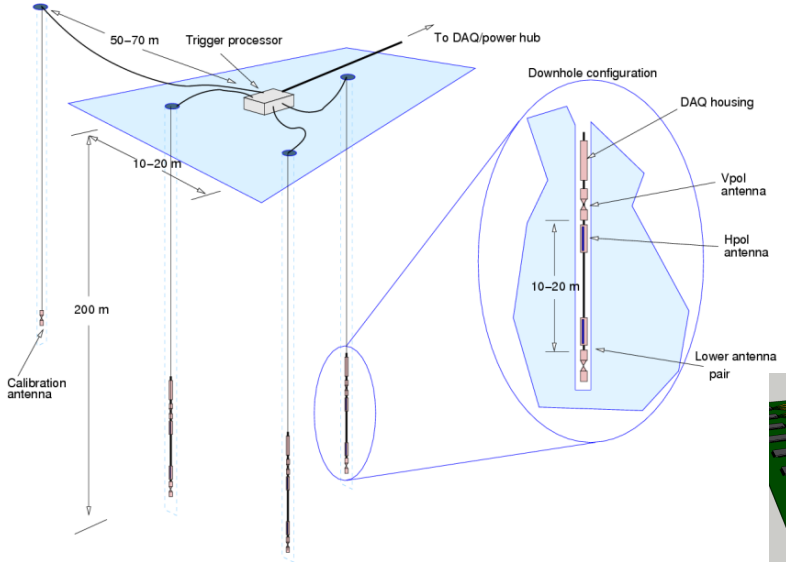
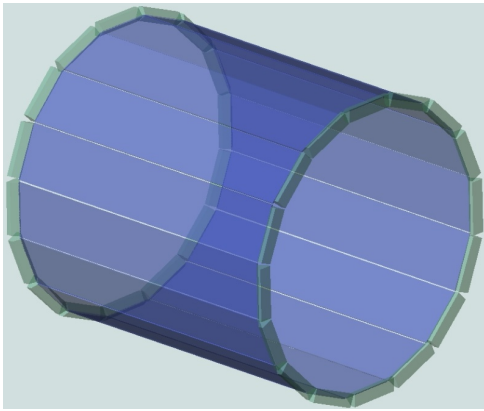
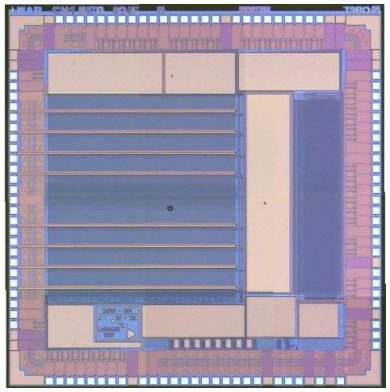
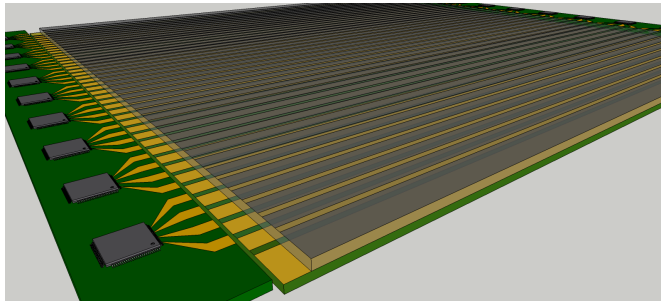
Deeper Sampling CMOS Transient Waveform Recording ASICs

The IRS and BLAB3 Deep Storage ASICs for UHE Radio Neutrino and Next Generation Collider Particle Identification









Matt Andrew, Kurtis Nishimura, Gary S. Varner

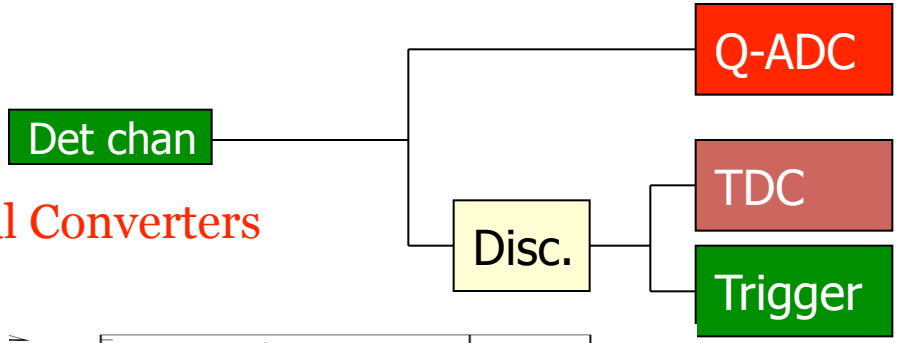
University of Hawai'i, and the

Large Area Picosecond PhotoDetector Collaboration

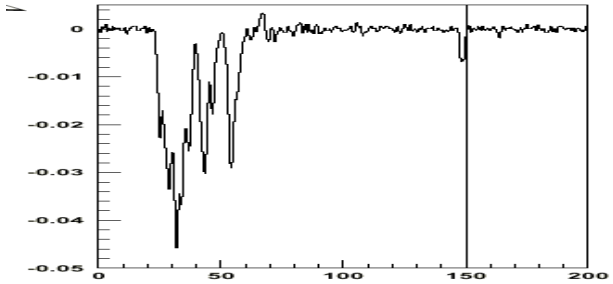
TIPP 2011, June 10, 2011

Why Waveform Sampling?

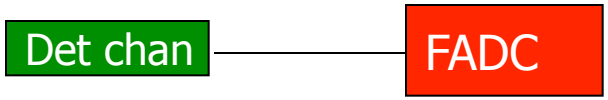
- Traditional "crate based" electronics
  - Gated Analog-to-Digital Converters
  - Referenced "triggered" Time-to-Digital Converters



- High-rate applications
  - "pipelined operation"
  - Low-speed, low-resolution sampling



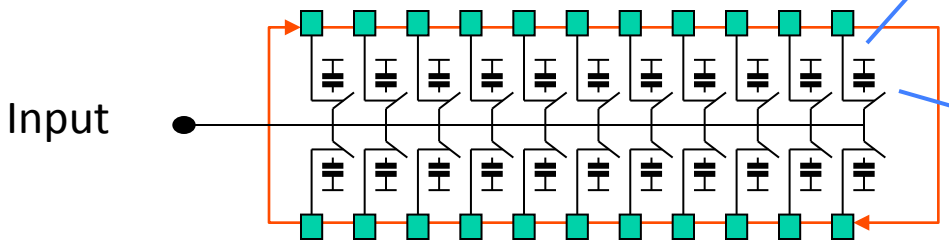
- High channel counts
  - Motivation to reduce cabling
  - Integrate electronics onto detector elements

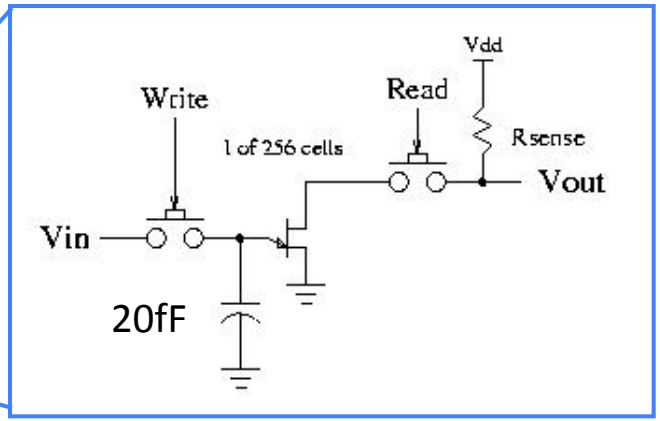


Issues: cost, power, resolution, data volume

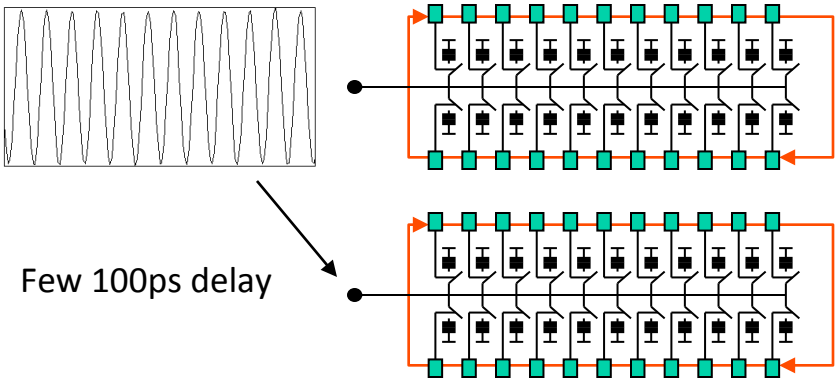
Switched Capacitor Array Sampling

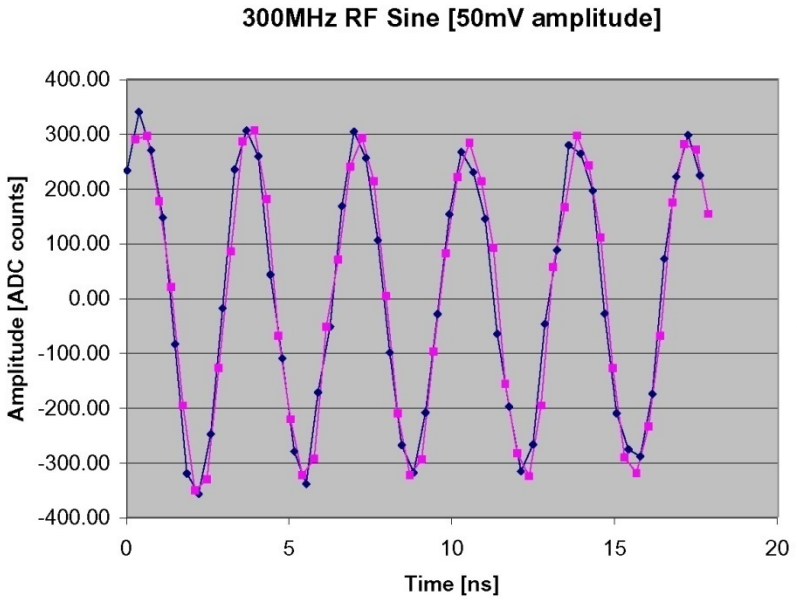
- Write pointer is ~few switches closed @ once



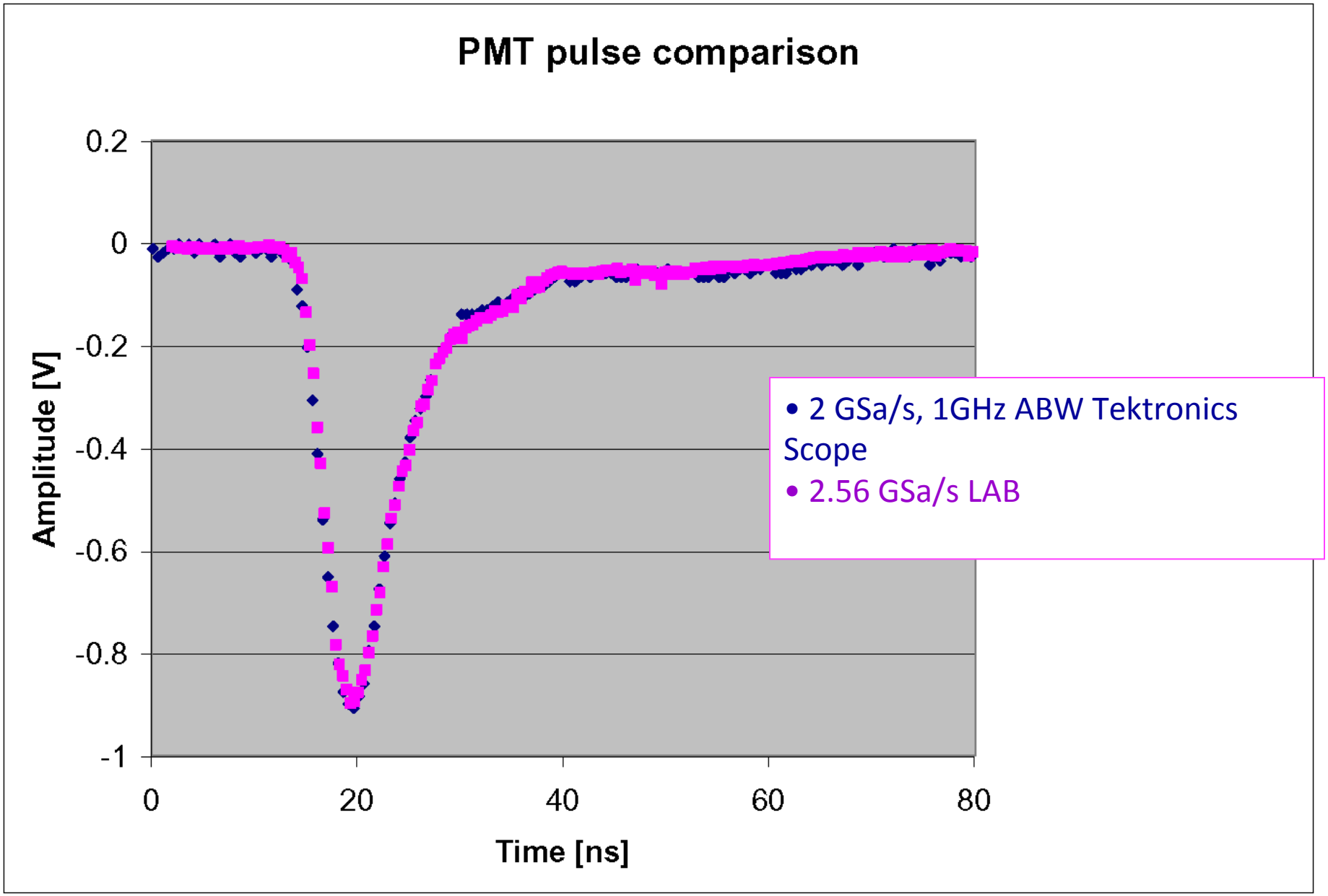


Tiny charge: 1mV ~ 100e$^-$

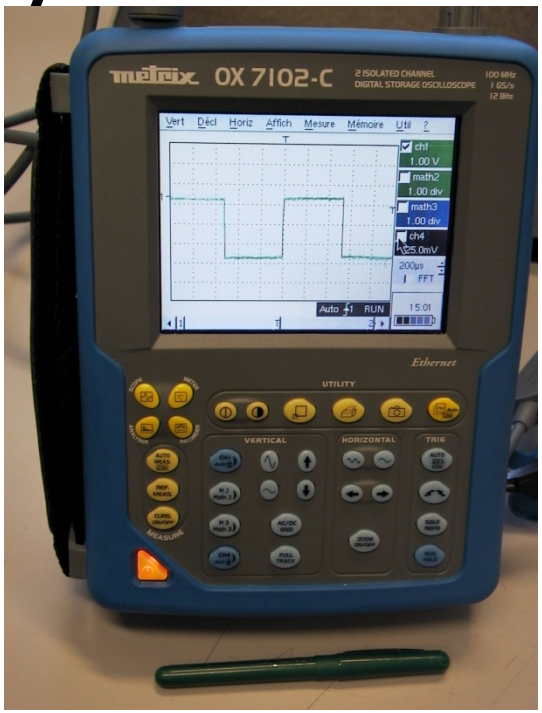


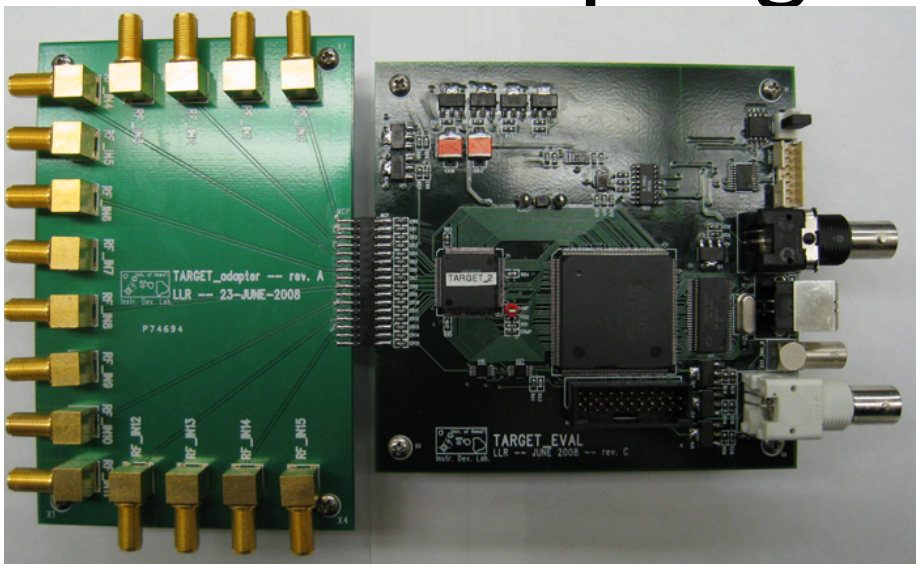


“Oscilloscope on a chip”



Easy access to Waveform sampling



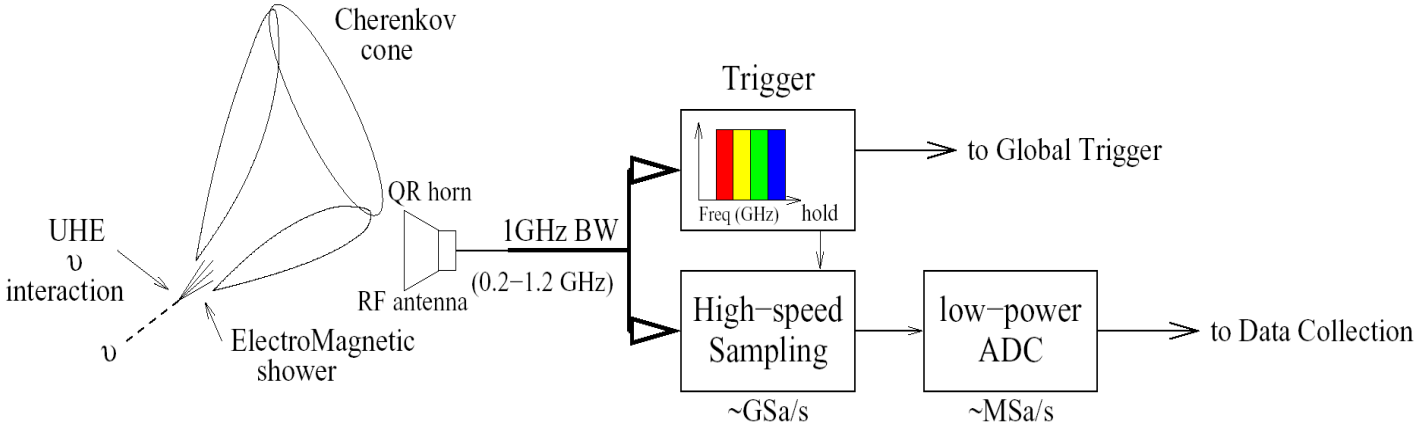


	WFS ASIC	Commercial
Sampling speed	0.1-6 GSa/s	3 GSa/s
Bits/ENOBs	16/9-13+	8/7.4
Power/Chan.	<= 0.05W	Few W
Cost/Ch.	< $10 (vol)	> 100$

An Intrinsic Limitation

No power (performance savings) for continuous digitization

We aren't going to put Analog Devices out of business

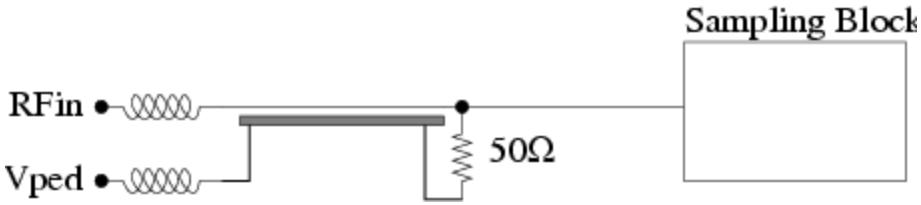


"analog down conversion"

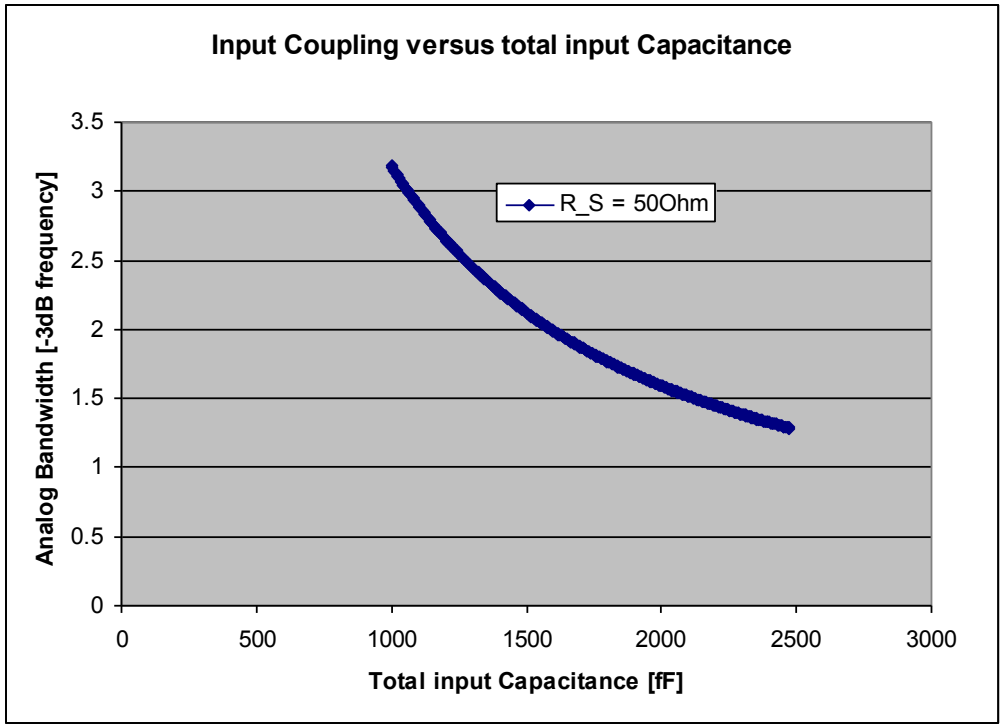
→ For most "triggered" 'event' applications, *not a serious drawback*

Gigasamples/s, but Nyquist?

Difficult to couple in Large BW (input C is deadly)

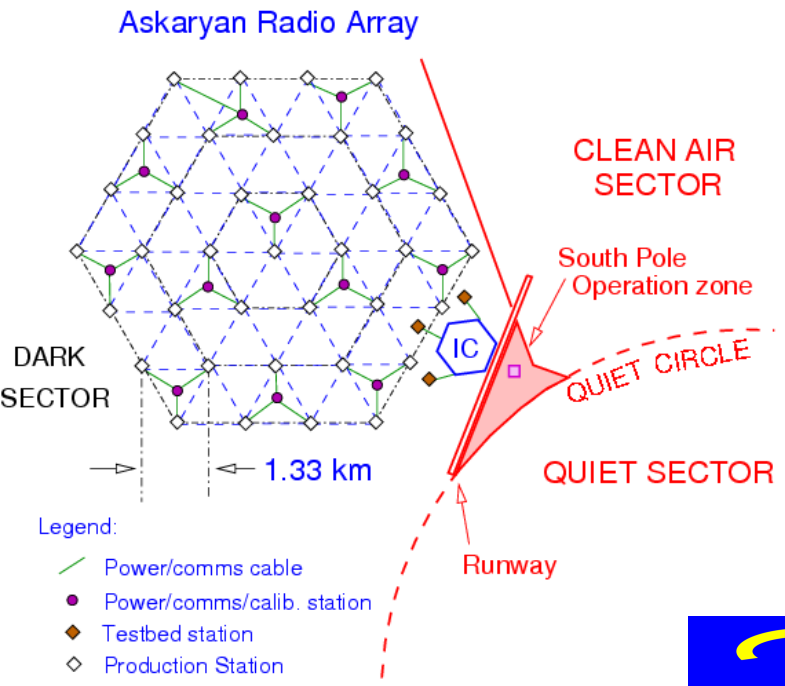


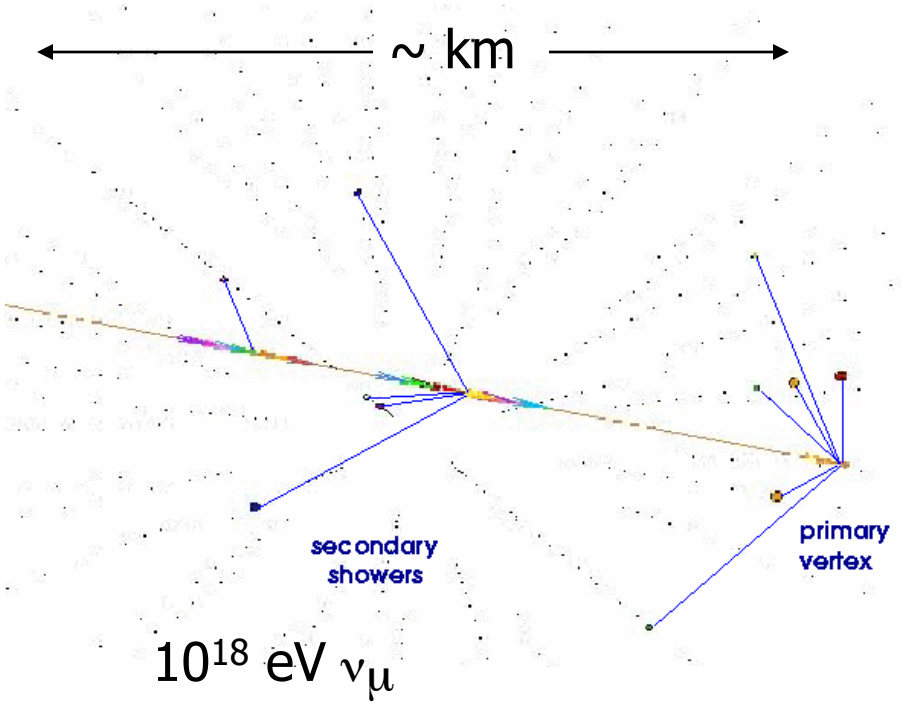
$f_{3dB} = 1/2\pi ZC$



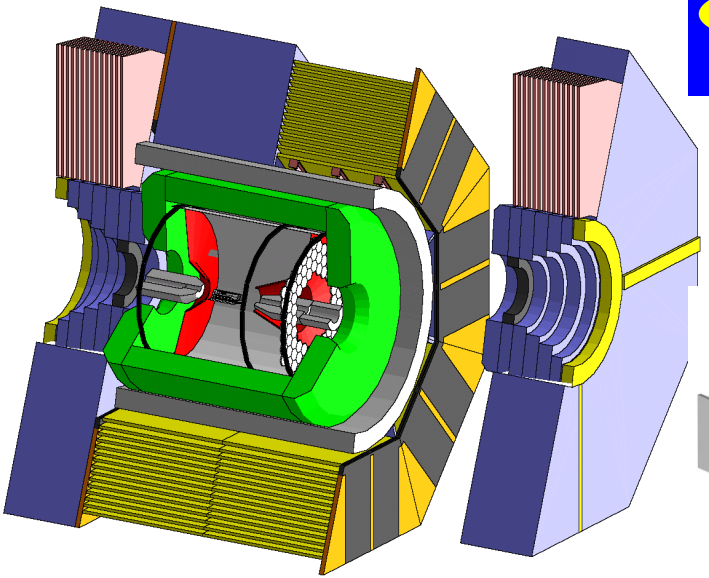
- More than 3pF input (ESD protection alone often more) limits ABW < 1GHz
- As a result, first generation WFS ASICs a few hundred to 1k samples (ATWD, SAM, DRS, LABRADOR…)
- Is this an fundamental limitation?

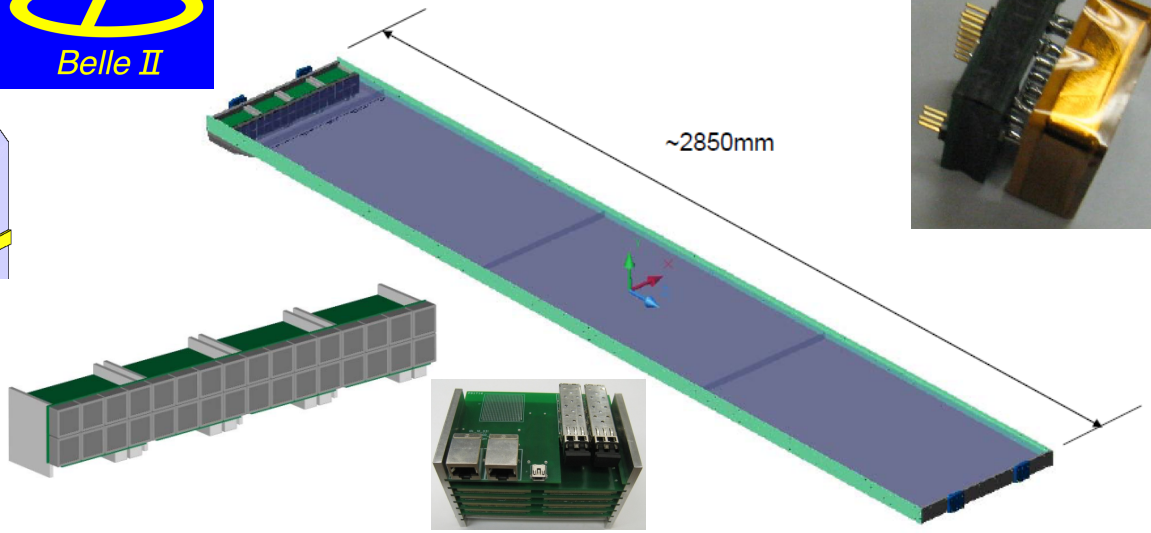
Why Deeper sampling?



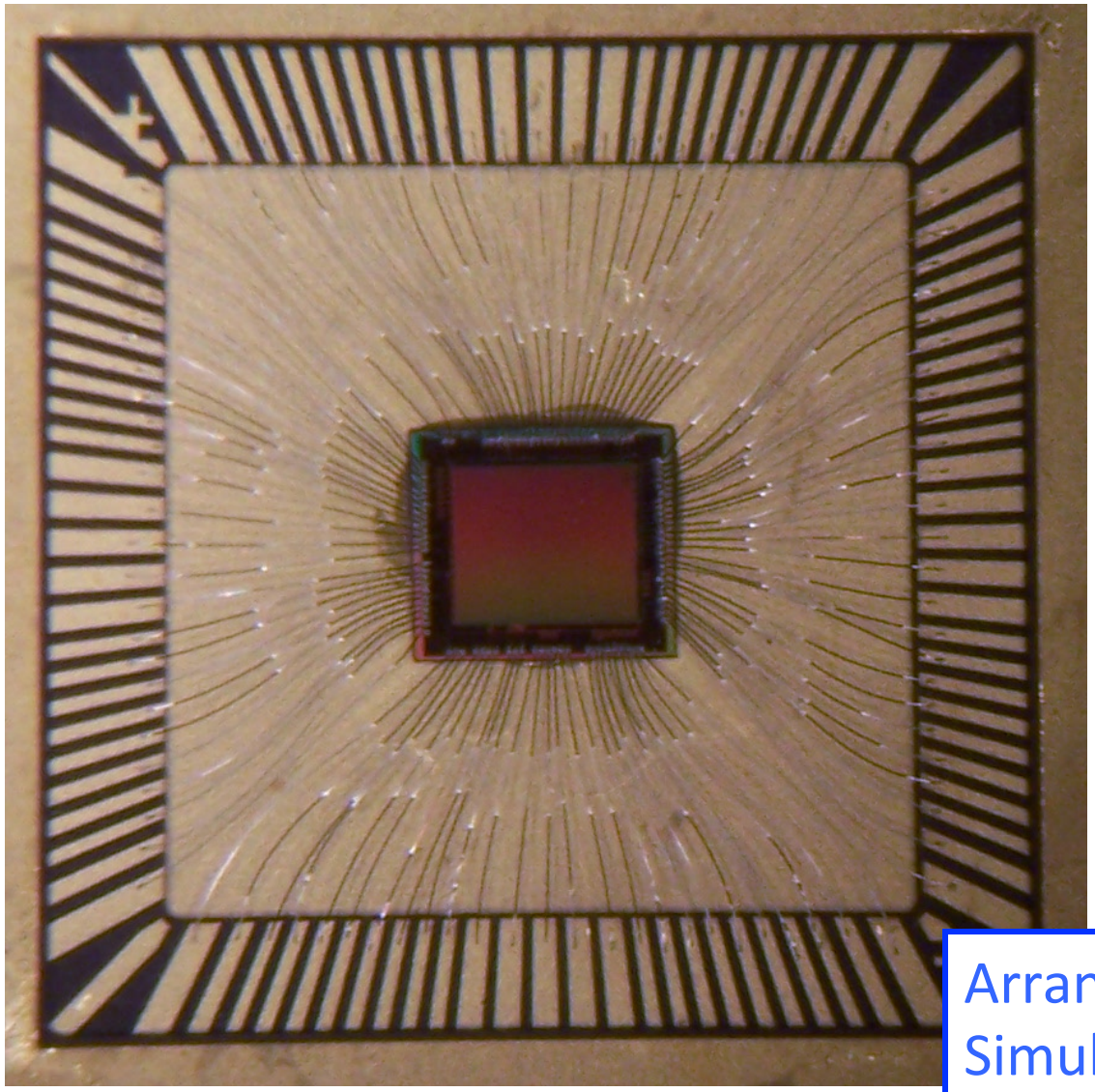


10^{18} eV ν_μ





Deeper storage: Buffered LABRADOR (BLAB1) ASIC



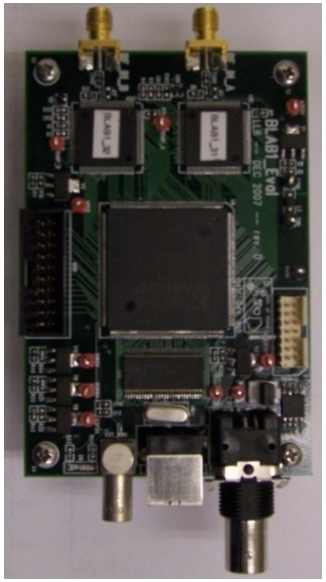
3mm x 2.8mm, TSMC 0.25um

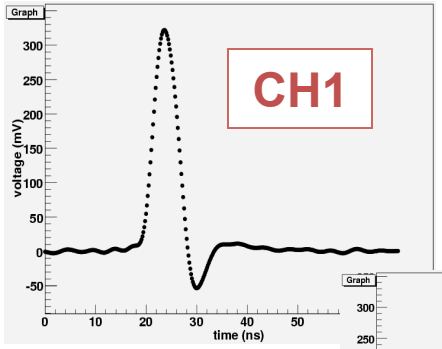
- Single channel
- 64k samples deep, same SCA technique as LAB, no ripple pointer
- Multi-MSa/s to Multi-GSa/s
- 12-64us to form Global trigger

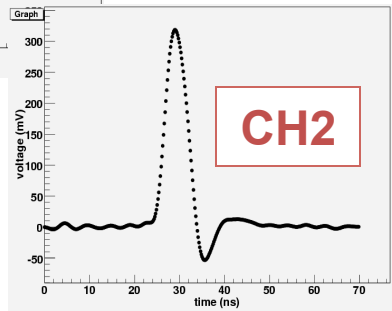
Arranged as 128 x 512 samples
Simultaneous Write/Read

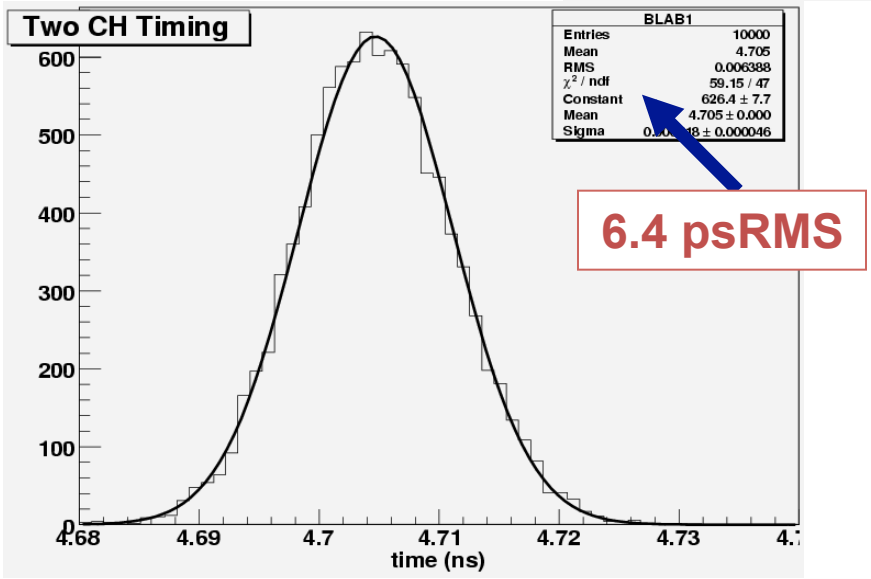
BLAB1 High speed Waveform sampling

- Comparable performance to best CFD + HPTDC
- MUCH lower power, no need for huge cable plant!
- Using full samples reduces the impact of noise
- Photodetector limited









NIM **A602** (2009) 438

Ice Radio Sampler (IRS) / Buffered LABRADOR 3 (BLAB3) Specifications

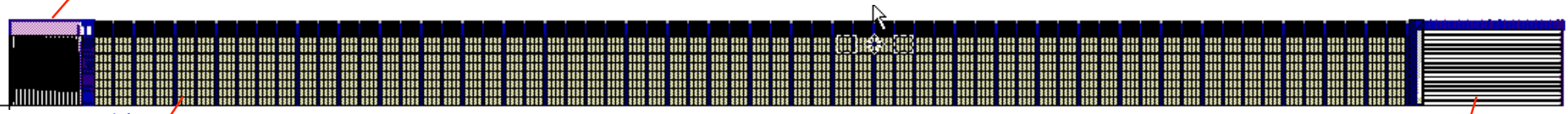
32768	samples/chan (8-32us trig latency)
8	channels/IRS ASIC
8	Trigger channels
~9	bits resolution (12-bits logging)
64	samples convert window (~16-64ns)
1-4	GSa/s
1	word (RAM) chan, sample readout
16	us to read all samples
100's	Hz sustained readout (multibuffer)

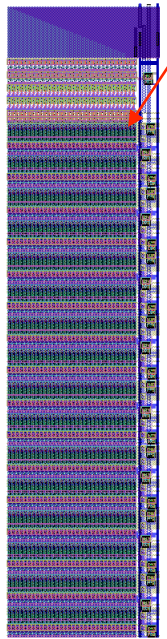
- Difference between IRS/BLAB
  - BLAB has input amplifier
  - IRS doesn't really use internal trigger capability

IRS/BLAB3
Single Channel

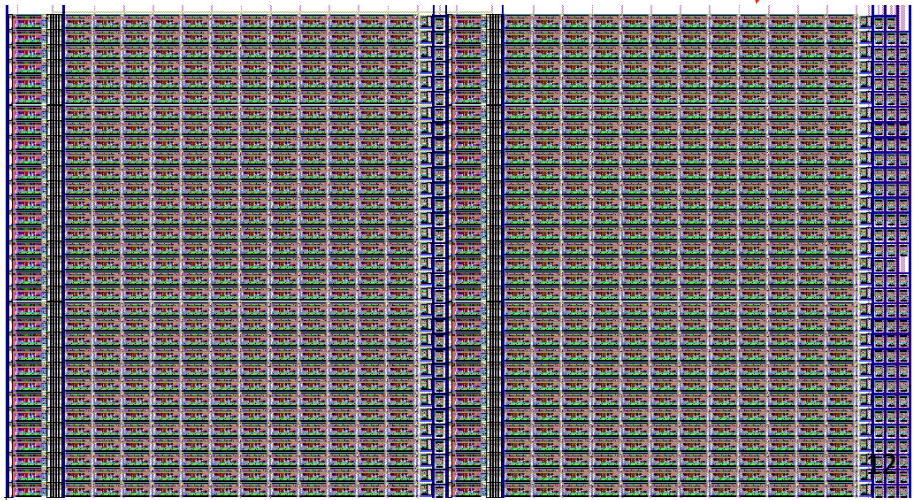
- Sampling: 128 (2x 64) separate transfer lanes

Recording in one set 64, transferring other
("ping-pong" → "2 stage sampling")



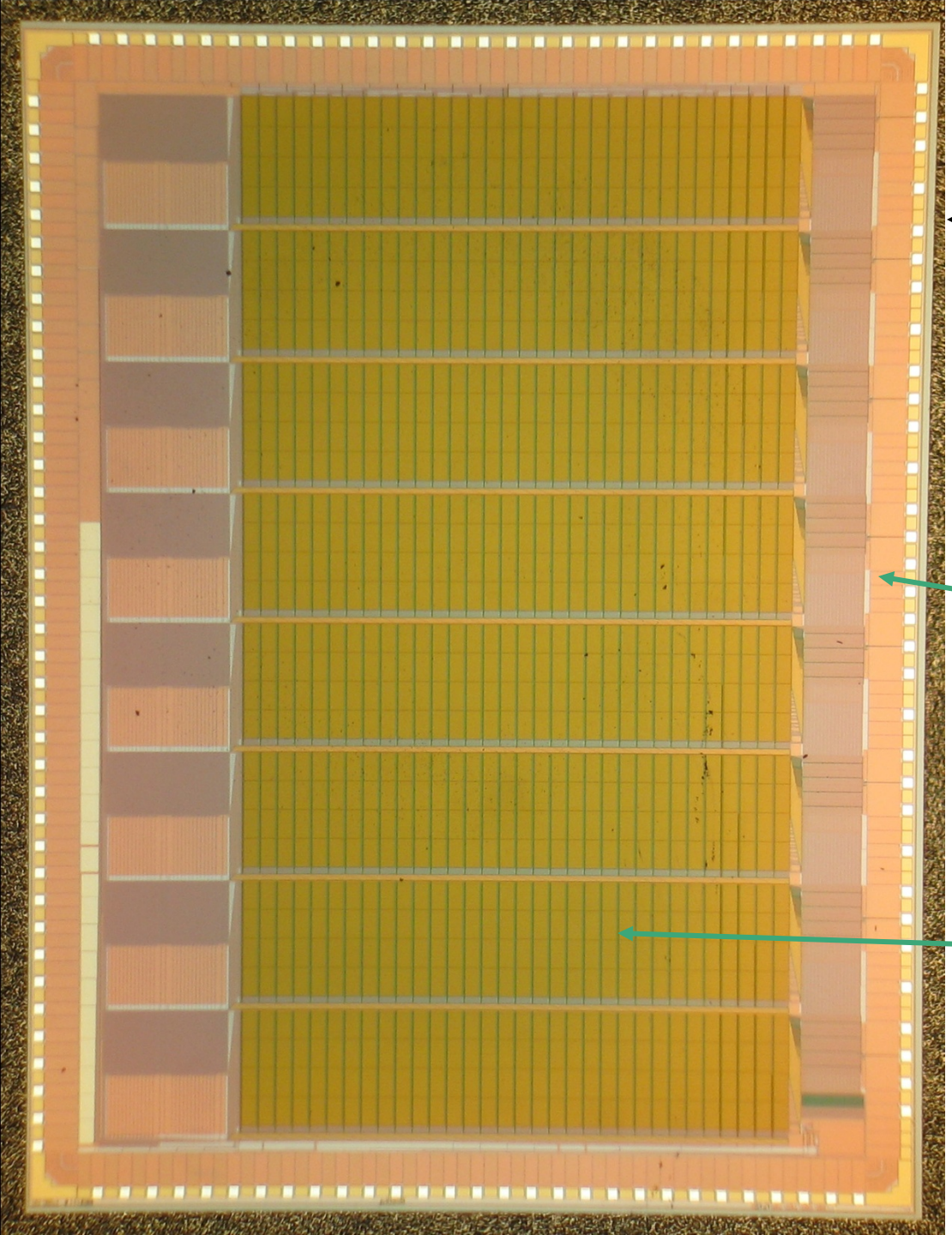


- Storage: 64 x 512 (512 = 8 * 64)

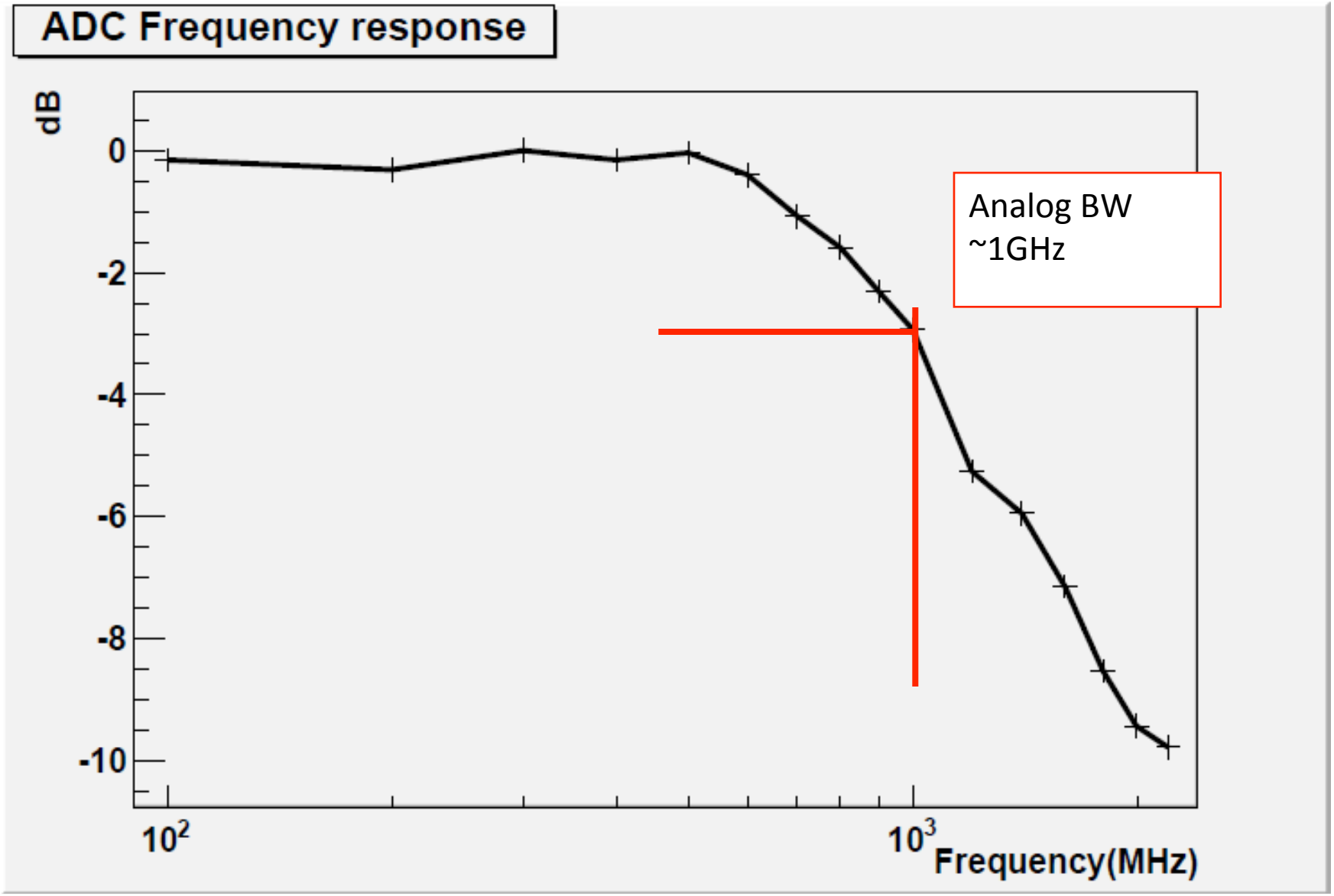


- Wilkinson (32x2): 64 conv/channel

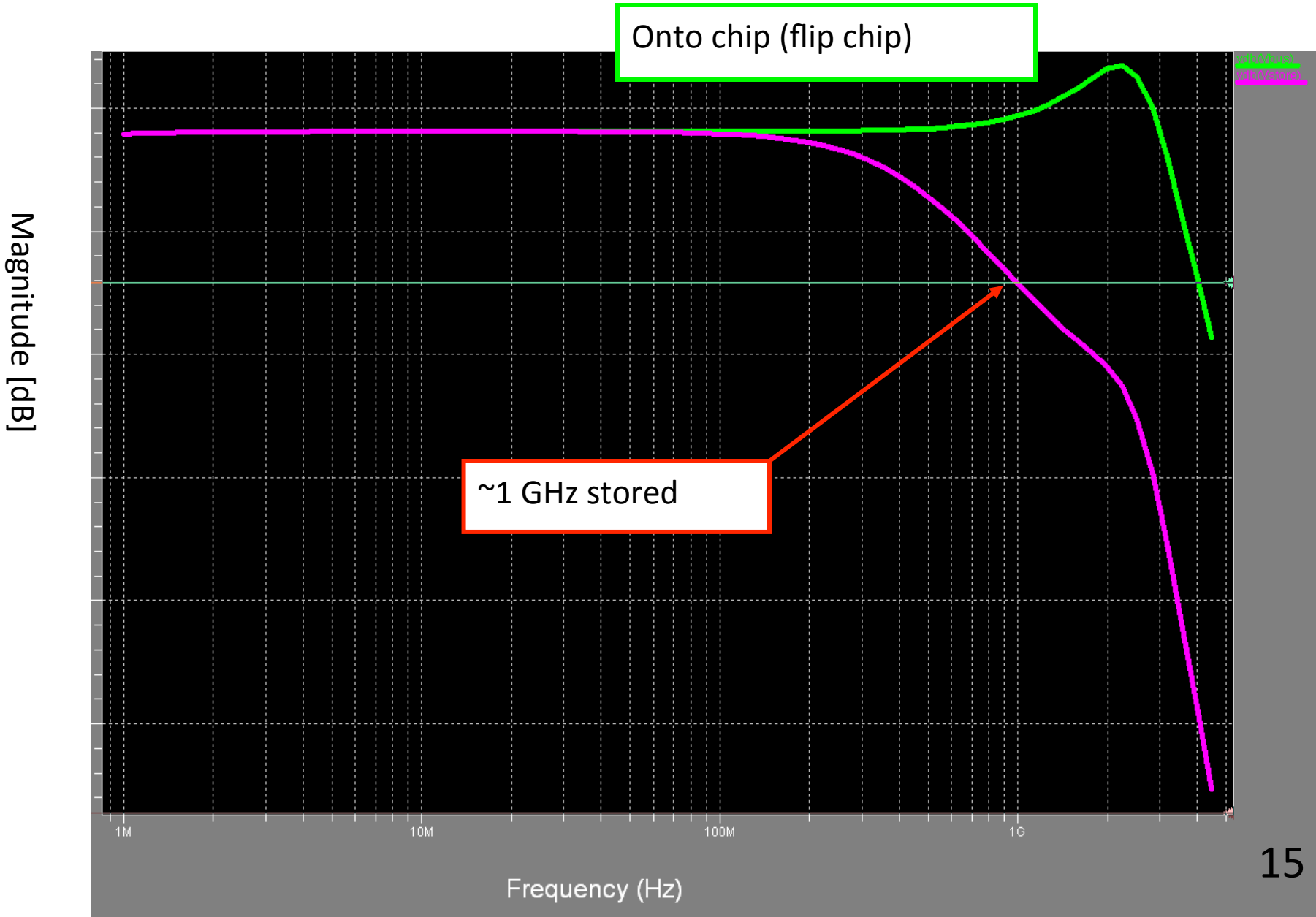
IRS/BLAB Die photo



Analog bandwidth

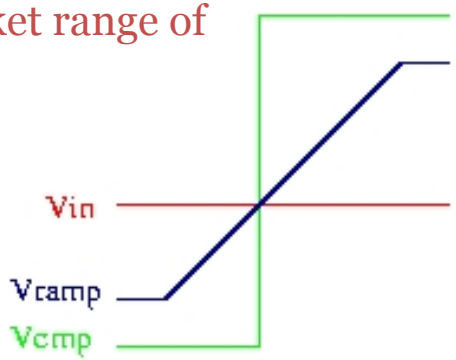


Input coupling simulation (35fF sample)

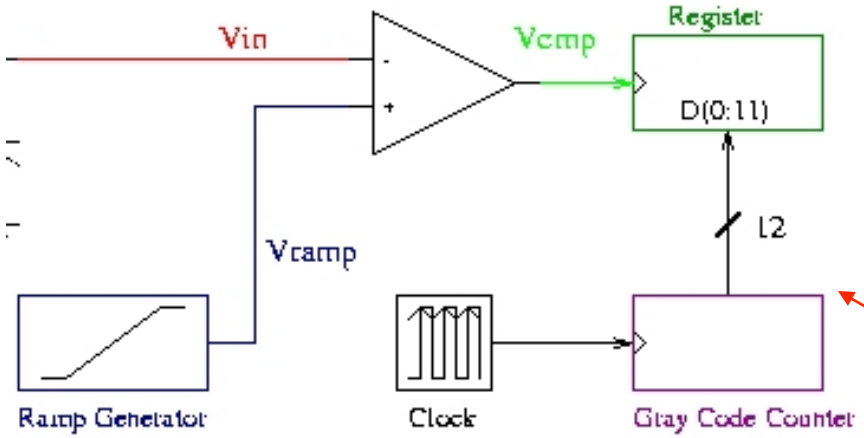


Wilkinson ADC – easy to integrate on-chip

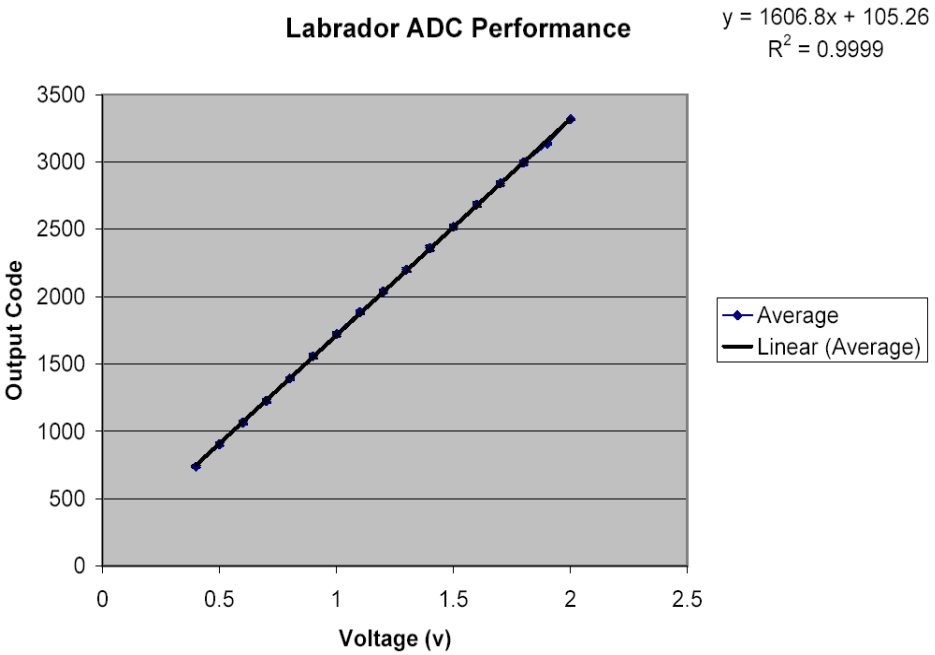
- No missing codes
- Linearity as good as can make ramp
- Can bracket range of interest



Run count during ramp



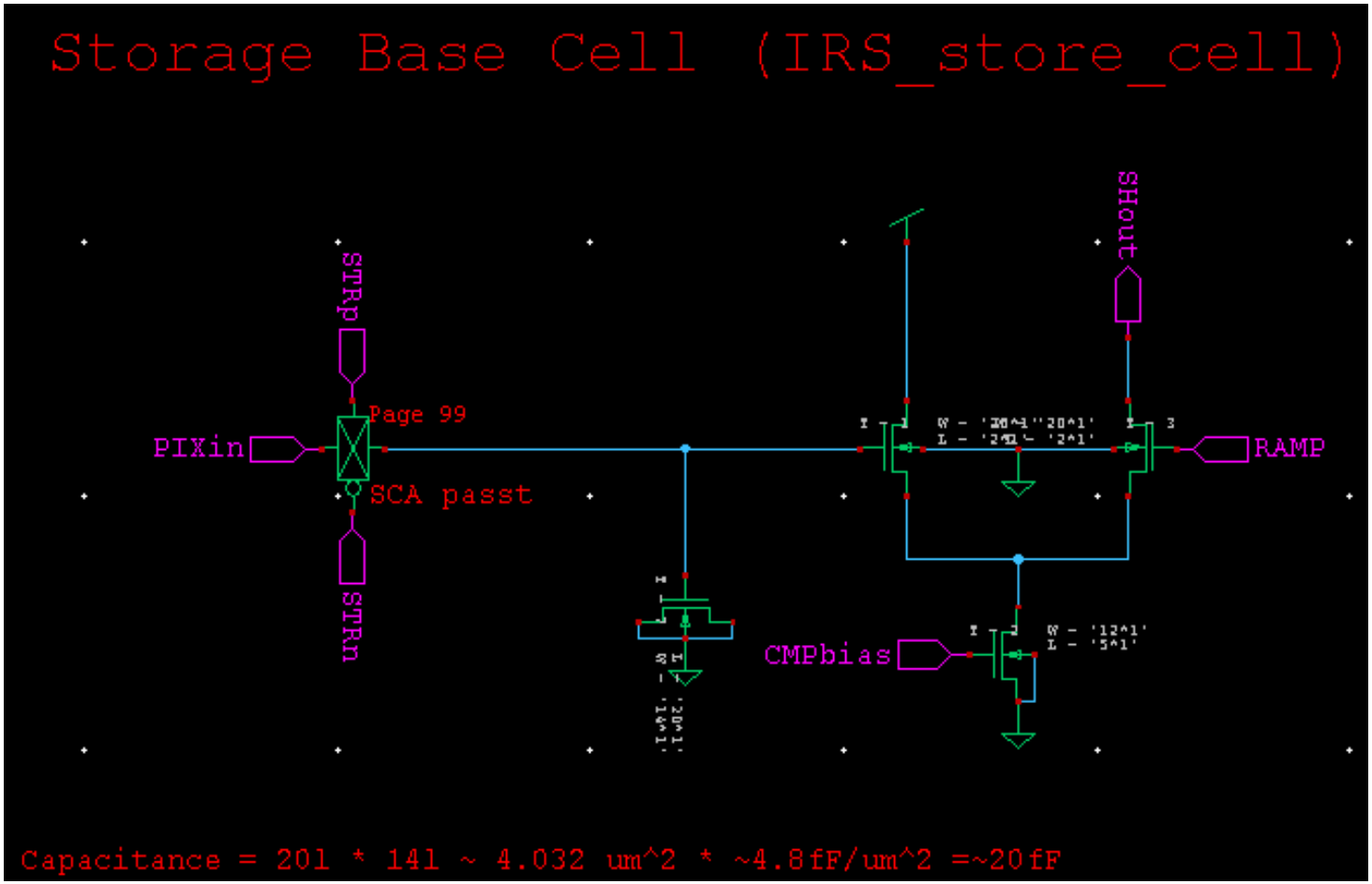
12-bit ADC

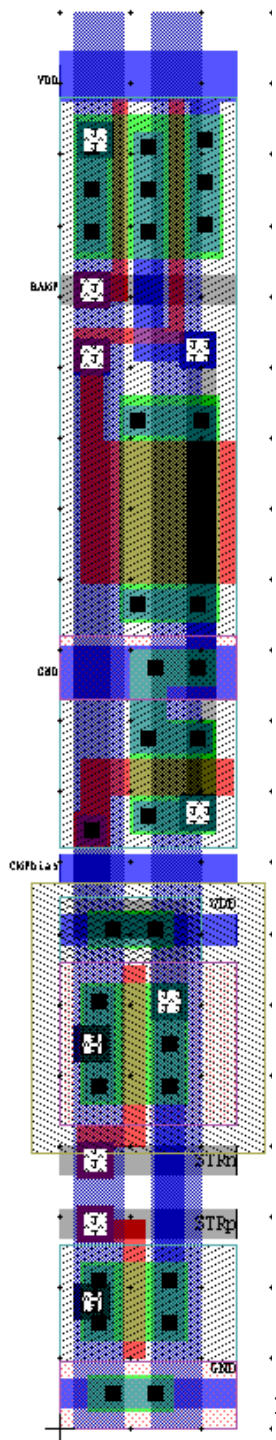


Modified! (on-chip clock/counter) [~0.7 GHz]

- Excellent linearity
- Basically as good as can make current source/ comparator

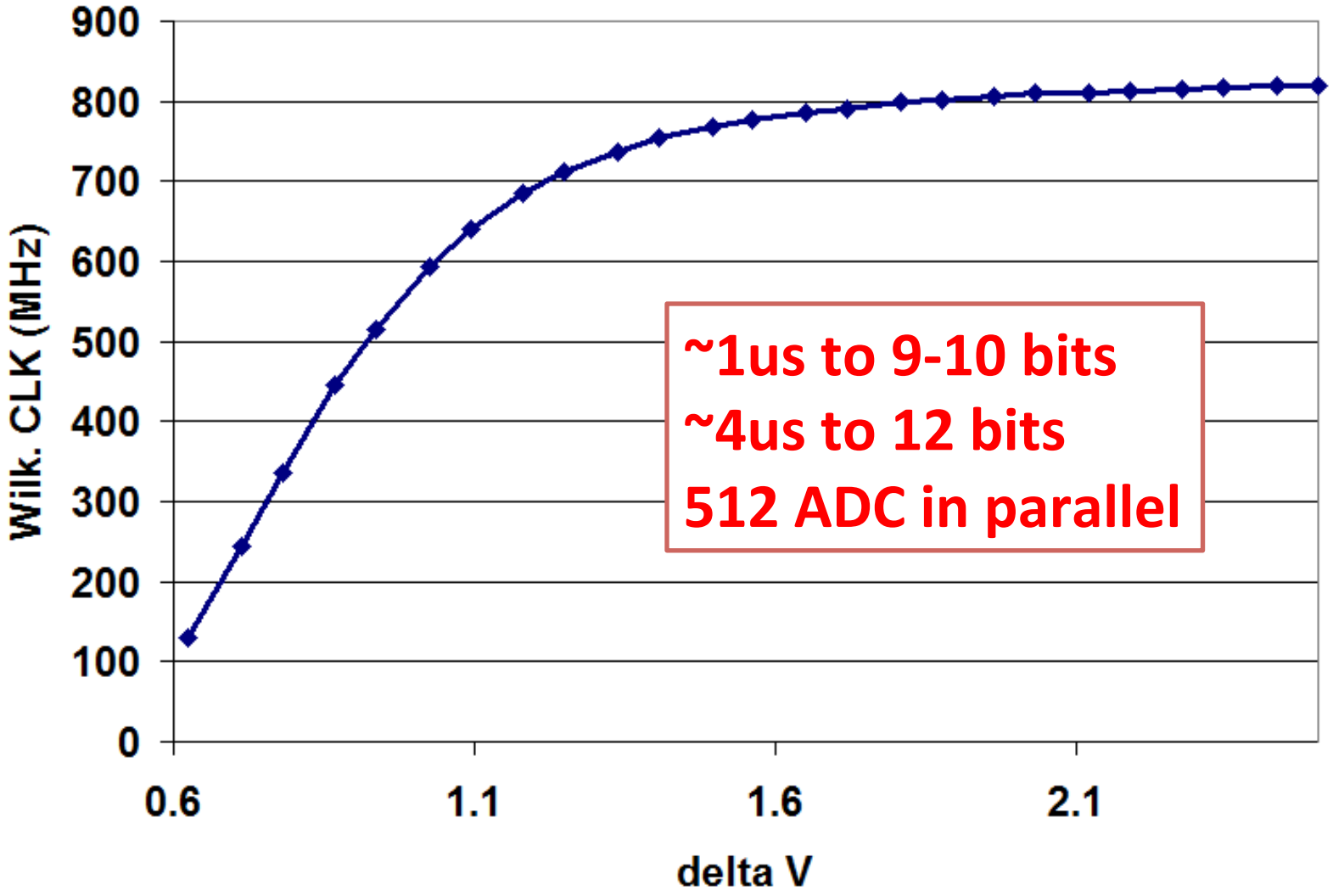
Storage Cell - compact



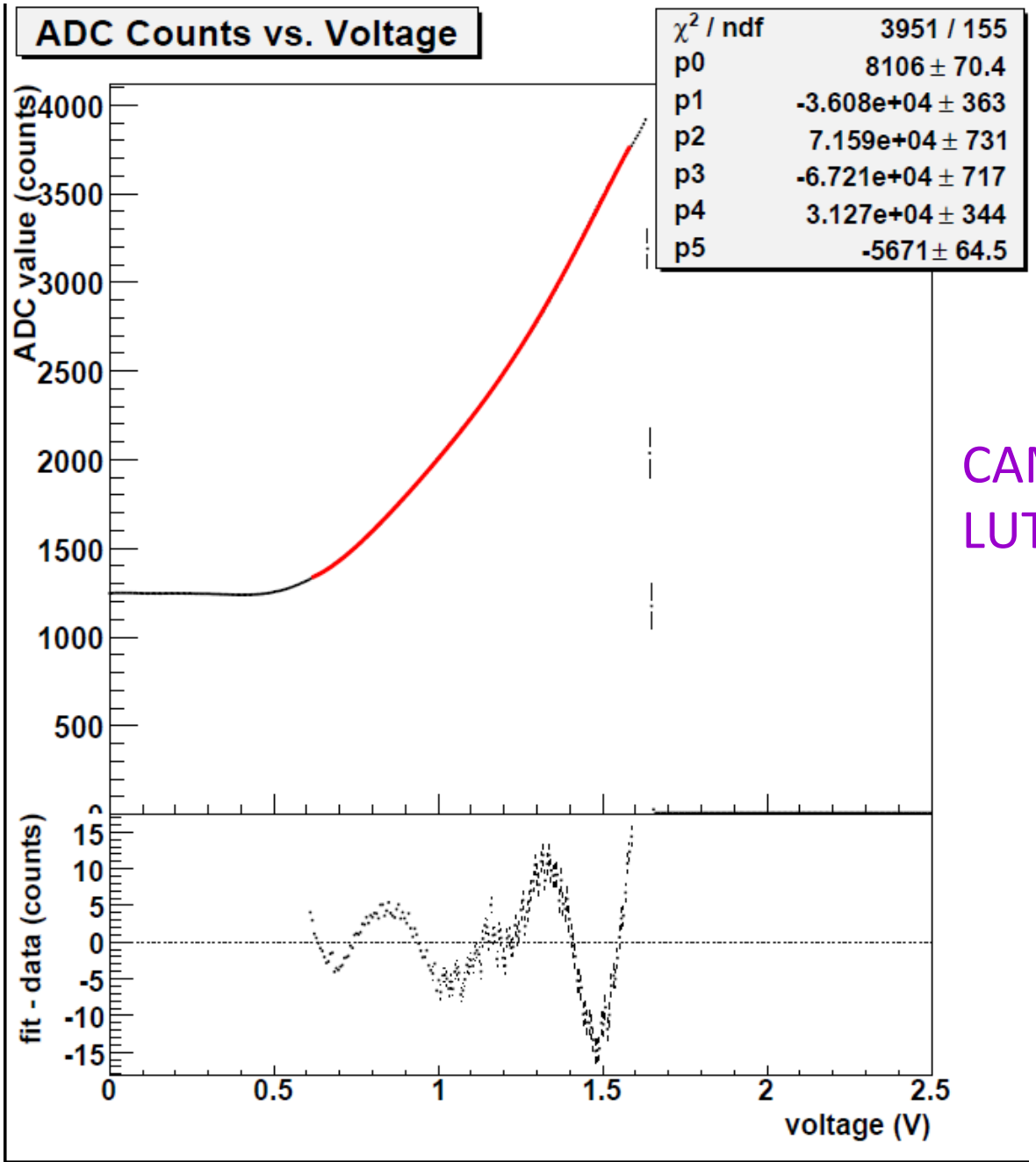


- Diff. Pair as comparator
  - Density ~ 25k storage cells/mm^2 (0.25um)

On chip Wilkinson Clock

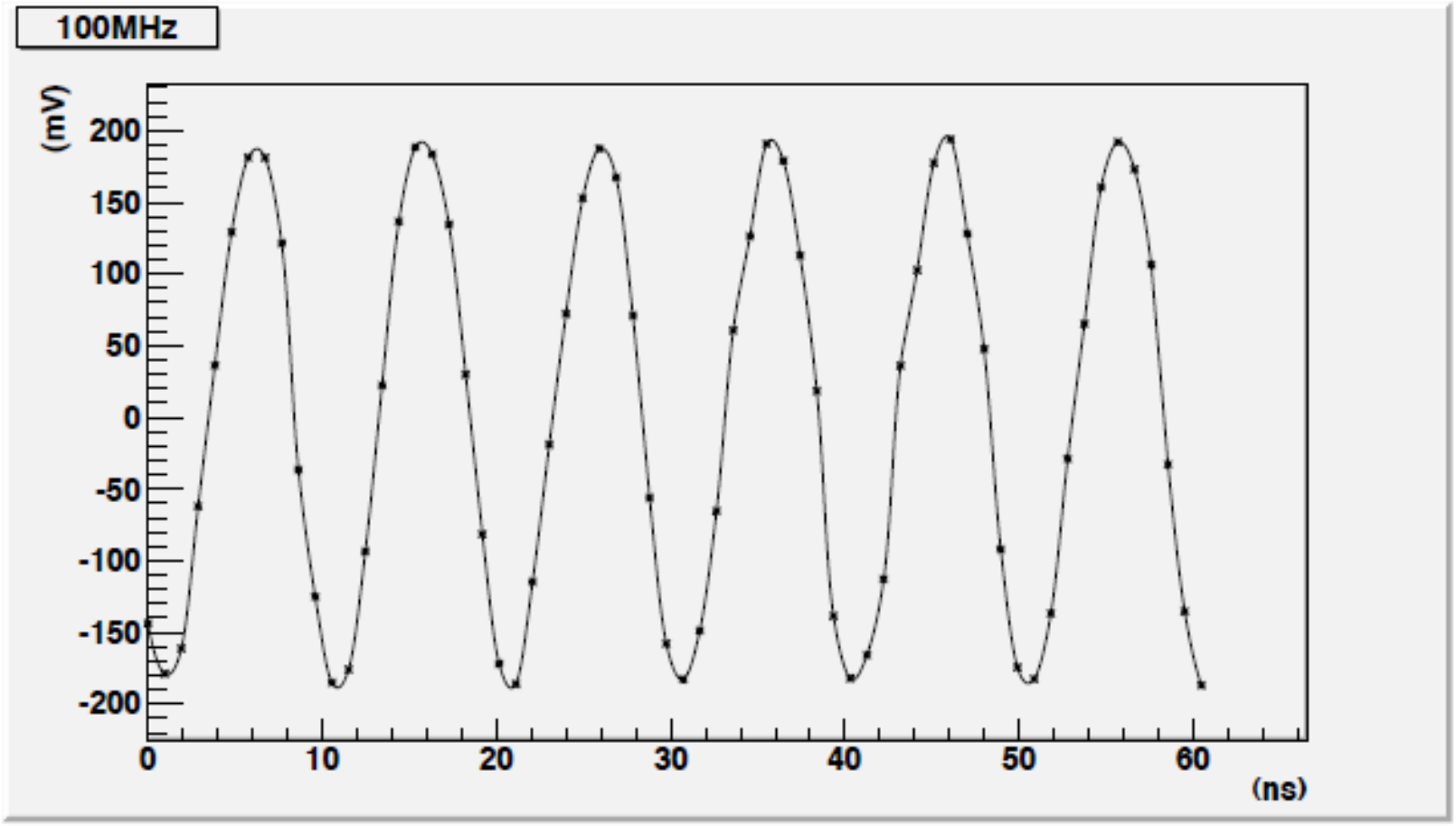


Linearity Calibration



CAM and/or
LUT in FPGA

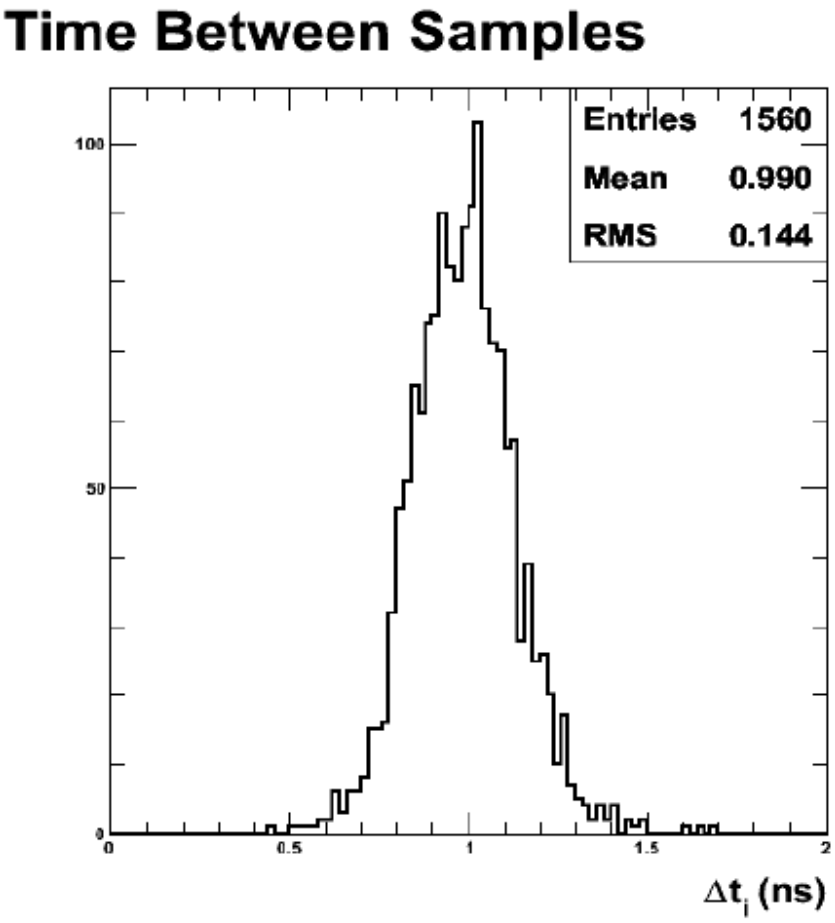
Example: 100 MHz sine wave input

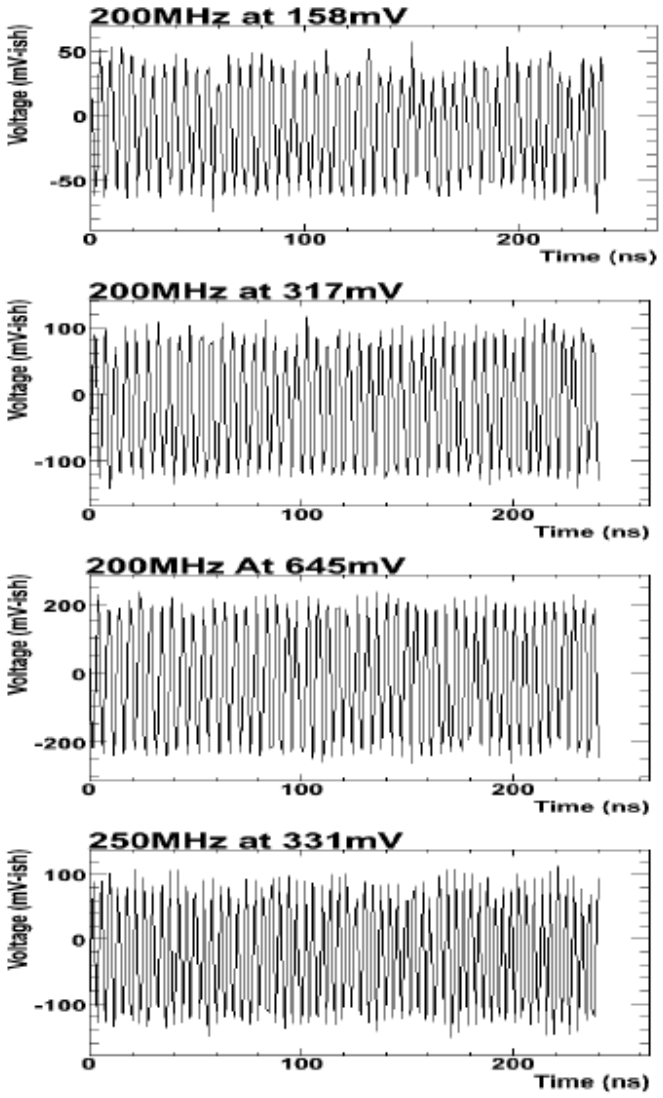


- Need dT calibrations – but only 128 per channel
- Any way to automate? (see K. Nishimura talk)

Not a small effect

J. Davies –UC London





More like 10% effect at 3.2GSa/s

Now a variety of options…

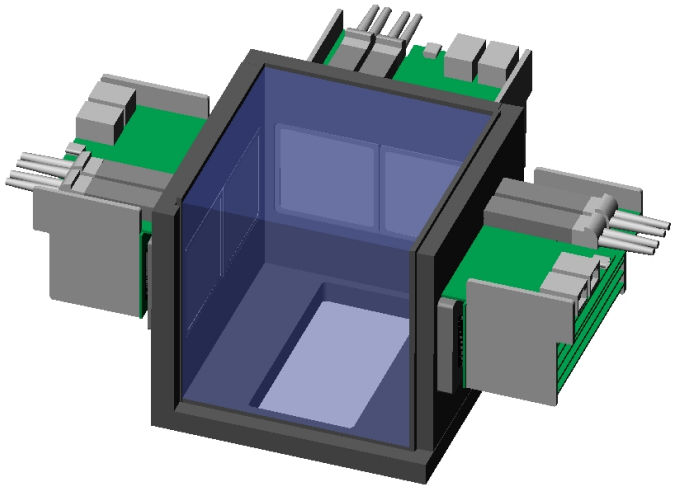
ASIC	Amplification?	# chan	Depth/chan	Sampling [GSa/s]	Vendor	Size [nm]	Ext ADC?
DRS4	no.	8	1024	1-5	IBM	250	yes.
SAM	no.	2	1024	1-3	AMS	350	yes.
IRS2	no.	8	32536	1-4	TSMC	250	no.
BLAB3A	yes.	8	32536	1-4	TSMC	250	no.
TARGET	no.	16	4192	1-2.5	TSMC	250	no.
TARGET2	yes.	16	16384	1-2.5	TSMC	250	no.
TARGET3	no.	16	16384	1-2.5	TSMC	250	no.
PSEC3	no.	4	256	1-16	IBM	130	no.
PSEC4	no.	6	256	1-16	IBM	130	no.

➔ **Success of PSEC3: proof-of-concept of moving toward smaller feature sizes.**

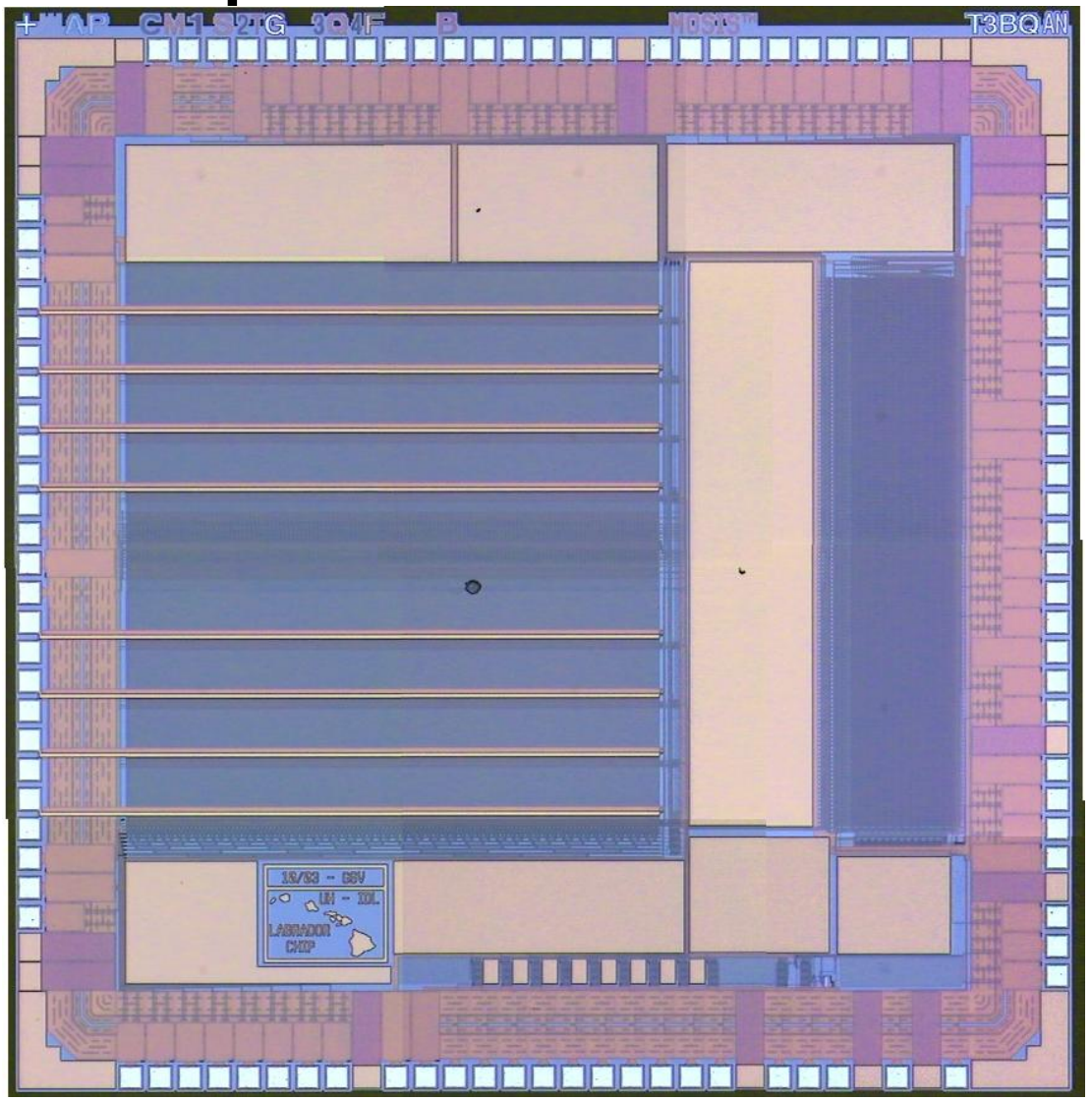
- Next DRS plans to use 110nm; next SAM plans to use 180 nm.

Future Prospects

- Expect many other designs in future
  - Barriers to entry are low
  - Many different reference designs out there
- Challenges (R&D continues):
  - Fine timing (~ 1ps)
  - Larger dynamic range
  - Deeper (continuous) sampling
  - Faster, sparsified readout
  - Calibration
- Key enabling technology
  - Large telescope arrays (CTA)
  - > 100km^3 neutrino detectors
  - PID, Fast x-ray detectors

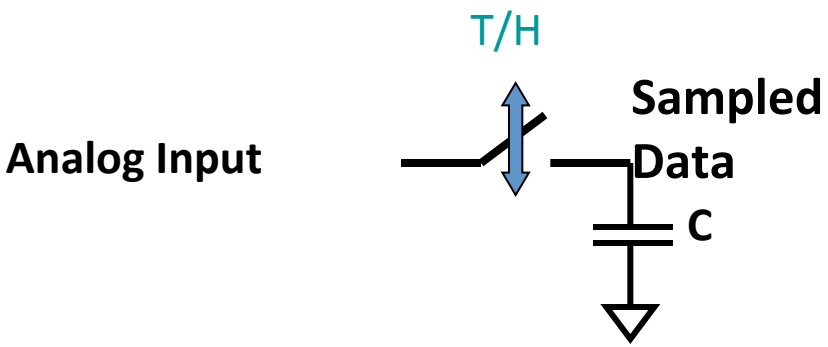


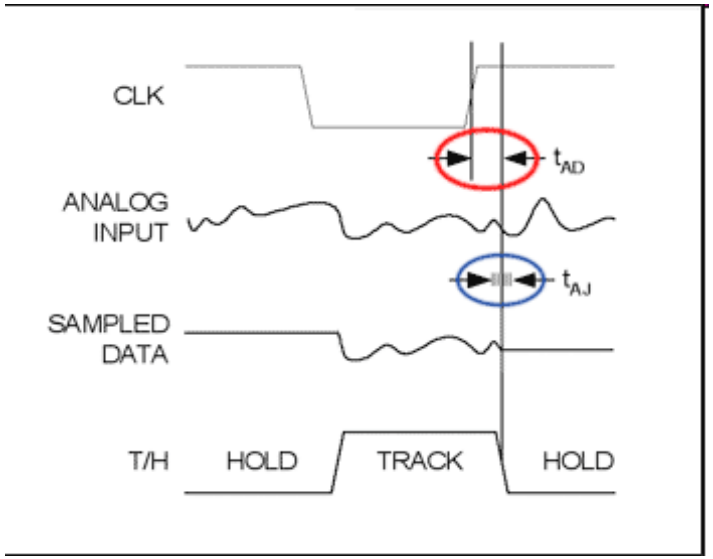
Back-up slides



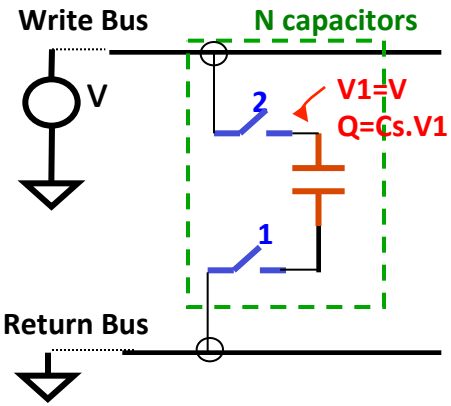
Underlying Technology

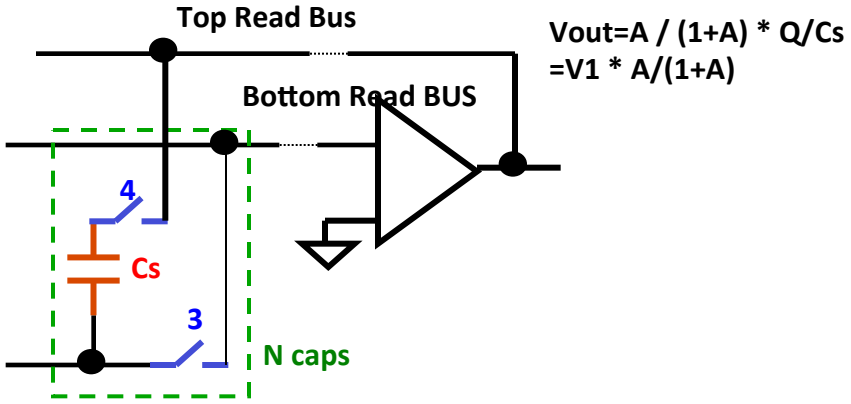
- Track and Hold (T/H)



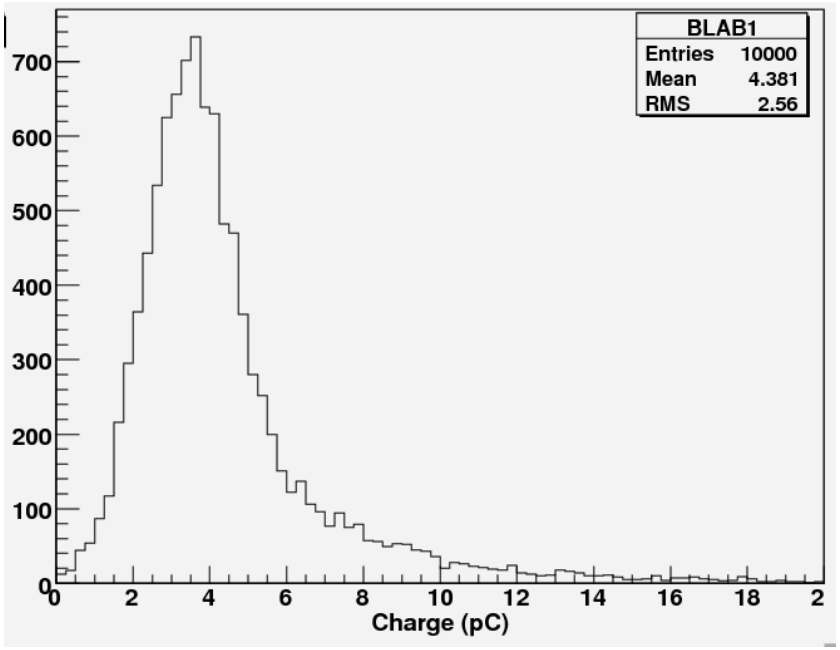


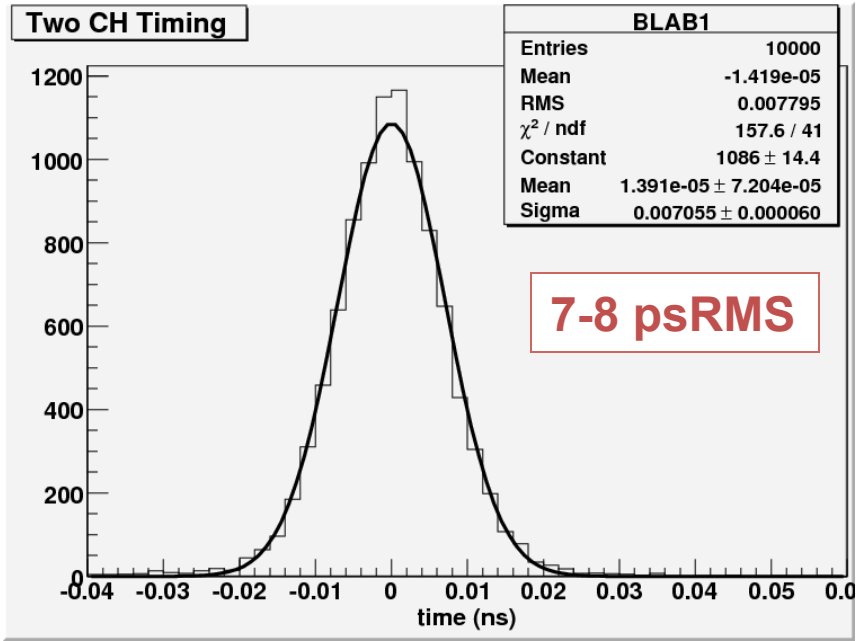
- Pipelined storage = array of T/H elements, with output buffering





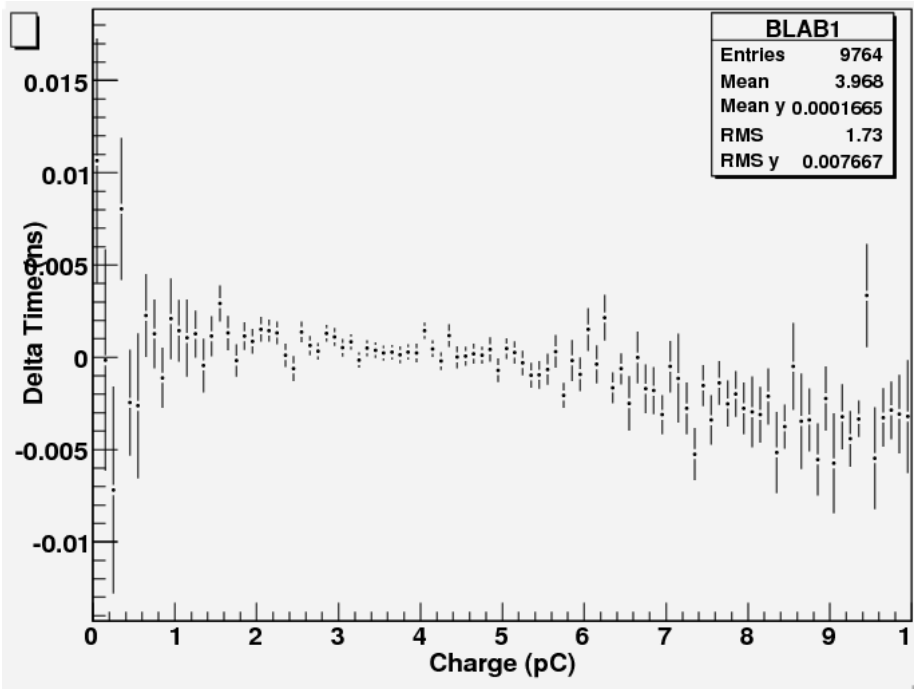
Real MCP-PMT Signals (with BLAB2)





7-8 psRMS

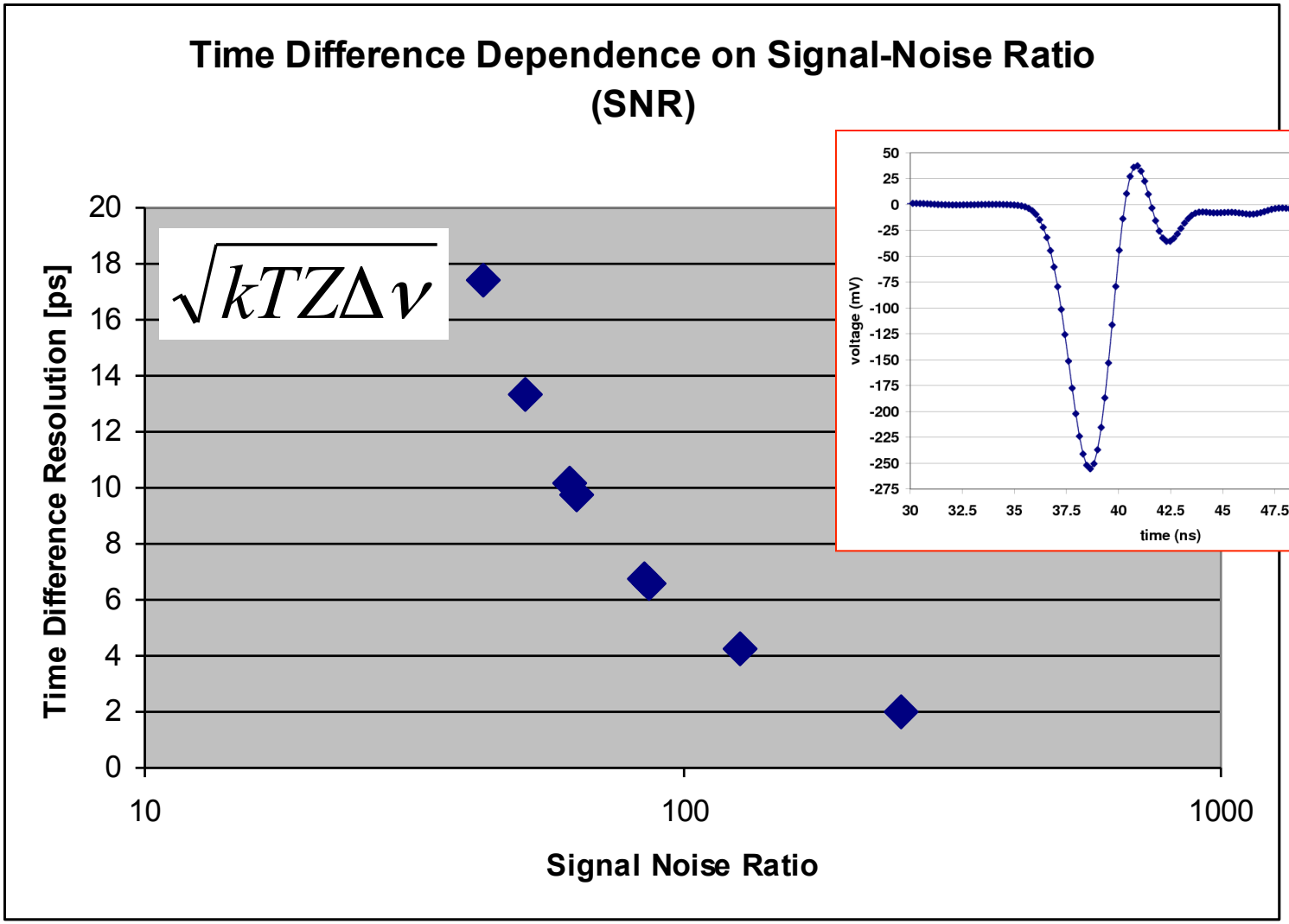
Residual Time Walk



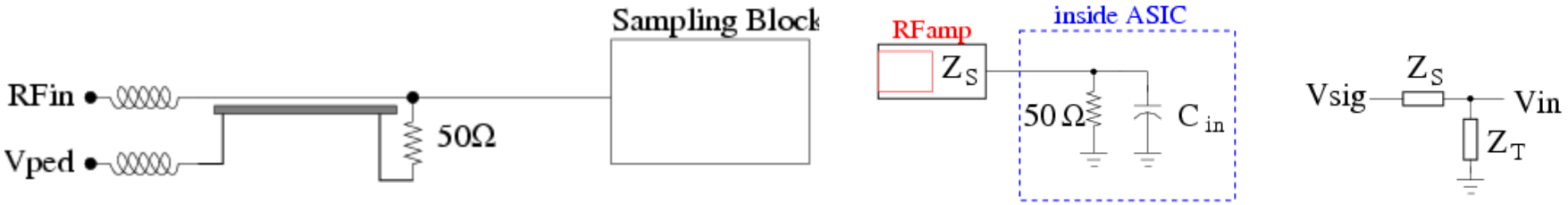
Rather robust for amplitude invariant signals,
TOF still hard, but can shape extract

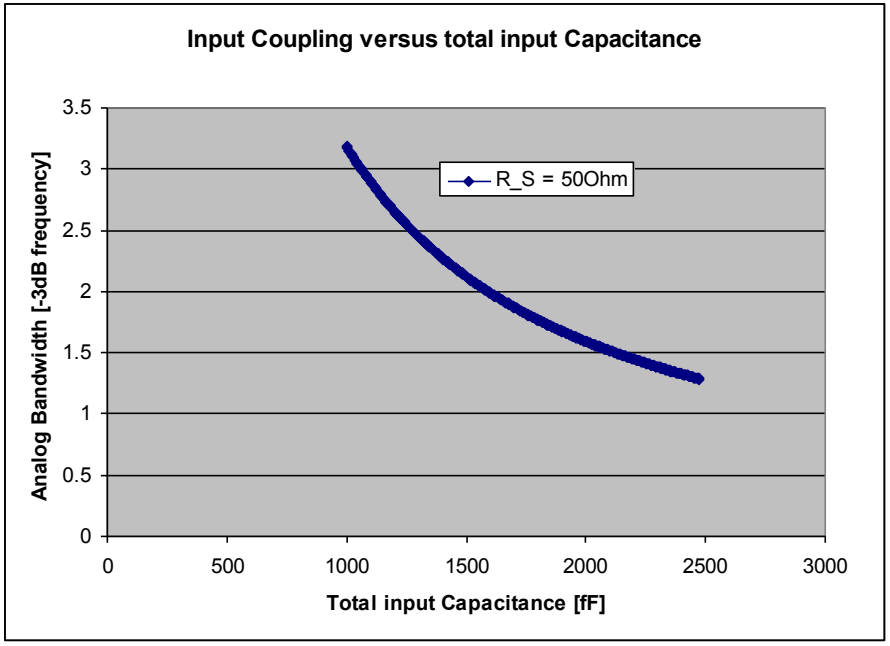
Simulated Performance vs. SNR

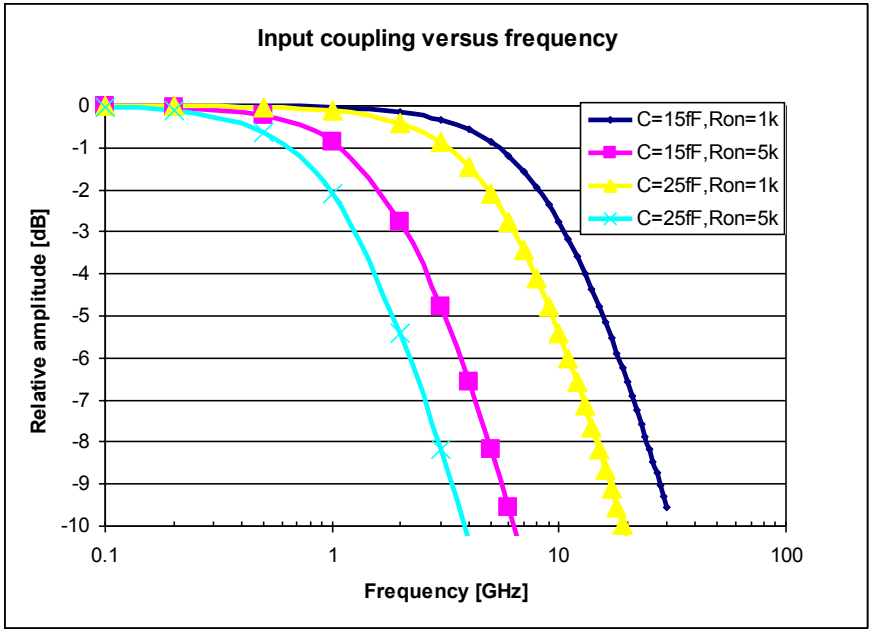
300MHz ABW, 5.9GSa/s



IRS Input Coupling

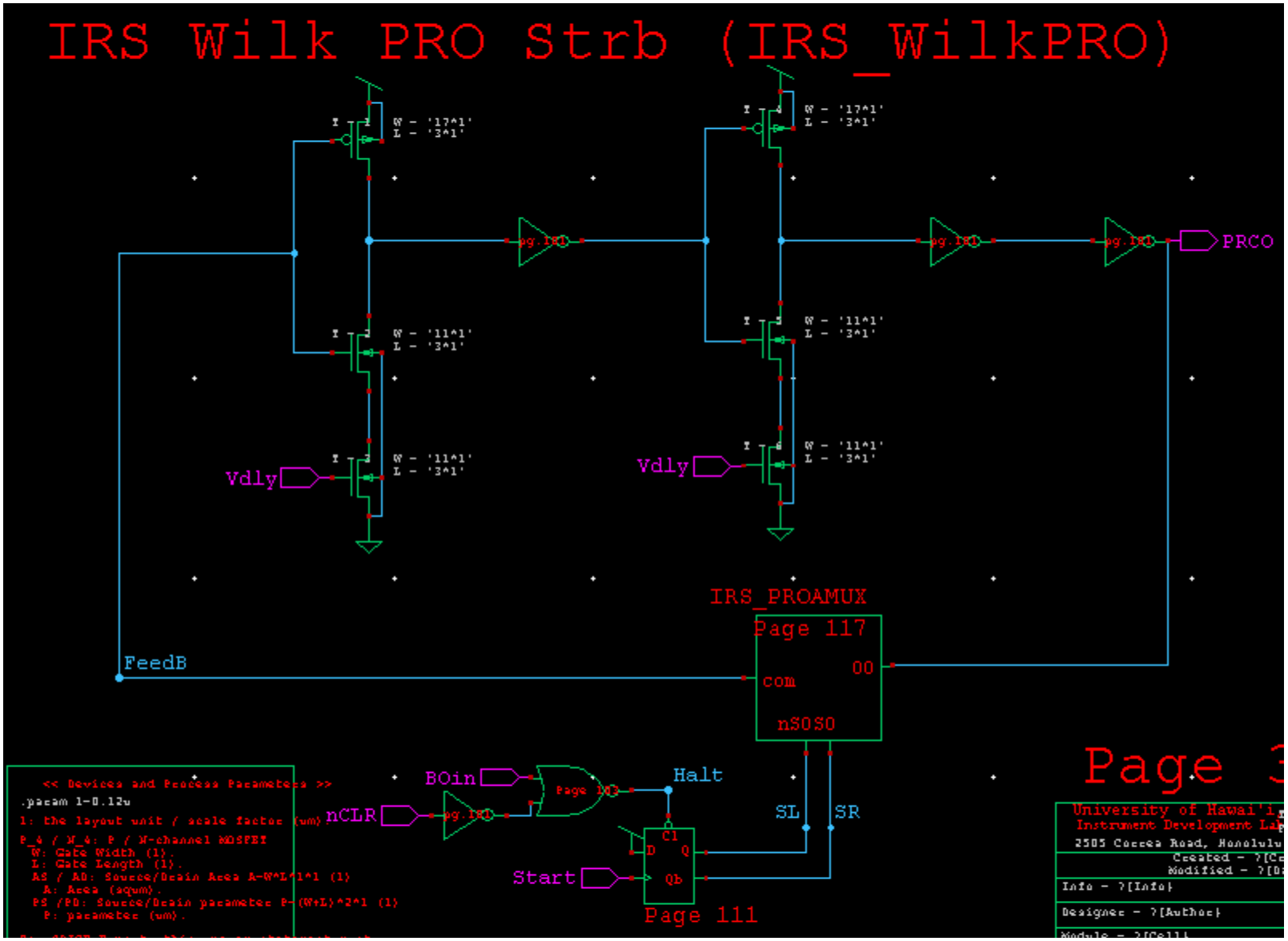




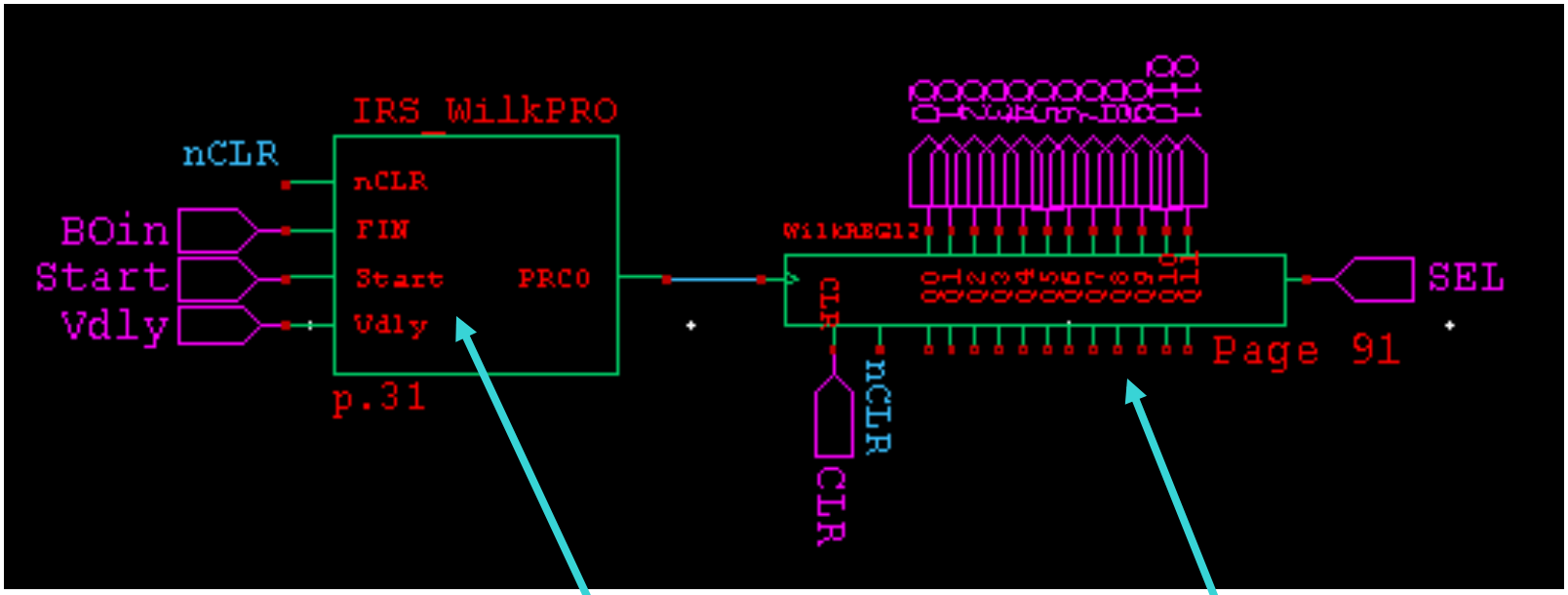


- Input bandwidth depends on 2x terms
  - $f3dB[input] = [2*\pi*Z*C_{tot}]^{-1}$
  - $f3dB[storage] = [2*\pi*R_{on}*C_{store}]^{-1}$

Wilkinson Clock Generation



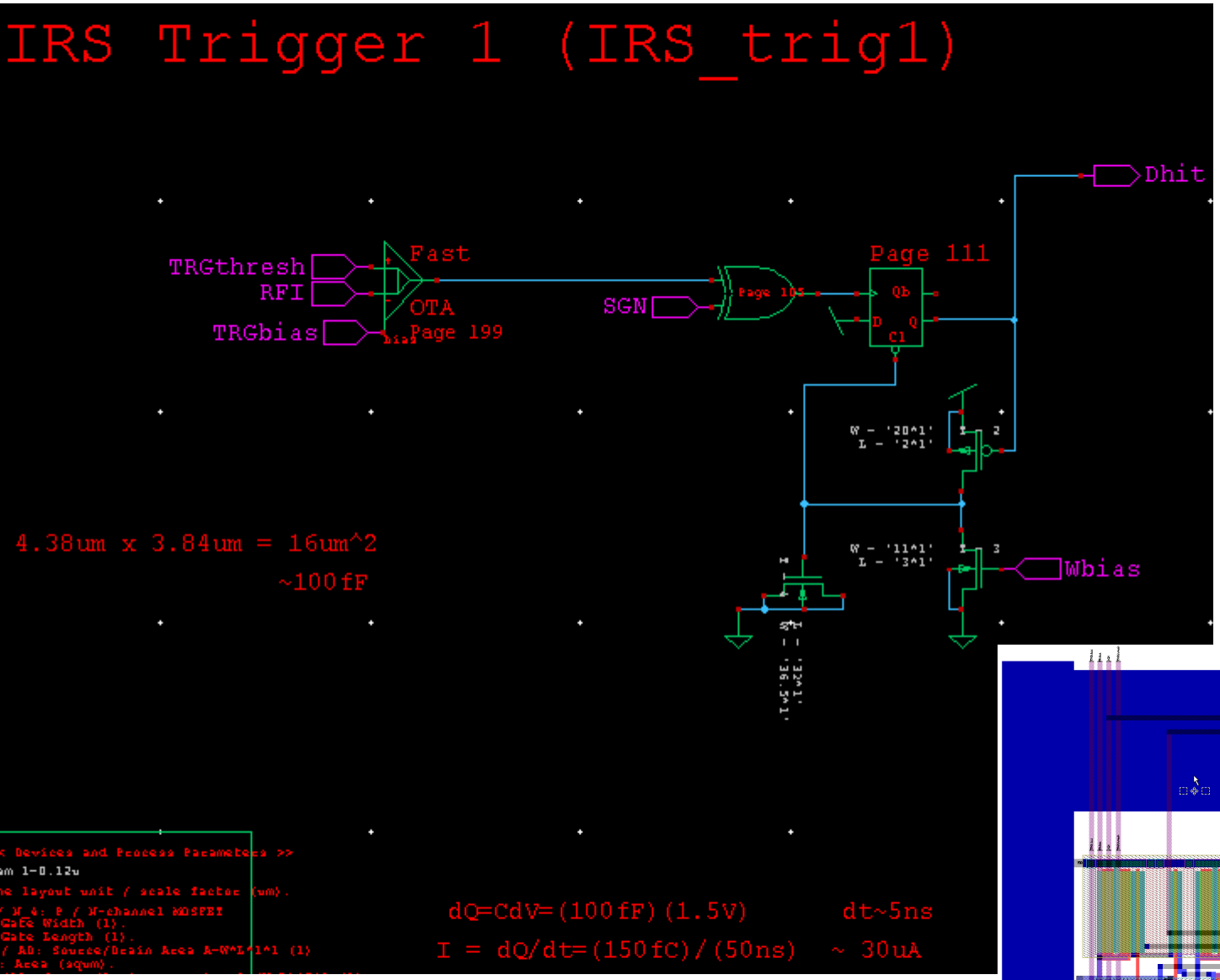
Wilkinson Recording

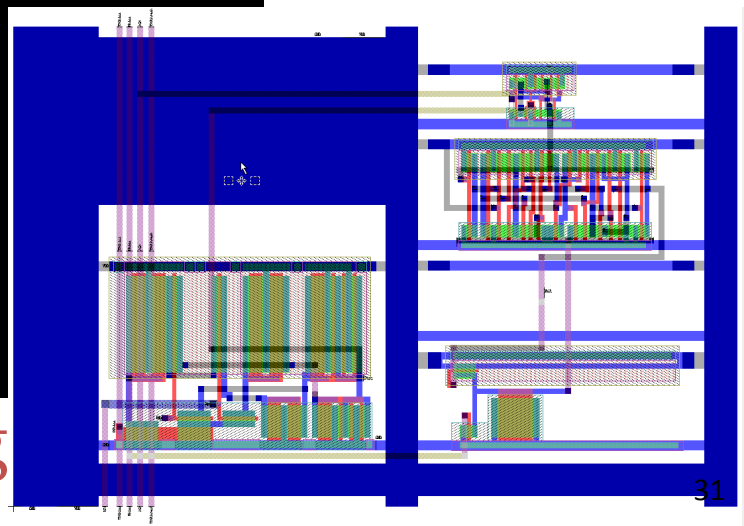


Start = start 0.5-1.5GHz Clock

Ripple counter (run as fast as can)

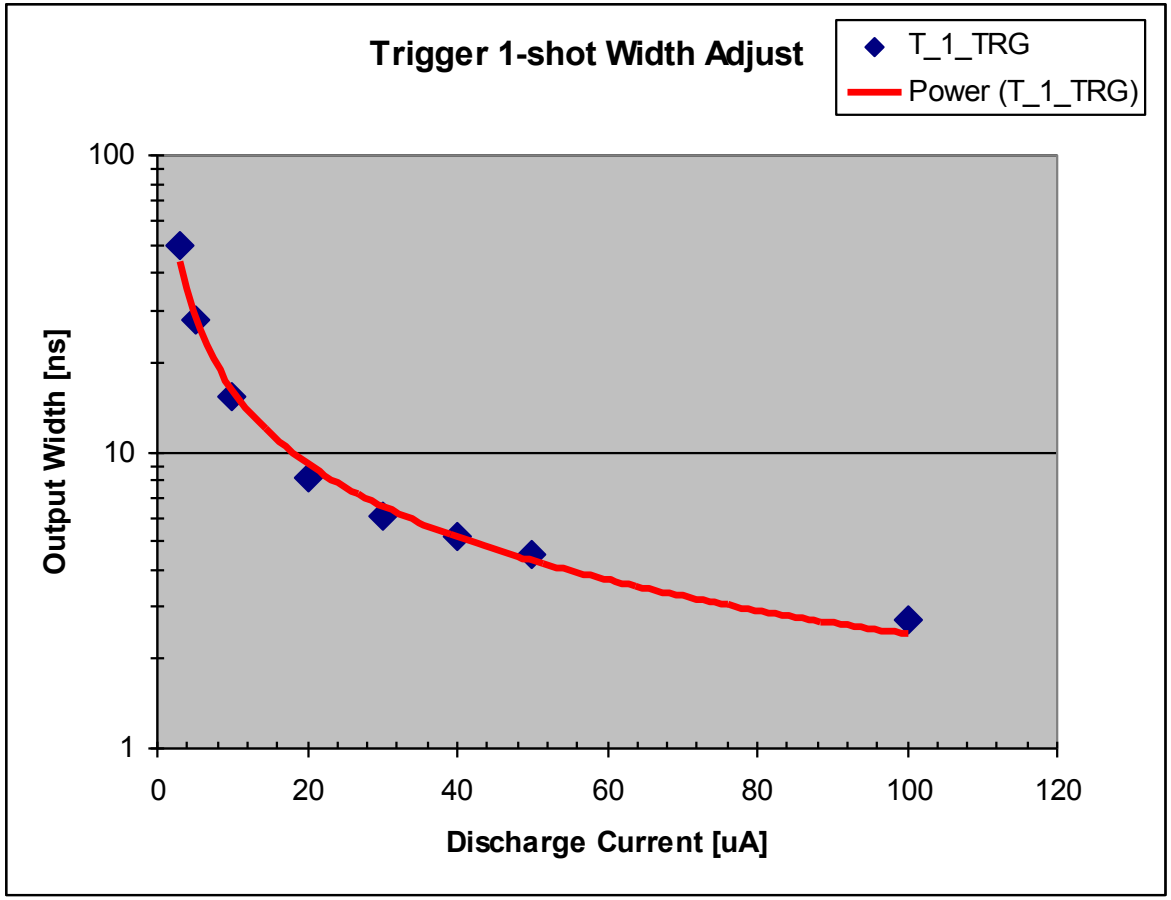
Triggering





- Need 9th channel for monitoring

Triggering – same as previous results

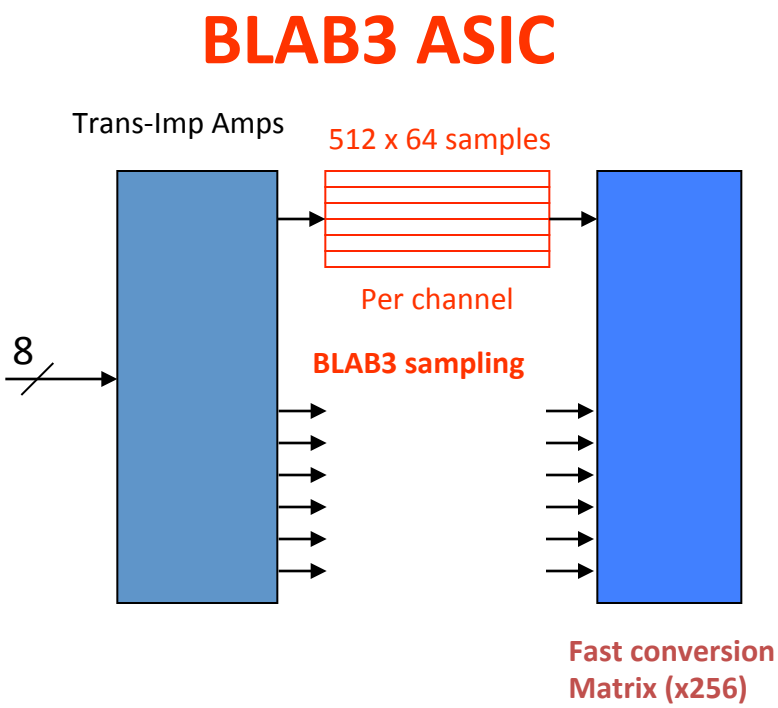


- Monitor 9th channel (uses Ch.1 threshold) to compensate for temperature dependence

Hit Processing numbers

Assume:
100kHz charged track hits on each bar

~32 p.e./track (1% of 100ns windows)
30kHz trigger rate
Each PMT pair sees <8> hits
240k hits/s
Each BLAB3 has an average occupancy <1 hit (assume 1)
400ns to convert 256 samples
16ns/sample to transfer
At least 16 deep buffering
(Markov overflow probability est. < 10^{-38})



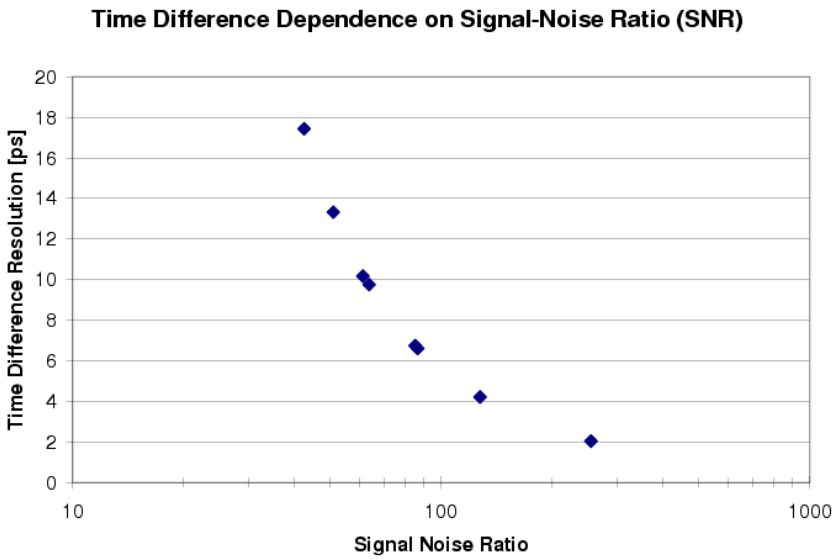
Each hit = 64samples * 8bits = 512bits
➔~125Mbits/s
(link is 3.0 Gb/s ~ x30 margin)

Improvements based upon
Lessons learned from BLAB2

Plan to model in standard queuing simulator, but looks like no problem
(CF have done same exercise with Jerry Va'vra for 150kHz L1 of SuperB and can handle rate)

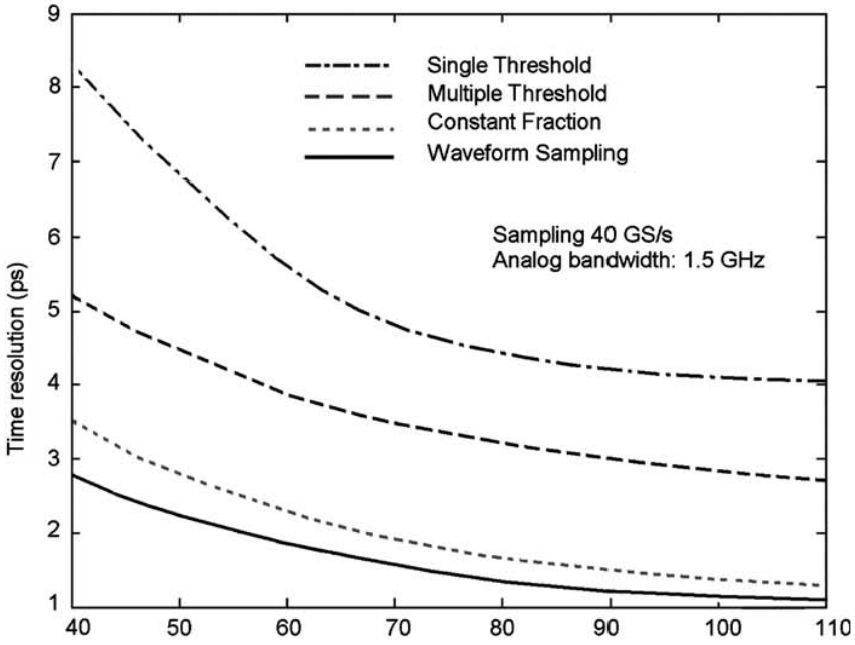
Front-end Electronics studies

1GHz analog bandwidth, 5GSa/s



G. Varner and L. Ruckman
NIM A602 (2009) 438-445.

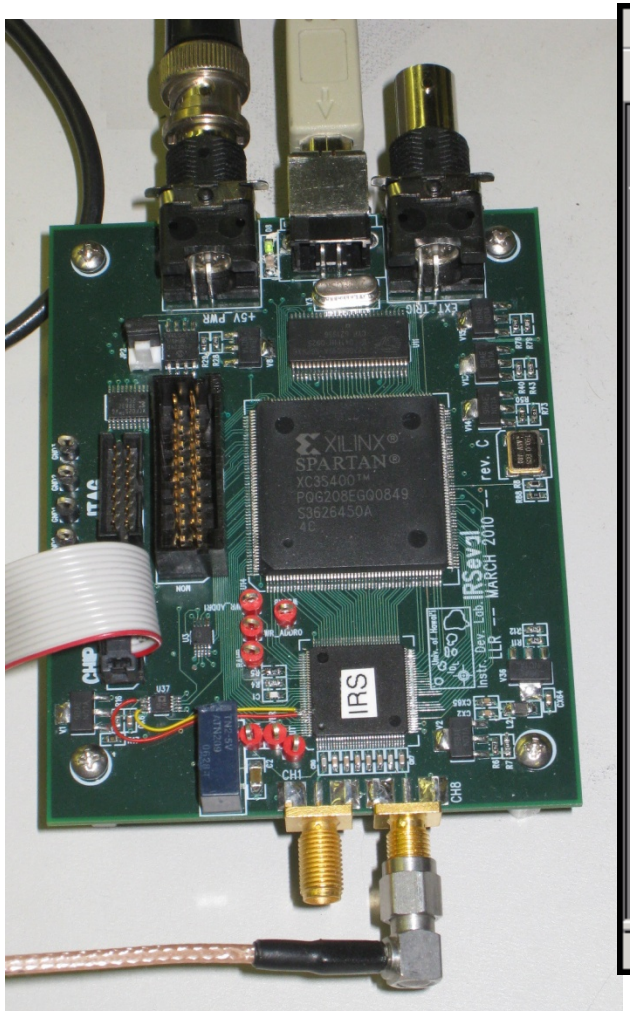
Simulation includes detector response

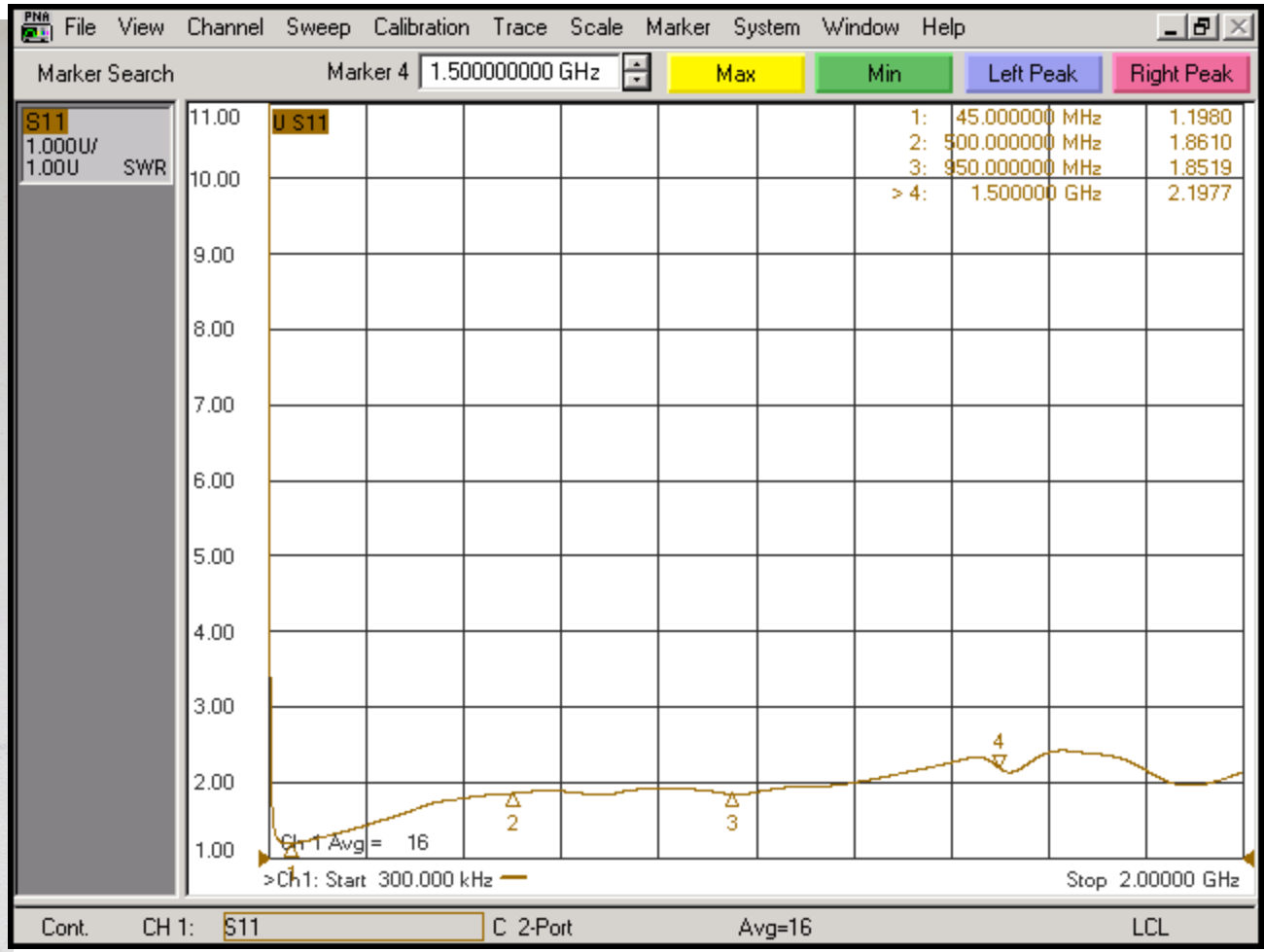


J-F Genat, G. Varner, F. Tang, H. Frisch
NIM A**607 (2009) 387-393**.

Ice Radio Sampler (IRS)

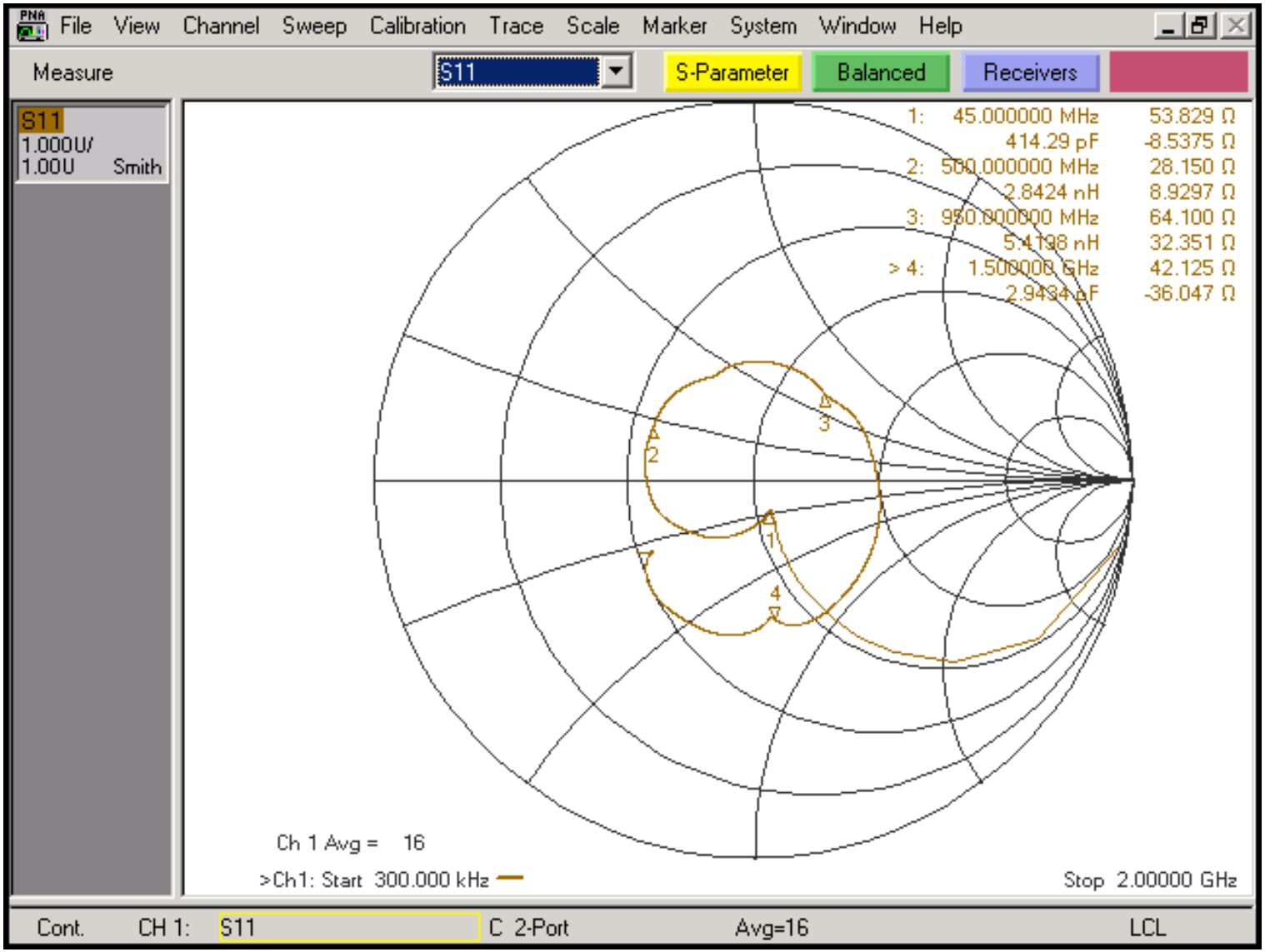
RF input coupling (S11)





P. Gorham -- measurement

Ice Radio Sampler (IRS)



P. Gorham -- measurement

WFS Evolution and Philosophy

- SAM
  1. Maximize dynamic range and minimize signal distorsion.
  2. Minimize need for calibrations and off-chip data corrections.
  3. Minimize costs (both for development & production)

- DRS family
  - Get a solid, general design working
  - Something that can work, in volume, for many apps

- LAB and siblings (6→8 generations)
  - Continue to explore parameter space
  - Concentrate on applications where more general solutions above many not be best choice

Approaches very complementary

References

- PSI activities (DRS)
  - IEEE/NSS 2008, TIPP09
  - **http://midas.psi.ch/drs**
- DAPNIA activities
  - MATDAQ: *IEEE TNS 52-6:2853-2860,2005 / Patent WO022315*
  - SAM; *NIM **A567** (2006) 21-26.*
- Hawaii activities
  - STRAW: Proc. SPIE 4858-31, 2003.
  - PRO: JINST, Vol. **3**, P12003 (2008).
  - LABRADOR: NIM **A583** (2007) 447-460.
  - BLAB: NIM **A591** (2008) 534-545; NIM **A602** (2009) 438-445.
  - STURM: EPAC08-TUOCM02, June, 2008.