Introduction

On October 27, 2012, a meeting was held at the University of Chicago to discuss desired specifications and possible architectures for a PSEC-5 ASIC. The following individuals participated in this meeting:

- Andrey Elagin, University of Chicago
- Henry Frisch, University of Chicago
- Craig Harabedian, University of Chicago
- Mary Heintz, University of Chicago
- Kurtis Nishimura, University of Hawaii
- Eric Oberla, University of Chicago
- Larry Sadwick, InnoSys Inc.
- Gary Varner, University of Hawaii
- Alexander Vostrikov, University of Chicago
- Bob Wagner, Argonne National Lab
- Bill Worstell, Photo Diagnostic Systems

The PSEC-5 is the successor to the PSEC-4 ASIC, which provides concrete proof-of-principle that delay-line-based waveform sampling and digitizing ASICs can operate at speeds in excess of 10 gigasamples-per-second with analog bandwidth well in excess of 1 GHz. Such an ASIC is an important step toward picosecond precision systems, and PSEC-4-based electronics have been developed to read out LAPPD tiles and SuperModules.

Despite this success, the collaboration recognizes that the PSEC-4 has limitations which may not make it usable in some applications, particularly those that require deeper buffering of data to accommodate long trigger latencies or high event rates while maintaining deadtimeless acquisition. The PSEC-5, then, should build off of the proven technologies of PSEC-4, while adding these features to make it suitable for the target applications.

We discussed a number of applications where LAPPD SuperModules and the PSEC-5 might be considered, and used these to determine some target specifications for the PSEC-5. Wherever possible, we identified the architecture for various PSEC-5 blocks. In some cases, such design decisions must be guided by further trade studies. This document summarizes the potential target applications, known specifications, and the remaining studies to be performed.

All materials presented at the meeting are available at the following link:

https://lappd-trac.uchicago.edu/wiki/Electronics/Agendas/PSEC-5_kickoff_meeting

Applications

A number of potential applications were discussed:

- Time-of-Flight Positron Emission Tomography (TOF PET)
- Large Water Cherenkov Detector
- Precision Time-of-Flight for a Hadron Collider
- Preshower Calorimeter for a Rare Kaon Decay Experiment

Estimates of specifications for these applications are posted as part of the meeting slides, and we cover only the summary of these discussions here.

The latter three applications are specifically identified as excellent candidates for a PSEC-5 readout. Specifically, their trigger latencies are ≤ 8 μs, with maximum L1 trigger rates ≤ 200 kHz. They all benefit from excellent timing resolution, with the collider TOF and preshower calorimeter pressing for the best possible timing resolutions, toward the single picosecond level. Because the focus on fast timing compliments the groundwork that has been laid with the PSEC-4, these application studies are used to guide the baseline PSEC-5 specifications.

As discussion of the TOF PET application progressed, it was determined that the requirements are unique enough to merit a separate readout, possibly with a dedicated custom ASIC. In particular, TOF PET requires both excellent timing (on the ~20 picosecond level), while maintaining sensitivity to the slow component of the scintillation light yield. In BaF_2, for example, a readout window of hundreds of nanoseconds is desired. This slow readout could be implemented at a much lower sampling rate, and could digitize an integrated signal rather than the raw MCP output. This significant difference in requirements motivated the decision to treat this application separately, with a dedicated meeting to be scheduled in the future.

PSEC-5 Baseline Specifications

The baseline PSEC-5 specifications are given in the following table.

Specification	Baseline Value
Fabrication process & feature size	IBM 130 nm
Channels per ASIC	4
Nominal sampling rate	10 GSa/s
Timebase stabilization method	On-chip DLL
Analog bandwidth	> 1.0 GHz
Length of sampling array	128 or 256 samples
Trigger latency accommodated[1]	8 μs
Absolute minimum buffer depth	100 ns [1000 samples @ 10 GSa/s]
Buffering style	Multi-stage transfer to analog storage; ≥ 1 stage digital buffering
Digitization style	Wilkinson ADC
Number of bits	12
Readout interface	Serial LVDS
Channel-level trigger capability	1 bit / channel

<Add a description of the architecture with a block diagram?>

[1] Note that the trigger latency that can be accommodated is a function of the buffer depth, occupancy, storage scheme, and system trigger rate. The given 8 μs number should be re-evaluated as the design continues to ensure that it is obtainable given further application specifications.

In an effort to decide on the specifics of the PSEC-5 interface, we have drafted the following draft list of PSEC-5 inputs and outputs.

Signal	Number	Type	Comments
Input signals	4	Analog inputs	
Pedestal levels	4	Analog inputs	Baseline voltage for each channel.
Serial I/O clock	1	Digital input	Interface to DACs and internal registers. This is an "SPI" style interface, as a placeholder, but other interfaces could be explored.
Serial I/O data in	1	Digital input	
Serial I/O data out	1	Digital output	
Serial I/O chip select	1	Digital input	
DAC monitoring	1?	Analog output	Monitors an internal DAC voltage. Exact DAC selectable via serial interface?
Wilkinson ramp start	1	Digital input	Initiates Wilkinson ramp.
Wilkinson counter clear	1	Digital input	Clears Wilkinson registers.
Wilkinson ramp monitor	1	Analog output	Allows monitoring of Wilkinson ramp signal.
Wilkinson ramp capacitor	1	Analog input	Connection to capacitor charged up during Wilkinson ramp.
Wilkinson counter Monitor	1	Digital output	Allows verification of Wilkinson clock running, monitoring for feedback on clock rate.
Delay line input	1	Digital input	Input clock – sampling rate / # of sampling cells.
Delay line output	1	Digital output	Output clock
DLL locked	1	Digital output	Indicates whether DLL has successfully locked.
DLL reset	1	Digital input	Resets the DLL.
DLL VDD	1	Supply/Ground	Independent 1.2 V VDD for DLL.
VCP	1	Analog output	Feedback voltages sent to the delay line. These are the outputs from the charge pump. Die pins allow for extra capacitance to integrate charge.
VCN	1	Analog output	
Trigger Bits Out	4	Digital output	One per channel
Data out – LVDSp	1?	LVDS output	Assuming a single LVDS pair as a primary serial readout. Could add parallel pairs, if desired.
Data out – LVDSn	1?	LVDS output	
Data clock – LVDSp	1?	LVDS output	Assumes a source synchronous model, but could be changed to inputs if FPGA will supply clock.
Data clock – LVDSn	1?	LVDS output	
LVDS VDD		Supply/Ground	2.5 V supply voltage for LVDS
LVDS GND		Supply/Ground	Could tie all grounds together.
Analog VDD		Supply/Ground	1.2 V analog supply voltage
Analog GND		Supply/Ground	Could tie all grounds together.
Digital VDD		Supply/Ground	1.2 V digital supply voltage
Digital GND		Supply/Ground	Could tie all grounds together.

The following are internal registers that will likely need to be accommodated:

Register	Number	Number Bits	Comments
DAC levels – trigger thresholds	4	12?	
DAC level – trigger bias	1	12?	
DAC level – ramp bias	1	12?	
DAC level – ring oscillator bias	2	12?	Controls Wilkinson count rate.
DAC level – transfer buffer bias	2	12?	Number of biases required depends on number of stages in the transfer.
DAC level – trigger width adjust	1	12?	Controls width of trigger bits out.
DAC levels – sampling rate trim	128/256?	12?	Bias voltages could be implemented, one per sampling cell, to trim out the non-uniform sampling rates. See design study list for more details.
DAC level – DLLn	1	12?	Charge pump bias voltages.
DAC level – DLLp	1	12?	
DAC level – DLL_pol	2	12?	Bias current for rising/falling edge charge pumps. May switch from 2 to 1.
Trigger polarity	1	1	Could also be variable by channel?
DAC Monitoring	1?	?	Digital multiplexer select to choose which internal DAC to monitor, if desired. See design study list for more details.

Summary of Further Studies Required

The following items have been flagged for further study or simulation.

Overarching Issues

- **Fabrication process** – The existing PSEC series has been fabricated in the IBM 130 nm CMOS process. This process is currently limited to four MOSIS multi-project wafer runs per year, and has typically had a relatively slow turnaround time. TSMC also offers a 130 nm process, which could be considered for PSEC-5. The TSMC process has monthly submissions through MOSIS and may be more economical for larger orders. However, it would require significant effort to redesign structures for the TSMC process, as the design kits and design rules are incompatible between the two systems. Further, the minimum cost of a die submission is larger, due to a significantly larger minimum size than the IBM process. This has a potential impact on the feasibility of smaller submissions consisting of mostly test structures. We tentatively assume that we will transfer to the TSMC process. This issue may be addressed again as the design studies mature.

Sampling

- **Current noise source** – What is the current dominant noise source in the PSEC-4? Is it consistent with kTC noise? This will be investigated by taking noise measurements at various temperatures with the existing PSEC-4 hardware.
- **Number of sampling cells vs. analog bandwidth** – What is the appropriate number of sampling cells? Is it possible to improve the analog bandwidth by moving from 256 sampling cells to 128 cells? This can be studied by simulating the analog bandwidth with a shorter storage array.
- **On-chip DLL** – The existing on-chip DLL of the PSEC-4 has proven to be quite useful in stabilizing the timebase. This could be reused in the PSEC-5, but the following changes should be studied:
    1. Use of an earlier or adjustable pickoff point for the feedback. The existing DLL feeds back based on the signal from the end of the delay line. This pickoff is effectively too late in the chain, and causes an excess delay of many effective sample lengths when wrapping around from sample 255 to sample 0. This creates a brief gap in the sampling record, which should be avoided.
    2. Addition of diagnostic outputs to determine the status of the DLL. For example, even a single digital output to indicate when the DLL is “locked” could be a very useful feature.

Storage

- **Multi-stage transfer scheme** – It was determined that a multi-stage transfer scheme is ideal for the targeted applications. However, the details of exactly how many stages and how they are implemented need further clarification. This study may include the following:
    1. Internally generated logic to control all or part of the transfer. Given the high sampling rate of the system, controlling all aspects of the transfer for a large number of ASICs with a single FPGA may be troublesome. The IRS3B ASIC, developed in Hawaii, has

demonstrated that some of these controls can be absorbed into the internal logic, while still allowing fine control of the timing via digital registers inside the ASIC. Such a scheme could be employed in the PSEC-5, and results of ongoing IRS3B testing will be useful for identifying potential implementations and improvements.

2. The number of stages of the transfer. This is intimately related to the previous point, as the timing margins required at each step depend on how many samples are being transferred at once, and between which stages. A large number of stages increases the complexity, but allows for more relaxed control at each successive stage.
3. The buffering implementation relative to the channel-level trigger bits. It is anticipated that there will not be enough storage space to sample continuously for the entire length of the trigger latency. Rather, windows can be moved to analog storage when channel-level trigger bits indicate that there is a signal of interest. Details such as the number and relative timing of which windows to store when a trigger bit fires should be considered.

- **Storage cell size, buffer depth, and number of channels** – The compactness of the storage cells and the total number of storage cells and input channels directly impacts the size, and therefore cost, of fabrication. A study must be performed that estimates the smallest practical size of a storage cell. Once this is known, tradeoffs between the number of channels and total buffer depth can be analyzed.
- **Reset stage/logic before transferring to storage** – To ensure that transfers to storage are performed in a repeatable manner, and to avoid imprints of previous stored voltages in the storage array, it is proposed that a "reset" stage be applied to each storage window before the signal voltages are written to its cells. This reset mechanism must be designed and simulated.

Digitization

- **Distributed Gray code counter** – It is observed across a number of ASICs, including PSEC-4, that the power draw increases dramatically when the digitization block is run. This is in part attributed to the activation of a ripple oscillator per digitization cell that is activated upon the start of the Wilkinson ADC process. This instantaneous increase in power can cause instabilities in power and ground of the ASIC, resulting in apparent discontinuities in sampled data coincident with the start of such a cycle. One proposed method to handle this problem is to run a single distributed Gray code counter to all digitization cells. This counter could be left on all the time in order to maintain a stable power level. To implement such a scheme would require design of a Gray code counter, evaluation of the speed at which such a counter could run, design of a Gray decoder, and integration into a modified Wilkinson scheme.

General Control

- **Internal DACs** – A 12-bit DAC has been demonstrated in multiple ASICs fabricated in IBM 130 nm CMOS. Adding DACs can decrease the number of auxiliary components required to support ASIC operation, so these could be considered for the PSEC-5, wherever possible.

- **Trim DACs** – If the DACs mentioned above can be made compact enough, it may be possible to add a DAC stage for each sample delay in the delay line. These "trim DACs" can be used to effectively remove the non-uniform effects of delay line sampling. This could be a tremendous benefit to downstream processing, either in an FPGA, DSP, or offline, as it would effectively remove or mitigate the need for precise timing calibrations. This is being prototyped on the LAB4B ASIC in Hawaii, and results of this testing can guide the decision to add such trim DACs to PSEC-5.
- **DAC monitoring** – Some functionality for monitoring internal DAC performances may be desired. For example, an analog multiplexer could be implemented that allows selection of a DAC to output to a monitor pin. Alternatively, key DAC voltages could be output to separate pins to allow measurement of DAC performance in addition to the possibility of overriding the internal DACs with external control voltages. Specifics can be determined as the design matures and critical control voltages are identified.

Control and Readout Interfaces

- **Serial control** – The current PSEC-4 requires a number of digital I/O pins to control the operation of the chip. Can and should these be streamlined into a serial control mechanism, such as SPI (or similar)?
- **LVDS serial readout** – A bottleneck of current throughput with the PSEC-4 involves the readout style, in which the user supplies a readout address, and the data is presented on a parallel bus of single-ended signals. To improve the speed and/or reduce the number of I/Os required for readout, it could be advantageous to move to serial LVDS data stream. The following issues are identified as requiring further study: design of the LVDS transmitters, number of serial streams per ASIC, encoding schemes, and implementation of training patterns.

Miscellaneous Issues

- **CHAMP2** – The Chicago Hawaii ASIC, Multi-Purpose (CHAMP) was fabricated in 2010-2011 as a joint project between the University of Chicago and the University of Hawaii. This ASIC consisted of a number of test structures in IBM 130 nm CMOS, and allowed prototyping of various structures, including delay lines operating in excess of 18 GSa/s and a functional 12-bit DAC. Further, it was an excellent vehicle to introduce a number of graduate students to the basics of ASIC design. A future submission, CHAMP2, could be considered next year, where test structures such as a distributed Gray code counter, serial links, or others, could be prototyped. As design studies for PSEC-5 continue, candidate structures for such a prototype submission should be identified. If the TSMC 130 nm process is ultimately decided upon for PSEC-5, a CHAMP2 ASIC may need to be funded via other external funding.