

Future Developments in Gigasample-per-second Waveform Sampling Application Specific Integrated Circuits

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Time Frame: Intermediate term

Physics Justification: Modern high energy physics and astrophysics experiments are increasingly making use of waveform sampling (WFS) technologies. In contrast to previous generations of readout electronics where one TDC and one ADC value might be stored per channel, recording full waveforms allows experimenters to perform real-time or offline digital signal processing, pulse shape analysis, cross-talk correction, and precision timing extraction. While many experiments can utilize commercial digitizers (typically flash ADCs), such components may not be viable if the experiment calls for some combination of multi-GSa/s sampling rates, low-power, or very high channel density.

Custom WFS ASICs fill this void in the available portfolio of front-end readout electronics. Such ASICs provide a novel approach to meeting these experimental challenges. They are capable of analog sampling at rates of several GSa/s to over 10 GSa/s at power levels of tens of mW per channel during sampling. The input analog bandwidths of these ASIC designs span a range of ~100 MHz to over 1 GHz.

Such electronics are already in use at the cosmic [1-3], intensity [4-5], and instrumentation [6] frontiers. For example, this technology has served as the key enabling component for the ANITA experiment's search for ultra-high energy cosmogenic neutrinos, due to its tightly constrained power budget and its need for timing resolutions at the ~10 ps level [7].

The cost of WFS ASICs is also relatively low, from tens or hundreds of dollars per channel in prototype quantities, down to a few dollars per channel when produced in large quantities.

Technical limitations:

The current generation of WFS ASICs have several technical challenges. Two of the primary design challenges are presented:

1) *Buffer Depth:* These waveform samplers are effectively 'analog down-conversion' devices, in which a waveform is recorded at a rate of several-GSa/s and data is read off-chip at a slower rate, typically ~10-100 MHz. Several designs incorporate an on-chip ADC that adds an intermediate latency step. Therefore, the 'event' waveform sample depth is limited by the on-chip buffering architecture.

Many of these custom WFS ASICs are limited to short buffer depths, typically less than 1 μ s, and in some cases as short as 25 ns. These ASICs are usually operated in a triggered mode, in which a system trigger initiates conversion and data readout. This experimental trigger latency sets the minimum required buffer depth of the front-end WFS ASIC.

WFS ASIC designs with very deep buffers, up to tens of microseconds, are currently being investigated. While this promises the possibility of accommodating long trigger latencies and effectively dead time-less operation below a given event rate, this gain may be offset by an increased nonlinearity, more calibration constants, higher power, and increased die size.

2) *Calibrations:* The typical technique of using delay lines to generate the fast effective sampling rates imposes a large number of timing calibration constants on the data from these ASICs. These calibrations must be performed if optimal timing resolution is to be obtained. While techniques exist to deal with these issues, they impose a significant burden on the analysis of such data.

Other calibrations, such as nonlinearity and pedestal corrections, are also required for optimal ASIC performance. Though these calibrations are relatively straightforward, the number of calibration constants will scale with the increased ASIC analog buffer.

Technical Capabilities: A few programs in the US are actively involved in designing and characterizing fast WFS ASICs. Most development is centered around expertise at LBNL / UC Irvine, the University of Chicago, and the University of Hawaii. Fabrication of ASICs is typically brokered through MOSIS, either through multi-project wafers for prototype runs, or dedicated runs for larger quantities.

Key R&D Directions: Continued work is required to fully characterize the tradeoffs that are available in terms of sampling rates, buffer depths, power consumption, and other features. The first long buffer depth (many μ s) WFS ASICs are being developed for experiments that will begin within the next few years.

There is an ongoing effort targeted at developing calibration and characterization techniques for these ASICs. This work is particularly important, as it dramatically reduces a significant barrier to entry for those interested in adopting fast waveform sampling technology for their experiments.

A further evolutionary step would be to build in features to these ASICs that can perform calibration at the hardware level, thus allowing downstream systems to deal with a significantly simplified data stream. This work is just beginning, and if successful, could dramatically widen the potential applications for these ASICs.

Additional developers of WFS ASICs, support electronics, and calibration systems that can be implemented in hardware and software, would be particularly helpful to ensure that these developments can be fully explored and realized in a timely manner.

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