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A 15 GSa/s, 1.5 GHz bandwidth waveform digitizing ASIC

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ABSTRACT

The PSEC4 custom integrated circuit was designed for the recording of fast waveforms for use in large-area time-of-flight detector systems. The ASIC has been fabricated using the IBM-8RF 0.13 μm CMOS process. On each of the six analog channels, PSEC4 employs a switched capacitor array (SCA) of 256 samples deep, a ramp-compare ADC with 10.5 bits of DC dynamic range, and a serial data readout with the capability of region-of-interest windowing to reduce dead time. The sampling rate can be adjusted between 4 and 15 Gigasamples/second (GSa/s) on all channels and is servo-controlled on-chip with a low-jitter delay-locked loop (DLL). The input signals are passively coupled on-chip with a −3 dB analog bandwidth of 1.5 GHz. The power consumption in quiescent sampling mode is less than 50 mW/chip; at a sustained trigger and a readout rate of 50 kHz the chip draws 100 mW. After fixed-pattern pedestal subtraction, the uncorrected integral non-linearity is 0.15% over a 750 mV dynamic range. With a linearity correction, a full 1 V signal voltage range is available. The sampling timebase has a fixed-pattern non-linearity with an RMS of 13%, which can be corrected for precision waveform feature extraction and timing.

1. Introduction

We describe the design and performance of PSEC4, a ≥10 Gigasample/second (GSa/s) waveform sampling and digitizing application specific integrated circuit (ASIC) fabricated in the IBM-8RF 0.13 μm complementary metal-oxide-semiconductor (CMOS) technology. This compact 'oscilloscope-on-a-chip' is designed for the recording of radio-frequency (RF) transient waveforms with signal bandwidths between 100 MHz and 1.5 GHz.

1.1. Background

The detection of discrete photons and high-energy particles is the basis for a wide range of commercial and scientific applications. In many of these applications, the relative arrival time of an incident photon or particle is best measured by extracting features from the full waveform at the detector output [1,2]. Additional benefits of front-end waveform sampling include the detection of pile-up events and the ability to filter noise or poorly formed pulses.

For recording 'snapshots' of transient waveforms, switched capacitor array (SCA) analog memories can be used to sample a limited time-window at a relatively high rate, but with a latency-cost of a slower readout speed [3,4]. These devices are well suited for triggered-event applications, as in many high energy physics experiments, in which some dead-time on each channel is acceptable. With modern CMOS integrated circuit design, these SCA sampling chips can be compact, low power, and have a relatively low cost per channel [4].

Over the last decade, sampling rates in SCA waveform sampling ASICs have been pushed to several GSa/s with analog bandwidths from several hundred MHz up to ~1 GHz [5,6]. As a scalable front-end readout option coupled with the advantages of waveform sampling, these ASICs have been used in a wide range of experiments; such as high-energy physics colliders [6], gamma-ray astronomy [7,8], high-energy neutrino detection [9,10], and rare decay searches [11,12].

1.2. Motivation

A natural extension to the existing waveform sampling ASICs is to push design parameters that are inherently fabrication-technology limited. Parameters such as sampling rate and analog bandwidth are

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of particular interest considering the fast risetimes ($\tau_r \sim 60$–500 ps) and pulse widths (FWHM ~ 200 ps–1 ns) of commercially available and novel technologies of micro-channel plate (MCP) and silicon photomultipliers [13–15]. These and other fast photo-optical or RF devices require electronics matched to the speed of the signals.

The timing resolution of discrete waveform sampling is intuitively dependent on three primary factors as described by Ritt[4] [16]:

$$\sigma_t \propto \frac{\tau_r}{(SNR)\sqrt{N_{samples}}} \quad (1)$$

where *SNR* is the signal-to-noise ratio of the pulse, τ_r is the 10–90% rise-time of the pulse, and $N_{samples}$ is the number of independent samples on the rising edge within time τ_r. The motivation for oversampling above the Nyquist limit is that errors due to uncorrelated noise, caused by both random time jitter and charge fluctuations, are reduced by increasing the rising-edge sample size. Accordingly, in order to preserve the timing properties of analog signals from a fast detector, the waveform recording electronics should (1) be low-noise, (2) match the signal bandwidth, and (3) have a fast sampling rate relative to the signal rise-time.

1.3. *Toward* 0.13 μm *CMOS*

The well-known advantages of reduced transistor feature size include higher clock speeds, greater circuit density, lower parasitic capacitances, and lower power dissipation per circuit [17]. The sampling rate and analog bandwidth of waveform sampling ASICs, which depend on clock speeds, parasitic capacitances, and interconnect lengths, are directly enhanced by moving to a smaller CMOS technology. Designing in a smaller technology also allows clocking of an on-chip analog-to-digital converter (ADC) at a faster rate, reducing the chip dead-time.

With the advantages of reduced transistor feature sizes also comes increasingly challenging analog design issues. One issue is the increase of leakage current. Leakage is enhanced by decreased source-drain channel lengths, causing subthreshold leakage ($V_{GS} < V_{TH}$), and decreased gate-oxide thickness, which promotes gate-oxide tunneling [18]. Effects of leakage include increased quiescent power dissipation and potential non-linear effects when storing analog voltages.

Another design issue of deeper sub-micron technologies is the reduced dynamic range [18]. The available voltage range is given by (V_{DD}–V_{TH}), where V_{DD} is the supply voltage and V_{TH} is the threshold, or 'turn-on', voltage for a given transistor. For technologies above 0.1 μm, the (V_{DD}–V_{TH}) range is decreased with downscaled feature sizes to reduce high-field effects in the gate-oxide [18]. In the 0.13 μm CMOS process, the supply voltage V_{DD} is 1.2 V and the values of V_{TH} range from 0.42 V for a minimum-size transistor (gate length 120 nm) to roughly 0.2 V for a large transistor (5 μm) [19,20].

The potential of waveform sampling design in 0.13 μm CMOS was shown with two previous ASICs. A waveform sampling prototype, PSEC3, achieved a sampling rate of 15 GSa/s and showed the possibility of analog bandwidths above 1 GHz [21]. Leakage and dynamic range studies were also performed with this chip. In a separate 0.13 μm ASIC, fabricated as a test-structure chip called CHAMP, a 25 GSa/s sampling rate was achieved using low V_{TH} transistors [22]. The performance and limitations of these chips led to the optimized design of the PSEC4 waveform digitizing ASIC. The fabricated PSEC4 die is shown in Fig. 1.

In this paper, we describe the PSEC4 architecture (Section 2) and experimental performance (Section 3).

[4] Assuming Shannon–Nyquist is fulfilled.

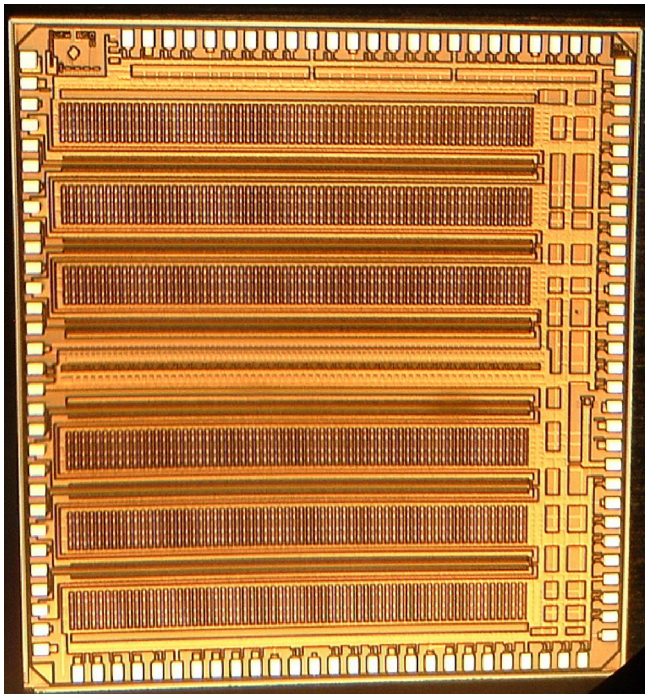

Fig. 1. Photograph of the fabricated PSEC4 die. The chip dimensions are 4×4.2 mm^2.

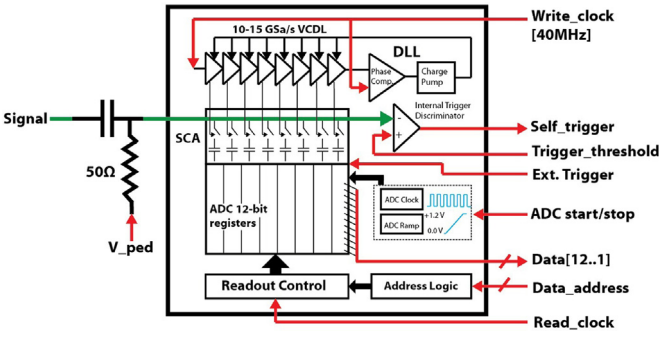

Fig. 2. A block diagram of PSEC4 functionality. The RF-input signal is AC coupled and terminated in 50 Ω off-chip. The digital signals (listed on right) are interfaced with an FPGA for PSEC4 control. A 40 MHz write clock is fed to the chip and up-converted to ~10 GSa/s with a 256-stage voltage-controlled delay line (VCDL). (For clarity, only 8 of the 256 cells and 1 of the 6 channels are illustrated.) A 'write strobe' signal is sent from each stage of the VCDL to the corresponding sampling cell in each channel. The write strobe passes the VCDL-generated sampling rate to the sample-and-hold switches of each SCA cell. Each cell is made from a switched capacitor sampling cell and an integrated ADC counter, as shown in Fig. 3. The trigger signal ultimately comes from the FPGA, in which sampling on every channel is halted and all analog samples are digitized. The on-chip ramp-compare ADC is run with a global analog ramp generator and 1 GHz clock which are distributed to each cell. Once digitized, the addressed data are serially sent off-chip on a 12-bit bus clocked at up to 80 MHz.

2. Architecture

An overview of the PSEC4 architecture and functionality is shown in Fig. 2. A PSEC4 channel is a linear array of 256 sample points and a threshold-level trigger discriminator. Each sample point in the array is made from a switched capacitor sampling cell and an integrated ADC circuit as shown in Fig. 3.

To operate the chip, a field-programmable gate array (FPGA) is used to provide timing control, clock generation, readout addressing, data management, and general configurations to the ASIC. Several analog voltage controls are also required for operation, and are provided by commercial digital-to-analog converter (DAC) chips.

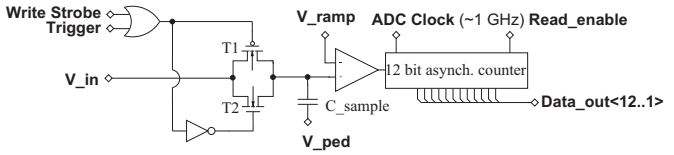

Fig. 3. Simplified schematic of the 'vertically integrated' PSEC4 cell structure. The sampling cell input, V_{in}, is tied to the on-chip 50 Ω input microstrip line. Transistors T1 and T2 form a dual-CMOS write switch that facilitates the sample-and-hold of V_{in} on C_{sample}, a 20 fF capacitance referenced to *V_ped*. The switch is toggled by the VCDL write strobe while sampling (Fig. 2) or an ASIC-global trigger signal when an event is to be digitized. When the ADC is initiated, a global 0.0–1.2 V analog voltage ramp is sent to all comparators, which digitizes the voltage on C_{sample} using a fast ADC clock and a 12-bit counter. To send the digital data off-chip, the register is addressed using *Read_enable*.

Further details of the chip architecture, including timing generation (Section 2.1) sampling and triggering (Section 2.2), analog-to-digital conversion (Section 2.3), and data readout (Section 2.4) are outlined in the following sections.

2.1. Timing generation

The sampling signals are generated with a 256-stage voltage-controlled delay line (VCDL), in which the individual stage time delay is adjustable by two complementary voltage controls. There is a single VCDL that distributes the timing signals to the entire chip. Each stage in the VCDL is an RC delay element made from a CMOS current-starved inverter. The inverse of the time delay between stages sets the sampling rate. Rates of up to 17.5 GSa/s are possible with PSEC4 as shown in Fig. 4. When operating the VCDL without feedback, the control voltage is explicitly set and the sampling rate is approximately given by

$$18 - 0.3e^{6 \cdot V_{control}} \ (\mathrm{GSa/s}). \tag{2}$$

Typically, the servo-locking will be enabled and the VCDL is run as a delay-locked loop (DLL). In this case, the sampling rate is automatically set by the input write clock frequency. The stability of the sampling rate is negatively correlated with the slope magnitude as the VCDL becomes increasingly sensitive to noise. The slowest stable sampling rate is ~ 4 GSa/s.

A 'write strobe' signal is sent from each stage of the VCDL to the corresponding sampling cell in each channel. The write strobe passes the VCDL-generated sampling rate to the sample-and-hold switch of the cell as shown in Fig. 3. To allow the sample cell enough time to fully charge or discharge when sampling, the write strobe is extended to a fixed duration of $8\times$ the individual VCDL delay stage. In a sampling mode, a 'sampling block' that made of eight adjacent SCA sampling cells continuously tracks the input signal.

To servo-control the VCDL at a specified sampling rate and to compensate for temperature effects and power supply variations, the VCDL can be delay-locked on chip. The VCDL forms a delay-locked loop (DLL) when this servo-controlled feedback is enabled. The servo-control circuit is made of a dual phase comparator and the charge pump circuit to lock both the rising and falling edges of the write clock at a fixed one-cycle latency [23]. A loop-filter capacitor is installed externally to tune the DLL stability.

With this DLL architecture, a write clock with frequency f_{in} is provided to the chip, and the sampling is started automatically after a locking time of several seconds. The nominal sampling rate in GSa/s is set by $0.256 \cdot f_{in}$ (MHz), and the sampling buffer depth in nanoseconds is given by $10^3/f_{in}$ (MHz^{-1}). A limitation of the PSEC4 design is the relatively small recording depth at high sampling rates due to the buffer size of 256 samples.

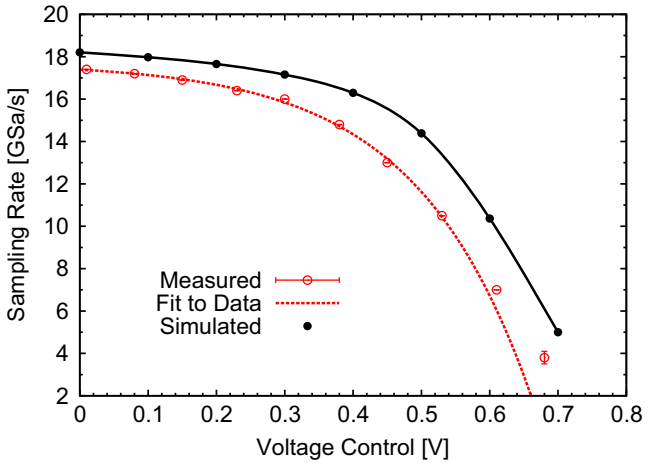

Fig. 4. Sampling rate as a function of VCDL voltage control. Good agreement is shown between post-layout simulation and actual values. Rates up to 17.5 GSa/s are achieved with the free-running PSEC4 VCDL.

2.2. Sampling and triggering

A single-ended, 256-cell SCA was designed and implemented on each channel of PSEC4. Each sampling cell circuit is made from a dual CMOS write switch and a metal–insulator–metal sampling capacitor as shown in Fig. 3. With layout parasitics, this capacitance is effectively 20 fF. During sampling, the write switch is toggled by the write strobe from the VCDL. To record an event, an external trigger, typically from an FPGA, overrides the sampling and opens all write switches, holding the analog voltages on the capacitor for the ADC duration ($\lesssim 4$ μs). Triggering interrupts the sampling on every channel, and is held until the selected data are digitized and read out. When triggered, the sampling is asynchronously halted. This corrupts the voltage on the seven sample cells that were in the process of sampling, reducing the effective number of PSEC4 samples to 249.

The PSEC4 has the capability to output a threshold-level trigger bit on each channel. The internal trigger is made from a fast comparator, which is referenced to an external threshold level, and digital logic to latch and reset the trigger circuit. To form a PSEC4 trigger, the self-trigger bits are sent to the FPGA, which returns a global trigger signal back to the chip. In the internal trigger mode, the trigger round-trip time is 15–20 ns (depending on the FPGA algorithm), which allows for the recording of a waveform before it is overwritten at 10 GSa/s.

2.3. ADC

Digital conversion of the sampled waveforms is done on-chip with a single ramp-compare ADC that is parallelized over the entire ASIC.[5] Each sample cell has a dedicated comparator and a 12 bit counter as shown in Fig. 3. In this architecture, the comparison between each sampled voltage (V_{sample}) and a global ramping voltage (V_{ramp}) controls the clock enable of a 12-bit counter. When $V_{ramp} > V_{sample}$, the counter clocking is disabled, and the 12-bit word, which has been encoded by the ADC clock frequency and the ramp duration below V_{sample}, is latched and ready for readout.

Embedded in each channel is a five-stage ring oscillator that generates a fast digital ADC clock, adjustable between 200 MHz and 1.4 GHz. The ADC conversion time, power consumption, and resolution may be configured by adjusting the ramp slope or by tuning the ring oscillator frequency.

[5] An overview of this ADC architecture can be found in Ref. [24].

2.4. Readout

The serial data readout of the latched counter bits is performed using a shift register 'token' architecture, in which a *read_enable* pulse is passed sequentially along the ADC counter array. To reduce the chip readout latency, a limited selection of the 1536 counters in PSEC4 can be read out. Readout addressing is done by selecting the channel number and a block of 64 cells. While not completely random access, this scheme permits a considerable reduction in dead time. At a maximum rate of 80 MHz, the readout time is 0.8 μs per 64-cell block.

The readout latency is typically the largest contributor to the dead-time of the chip. The ADC conversion time also adds up to 4 μs of latency per triggered event. These two factors limit the sustained trigger rate to ~200 kHz/channel or ~50 kHz/chip.

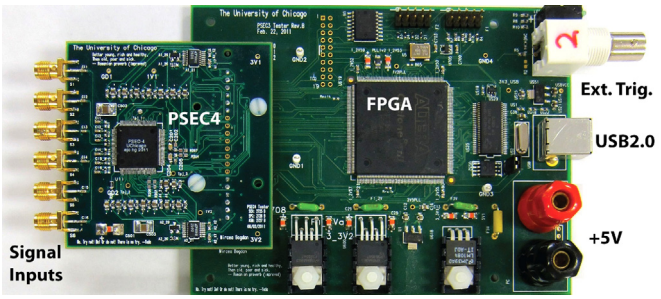

Fig. 5. The PSEC4 evaluation board. The board uses a Cyclone III Altera FPGA (EP3C25Q240) and a USB 2.0 PC interface. Custom firmware and acquisition software were developed for overall board control. The board uses +5 V power and draws <400 mA, either from a DC supply or the USB interface.

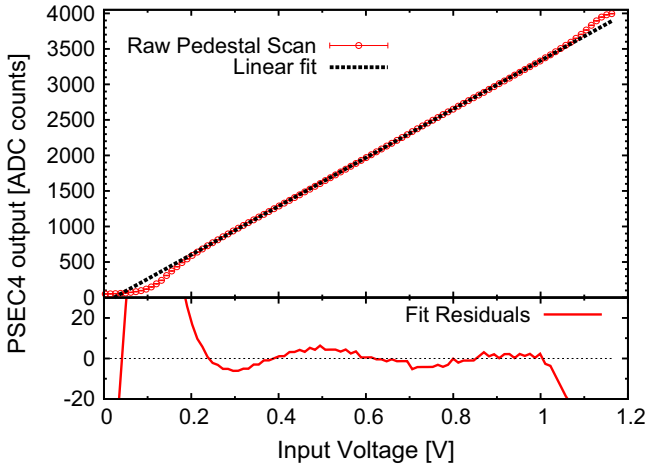

Fig. 6. DC response of the device running in 12 bit mode. The data are an average response of all 256 cells from a single channel. The upper plot shows raw data (red points) and a linear fit over the same dynamic range (dotted black line, a slope of 4 counts/mV). The fit residuals are shown in the lower plot. (For interpretation of the references to color in this figure caption, the reader is referred to the web version of this article.)

3. Performance

Measurements of the PSEC4 performance have been made with several chips on custom evaluation boards shown in Fig. 5. The sampling rate was fixed at a nominal rate of 10.24 GSa/s. Here we report on bench measurements of linearity (Section 3.1), analog leakage (Section 3.2), noise (Section 3.3), power (Section 3.4), frequency response (Section 3.5), sampling calibrations (Section 3.6), and waveform timing (Section 3.7). A summary table of the PSEC4 performance is shown in Section 3.8.

3.1. Linearity and dynamic range

The signal voltage range is limited by the 1.2 V core voltage of the 0.13 μm CMOS process [19]. To enable the recording of signals

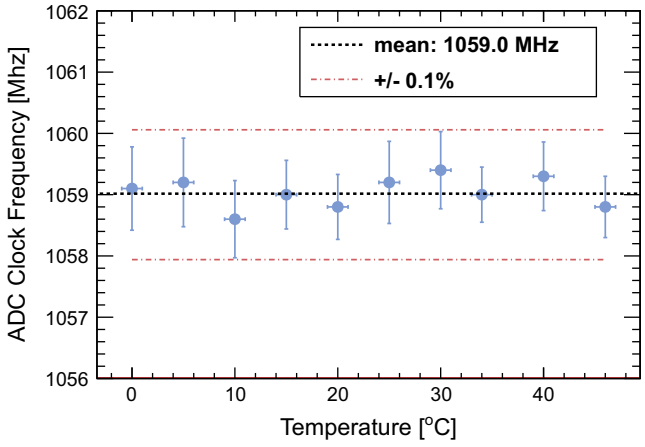

Fig. 8. Ring oscillator clock stability over temperature. This clock is stabilized with a servo-control algorithm in the FPGA that adjusts the DAC oscillator voltage controls. With this feedback, the ring oscillator frequency is held within 0.1% of the nominal 1.059 GHz over the tested temperature range.

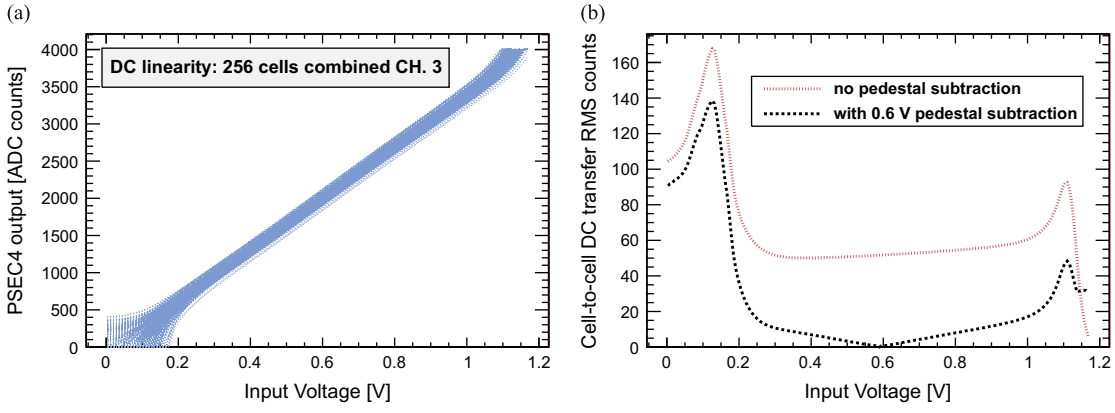

Fig. 7. (a) Raw DC scans for all 256 PSEC4 cells on a single channel. (b) RMS spread in ADC counts scanned over input voltage on a PSEC4 channel. A mid-range pedestal subtraction on each cell reduces the RMS/mean spread to ~1% over a 0.8 V range.

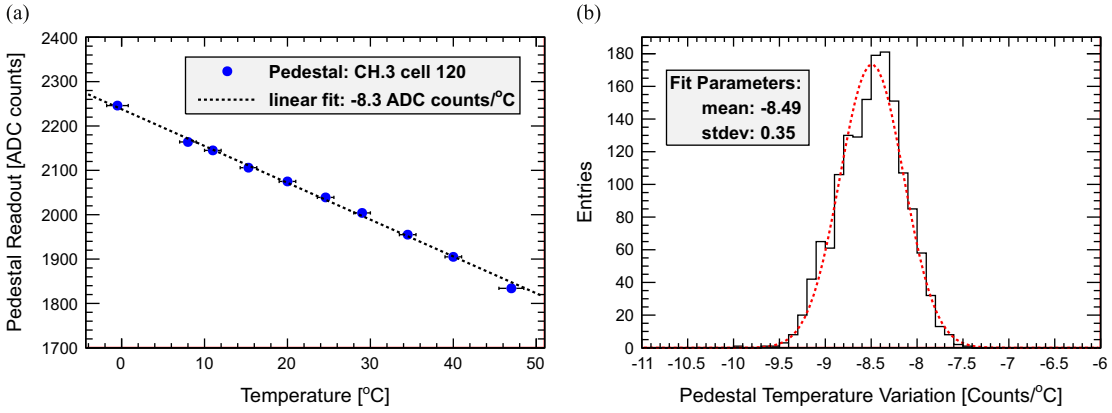

Fig. 9. (a) Temperature dependance of the pedestal level of a single cell. The data are consistent with a linear change in the pedestal level over temperature. (b) Distribution of pedestal-temperature variations over entire chip. The pedestal-temperature trend is consistent to 4% over all 1536 cells of a PSEC4 chip.

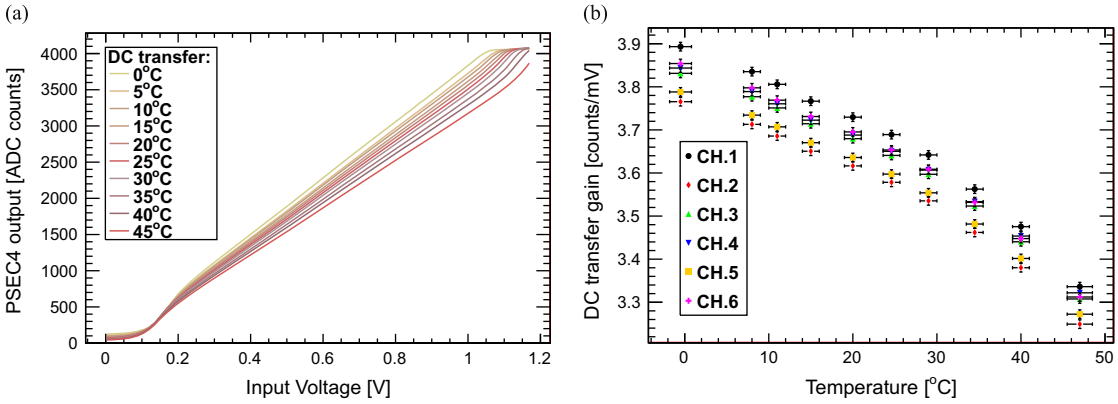

Fig. 10. (a) Average DC response of a single PSEC4 channel over a temperature range of 0 °C–45 °C. (b) The extracted DC transfer gains as a function of temperature for all channels.

with pedestal levels that exceed this range, the input is AC coupled and a DC offset is added to the 50 Ω termination. This is shown in Fig. 2 block diagram, in which the DC offset is designated by *V_ped*. The offset level is tuned to match the input signal voltage range to that of PSEC4.

The PSEC4-channel response to a linear pedestal scan is shown in Fig. 6. This is the average DC response over all 256 cells in a channel. A signal voltage range of 1 V is shown, as input signals between 100 mV and 1.1 V are fully coded with 12 bits. An integral non-linearity (INL) of better than 0.15% is shown for most of that range. The non-linearity and limited DC signal range near the voltage rails are due to transistor threshold issues in the comparator circuit.

The DNL of this response, shown by the linear fit residuals in Fig. 6, can be corrected by creating an ADC count-to-voltage look-up-table (LUT) that maps the input voltage to the PSEC4 output code. The raw PSEC4 data are converted to voltage and 'linearized' with a channel-averaged LUT.

Further linearity calibrations can be implemented to correct for cell-to-cell gain variations. A display of raw linearity scans over cells in a single channel is shown in Fig. 7. After a cell pedestal subtraction, the RMS cell-to-cell gain dispersion is $\sim 1\%$ over a 0.8 V range. Over this range, a single count-to-voltage LUT per channel may be sufficient. To effectively use the entire PSEC4 DC dynamic range, a count-to-voltage conversion LUT should be implemented for each individual cell.

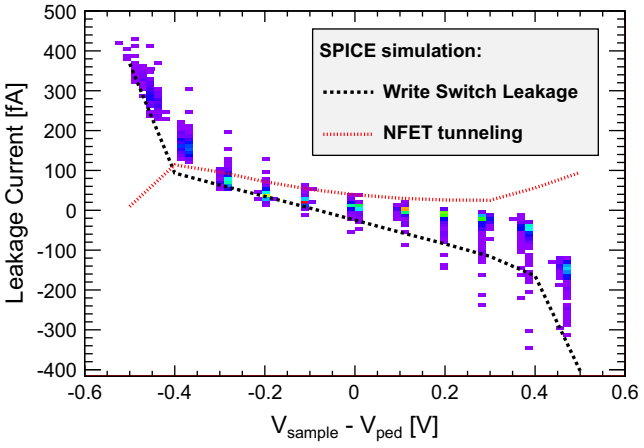

Fig. 11. PSEC4 sample cell leakage measured at room temperature. The measured leakage is shown by the histogrammed data points. Results from a 0.13 μm CMOS SPICE simulation are also included. The simulation shows the leakage current contributions from (1) sub-threshold conduction through the disengaged write switch and (2) gate-oxide tunneling from the NFET in the input stage of the comparator.

3.1.1. *Temperature dependance*

The ring oscillator ADC clock is the most temperature sensitive circuit and is servo-controlled using the FPGA to better than 0.1% over a wide temperature range as shown in Fig. 8. The ADC clock frequency was measured using 50k events at each temperature. Other temperature sensitive circuitries, including the chip-global ramp generator, are not feedback controlled.

The mid-range cell pedestal temperature dependence is shown in Fig. 9a. Pedestal levels are computed for each cell by recording the average ADC baseline over several readouts. The pedestal variation

is consistent with a linear trend of ~ 8.5 ADC counts/°C. This trend is common to all cells in PSEC4 as shown in Fig. 9b. A simple event baseline subtraction can correct for this effect with 4% accuracy.

The count-to-voltage transfer also shows temperature variation due to changes in the ADC ramp slope. The average DC transfer curves at different temperatures are shown in Fig. 10a. The count-per-voltage gain is extracted from a fit to the linear region of the DC transfer curve and is plotted in Fig. 10b. Since the ADC ramp is common to all channels, the average DC transfer gains of all channels are observed to have the same temperature dependence. To mitigate this effect, a feedback loop that serves the ramp current source could be implemented.

3.2. Sample leakage

When triggered, the write switch on each cell is opened and the sampled voltage is held at high impedance on the 20 fF capacitor (Fig. 3). Two charge leakage pathways are present: (1) sub-threshold conduction through the write switch formed by transistors T1 and T2 and (2) gate-oxide tunneling through the NFET at the comparator input. The observable leakage current is the sum of these two effects.

To measure the leakage current, a 300 ns wide, variable-level pulse was sent to a single PSEC4 channel. Since the sampling window is 25 ns, each SCA cell sampled the transient level. After triggering, the sampled transient voltage was repeatedly digitized at 1 ms intervals and the change in voltage on the capacitor was recorded over a 10 ms storage-time.

The room temperature PSEC4 leakage current as a function of input voltage over the full 1 V dynamic range is shown in Fig. 11. A pedestal level of $V_{DD}/2 = 0.6$ V was set at the input. The measured leakage is shown in the 2-D histogram. A large spread (RMS ~ 70 fA) is seen at each voltage level. Results from a 0.13 μm CMOS SPICE simulation show that the write-switch leakage is the dominant pathway. A small amount (≤ 100 fA) of NFET gate-oxide tunneling is also consistent with the data.

In normal operation, the ADC is started immediately after a trigger is registered. In this case, the analog voltage hold time is limited to the ADC conversion time. Assuming a constant current, the leakage-induced voltage change is given by

$$\Delta V = \frac{I_{leakage}\Delta t}{C_{sample}} \tag{3}$$

where Δt is the ADC conversion time. With the maximum leakage current of ± 500 fA and a conversion time of 4 μs, ΔV is ± 100 μV. This value is at least $5\times$ lower than the electronics noise.

3.3. Noise

After fixed-pattern pedestal correction and event-by-event baseline subtraction, which removes low-frequency noise contributions, the PSEC4 electronic noise is measured to be ~ 700 μV RMS on all channels as shown in Fig. 12a. The noise level is consistently sub-mV over a ± 20 °C temperature range at around room temperature. Above ~ 20 °C, the electronics noise increases with temperature, which is consistent with the thermal noise expectation of $\sqrt{k_B T/C}$ (Fig. 12b). The noise figure is dominated by broadband thermal noise on the 20 fF sampling capacitor, which contributes 450 μV (RMS 60 electrons) at 300 K. Other noise sources include the ADC ramp generator and the comparator. The noise corresponds to roughly three least significant bits (LSBs), reducing the DC RMS dynamic range to 10.5 bits over the signal voltage range.

3.4. Power

The power consumption is dominated by the ADC, which simultaneously clocks 1536 ripple counters and several hundred large digital buffers at up to 1.4 GHz. The total power draw per chip as a function of ADC clock rate is shown in Fig. 13. To reduce

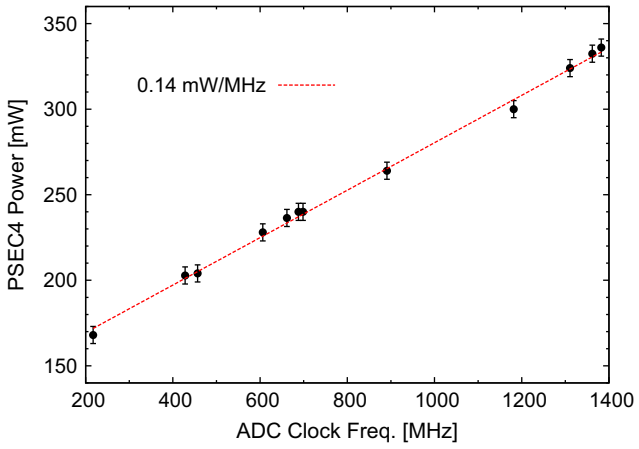

Fig. 13. Total PSEC4 power as a function of the ADC clock rate. Clock rates between 200 MHz and 1.4 GHz can be selected based on the power budget and targeted ADC speed and resolution. When the ADC is not running, the quiescent (continuous sampling) power consumption is ~40 mW per chip.

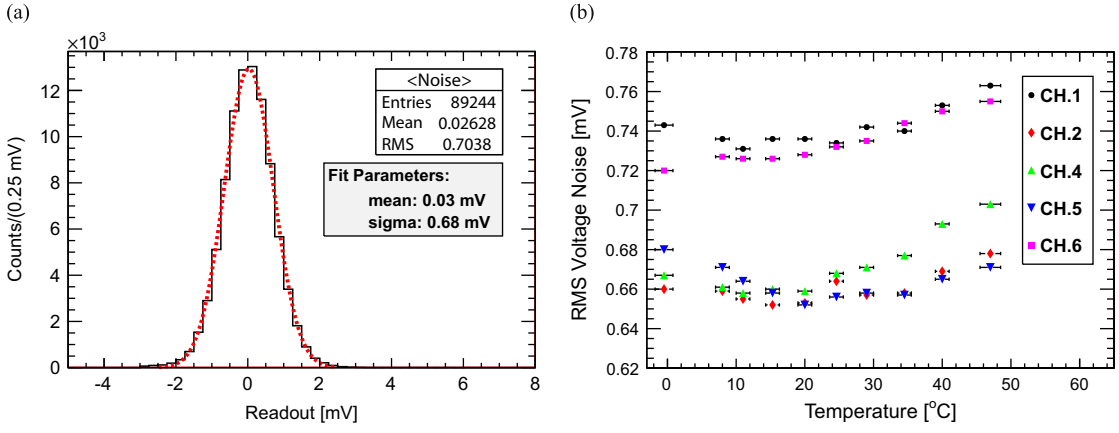

Fig. 12. (a) A PSEC4 baseline readout showing the electronic noise. The data are recorded from single channel after offset correction. The RMS value of ~ 700 μV is representative of the electronics noise on all channels. (b) Channel RMS noise measured over temperature.

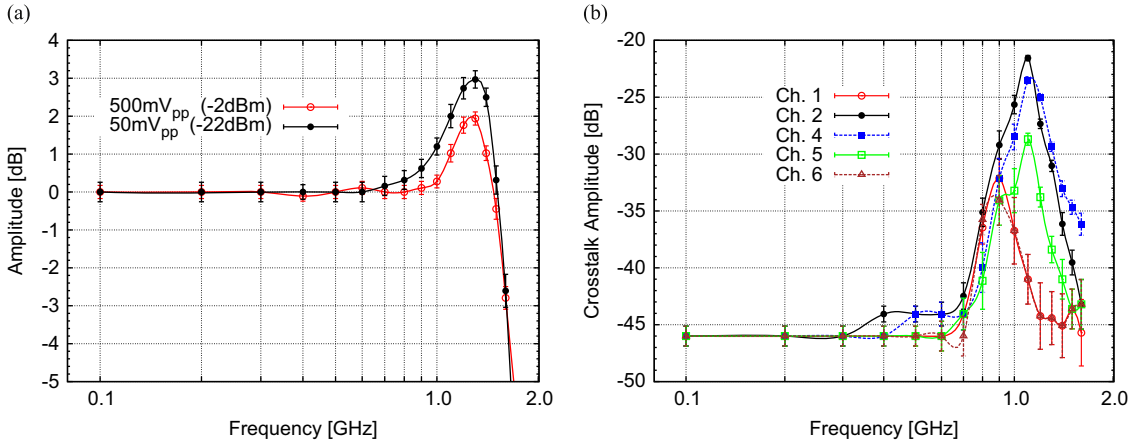

Fig. 14. (a) PSEC4 frequency response. The −3 dB analog bandwidth is 1.5 GHz. The positive resonance above 1 GHz is due to bondwire inductance of the signal wires in the chip package. Similar responses are shown for large and small sinusoidal inputs. (b) Channel-to-channel crosstalk as a function of frequency. Channel 3 was driven with a −2 dBm sinusoidal input. Adjacent channels see a maximum of −20 dB crosstalk at 1.1 GHz. The electronic noise floor is −50 dB for reference.

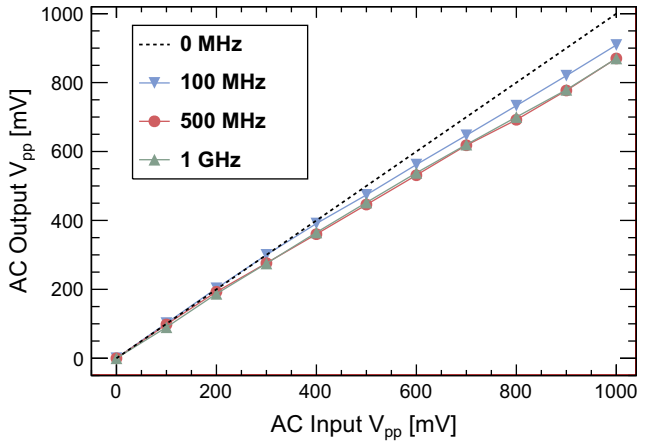

Fig. 15. AC response of a single channel. The PSEC4 data were converted to voltage using the DC linearity LUT as shown in Fig. 6. Saturation of the AC signals is observed for all frequencies, most clearly above 500 mV$_{pp}$.

the steady state power consumption and to separate the chip's digital processes from the analog sampling, the ADC is run only after a trigger is sent to the chip. Without a trigger, the quiescent power consumption is ∼40 mW per chip, including the locked VCDL sampling at 10.24 GSa/s and the current biases of all the comparators.

Initiating the ADC with a clock rate of 1 GHz causes the power draw to increase from 40 mW to 300 mW within a few nanoseconds. To mitigate high-frequency power supply fluctuations when switching on the ADC, several 'large' (2 pF) decoupling capacitors were placed on-chip near the ADC. These capacitors, in addition to the close-proximity evaluation board decoupling capacitors (∼0.1–10 μF), prevent power supply transients from impairing chip performance.

At the maximum PSEC4 sustained a trigger rate of 50 kHz, in which the ADC is running 20% of the time, a maximum average power of 100 mW is drawn per chip.

3.5. Frequency response

The target analog bandwidth for the PSEC4 design was ≥1 GHz. The bandwidth is limited by the parasitic input capacitance (C_{in}), which drops the input impedance at high frequencies[6] as

$$|Z_{in}| = \frac{R_{term}}{\sqrt{1+\omega^2 R_{term} C_{in}}} \tag{4}$$

where R_{term} is an external 50 Ω termination resistor. Accordingly, the expected half-power bandwidth is given by the following:

$$f_{3dB} = \frac{1}{2\pi R_{term} C_{in}}. \tag{5}$$

The extracted C_{in} from post-layout studies was ∼2 pF, projecting a −3 dB bandwidth of 1.5 GHz which corresponds to the measured value shown in Fig. 14a. The chip package-to-die bondwire inductance gives a resonance in the response above 1 GHz that distorts signal content at these frequencies. An external filter may be added to flatten the response.

The error bars correspond to the measurement procedure, in which several thousand sine waves are recorded at each frequency and histogrammed. The histogram bins with the maximum values are at the high and low peaks of the PSEC4-digitized sine wave. These peaks are fitted with a Gaussian function, from which the mean sine wave amplitude and measurement error (σ from fits) are extracted.

The measured channel-to-channel crosstalk is −25 dB below 1 GHz for all channels as shown in Fig. 14b. For frequencies less then 700 MHz, this drops to better than −40 dB. The primary crosstalk mechanism is thought to be the mutual inductance between signal bondwires in the chip package. High frequency substrate coupling on the chip or crosstalk between input traces on the PSEC4 evaluation board may also contribute.

3.5.1. AC linearity

The PSEC4 response to sinusoidal signals of varying magnitude is shown in Fig. 15. The AC signals were calibrated using the DC transfer count-to-voltage LUT (Fig. 6). Saturation is observed for signals as low as 100 MHz (∼9% above V_{pp} of 500 mV) and this effect becomes constant for frequencies above 500 MHz (∼15% above V_{pp} of 500 mV).

This AC saturation effectively reduces the PSEC4 ADC dynamic range. With a DC calibration, it was shown that 10.5 bits effectively covered a 1 V range including electronics noise. At 100 MHz, the

[6] This ignores negligible contributions to the impedance due to the sampling cell input coupling. The write switch on-resistance (≤4 kΩ over the full dynamic range) and the 20 fF sampling capacitance introduce a pole at ≥2 GHz.

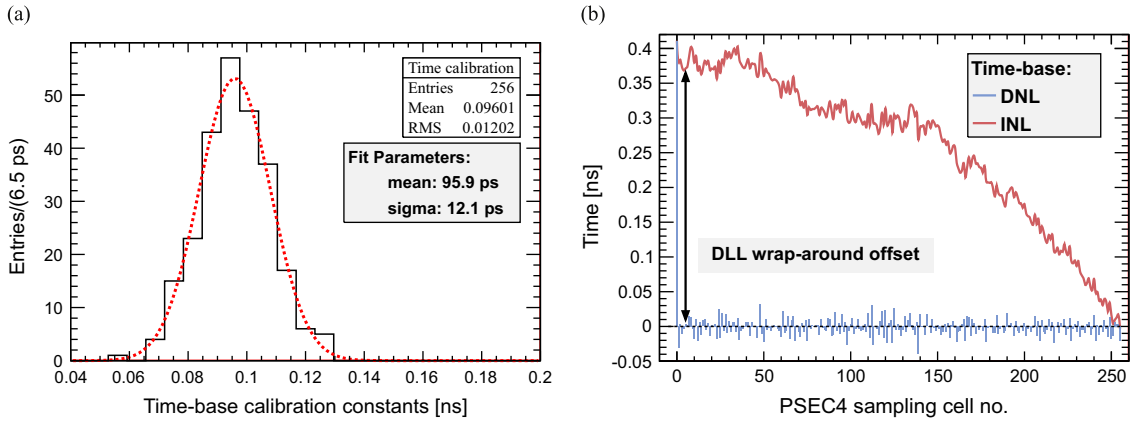

Fig. 16. (a) A histogram of the extracted time-base calibration constants (Δt) from a single channel. These values are calculated using the zero-crossing technique and are used to correct the sampling time-base of the PSEC4 chip. (b) The differential (DNL) and integral non-linearity (INL) of the PSEC4 time-base. The extracted Δt s are compared to an ideal linear time-base with equal time-steps per sample point. The large time-step at the first sample bin is caused by a fixed DLL latency when wrapping the sampling from the last cell to the first.

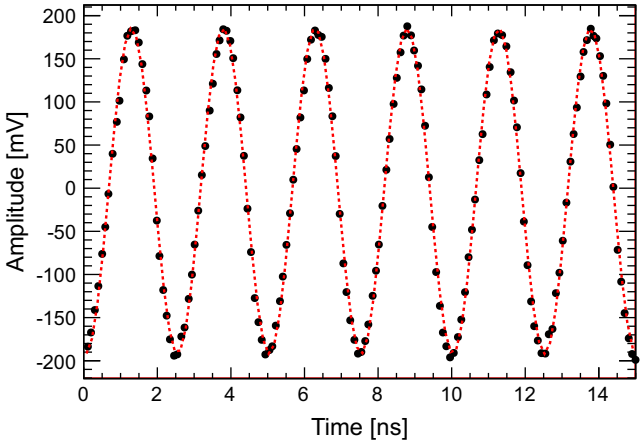

Fig. 17. A 10.24 GSa/s capture of a 400 MHz sine input is shown (black dots) after a channel-only linearity correction and time-base calibration. A fit (red dotted line) is applied to the data. (For interpretation of the references to color in this figure caption, the reader is referred to the web version of this article.)

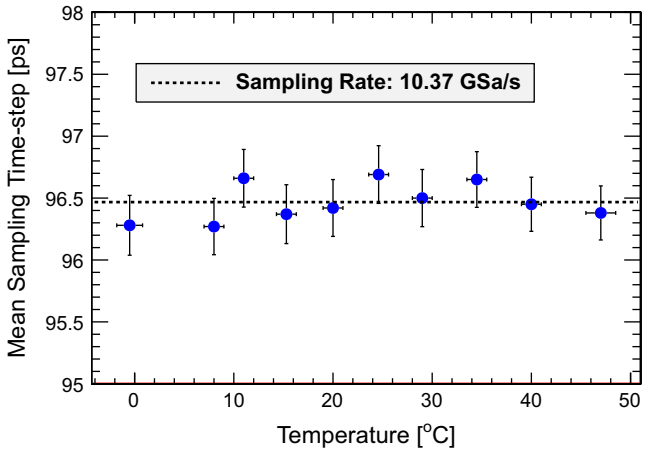

Fig. 18. Mean time-base step as measured over a temperature range −1 °C to 46 °C. The sampling rate is held constant over temperature with the on-chip DLL.

dynamic range drops to ~10.35 bits. For signals up to 1 GHz, the dynamic range is 10.3 bits. Additionally, an AC count-to-voltage conversion calibration LUT can be used to correct for this saturation.

3.6. Sampling calibration

For precision waveform feature extraction, both the overall time-base of the VCDL and the cell-to-cell time step variations must be calibrated. With the rate-locking DLL, the overall PSEC4 sampling time base is stably servo-controlled at a default rate of 10.24 GSa/s. The time-base calibration of the individual 256 delay stages, which vary due to cell-to-cell transistor size mismatches in the VCDL, is the next task. Since this is a fixed-pattern variation, the time-base calibration is typically a one-time measurement.

The brute force 'zero-crossing' time-base calibration method is employed [25]. This technique counts the number of times a sine wave input crosses zero voltage at each sample cell. With enough statistics, the corrected time per cell is extracted from the number of zero-crossings (N_{zeros}) using

$$\langle \Delta t \rangle = \frac{T_{input} \langle N_{zeros} \rangle}{2N_{events}} \tag{6}$$

where T_{input} is the period of the input and N_{events} is the number of digitized sine waveforms. A typical PSEC4 time-base calibration uses 10^6 recorded events of 400 MHz sinusoids.

The variation of the time-base sampling steps is ~13% as shown in Fig. 16a. Due to a relatively large time step at the first cell, the average sampling rate over the remaining VCDL cells is ~10.4 GSa/s, slightly higher than the nominal rate. With the servo-locking DLL the INL is constrained to be zero at the last cell. A digitized 400 MHz sine wave is shown in Fig. 17 after applying the time-base calibration constants.

The non-linearity of the PSEC4 time-base is shown in Fig. 16b. Each bin in the plot is indicative of the time-base step between the binned cell and its preceding neighbor cell. The relatively large DNL in the first bin, which corresponds to the delay between the last (cell 256) and first sample cells, is caused by a fixed DLL latency when wrapping the sampling from the last cell to the first.

The mean sampling rate is shown in Fig. 18 to be uniform over temperature. This is an expected feature of the on-chip DLL. Fifty-thousand events were recorded at each temperature point and the zero crossing algorithm was run on each dataset. No temperature dependence is observed.

3.7. Waveform timing

The effective timing resolution of a single measurement is calculated by waveform feature extraction after linearity and time-base calibration. A $0.5V_{pp}$, 1.25 ns FWHM Gaussian pulse was created using a 10 GSa/s arbitrary waveform generator (Tektronix

AWG5104). The output of the AWG was sent to two channels of the ASIC using a broadband-RF 50/50 splitter (Mini-Circuits ZFRSC-42). This pulse, as recorded by a channel of PSEC4, is shown in Fig. 19. A Gaussian functional fit is performed to the leading edge of the pulse. The pulse times from both channels are extracted from the fit and are subtracted on an event-by-event basis.

The timing resolution was measured by asynchronous pulse injection to two channels of PSEC4. In this measurement, the two pulses were delayed relative to one-another and the waveforms were captured uniformly across the 25 ns PSEC4 sampling buffer. Ten-thousand events were recorded at each delay stage. The time difference resolution was extracted by the waveform fitting procedure shown in Fig. 19, before and after applying the time-base calibration to both channels. Fig. 20a and b shows the timing resolution results for pulse separations in the PSEC4 buffer of 0 ns and 16 ns, respectively. For uncalibrated data in which the pulse separation is non-zero, the bimodal timing distribution is due to the fixed DLL-wraparound offset.

A PSEC4-calibrated timing resolution of 9 ps or better was measured over a 20 ns span of pulse separation as shown in Fig. 21. The 1σresolution was extracted by fitting the calibrated timing distributions shown in Fig. 20. For simultaneous pulses the resolution is ~4 ps, but the timing resolution slightly degrades as the time difference between pulses is increased. The large RMS in the timing for uncalibrated data is due to the DLL wrap around offset of roughly 400 ps.

3.8. Performance summary

The performance and key architecture parameters of PSEC4 are summarized in Table 1.

4. Conclusions

We have described the architecture and performance of the PSEC4 waveform digitizing ASIC. The advantages of implementing waveform sampling IC design in a deeper sub-micron process are shown, with measured sampling rates of up to 15 GSa/s and analog bandwidths of 1.5 GHz. Potential 0.13 μm design issues, such as leakage and dynamic range, were optimized and provide a 1 V dynamic range with sub-mV electronics noise. After a one-time timebase calibration, it is possible to extract precision timing measurements (4–9 ps) when applying a simple rising-edge fit to the PSEC4 digitized waveform.

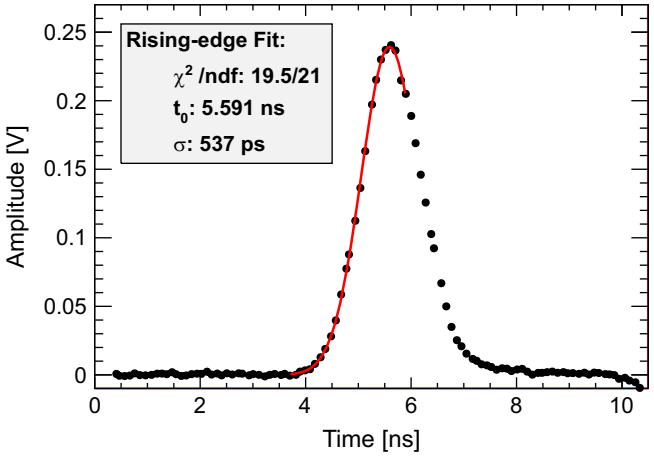

Fig. 19. An example PSEC4 digitized pulse (black dots) and waveform fit (red line) that was used for the timing resolution measurement. A 1.25 ns FWHM Gaussian pulse was split and injected into two channels of the chip. The waveform was captured at 10.24 GSa/s and is shown after applying the time-base calibration constants. (For interpretation of the references to color in this figure caption, the reader is referred to the web version of this article.)

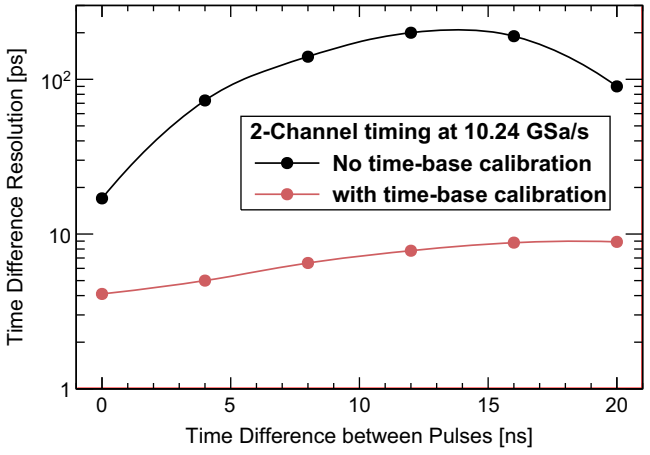

Fig. 21. Two-channel time resolution from asychronous pulse injection into PSEC4. The timing resolution as a function of pulse separation in the PSEC4 sampling buffer is shown.

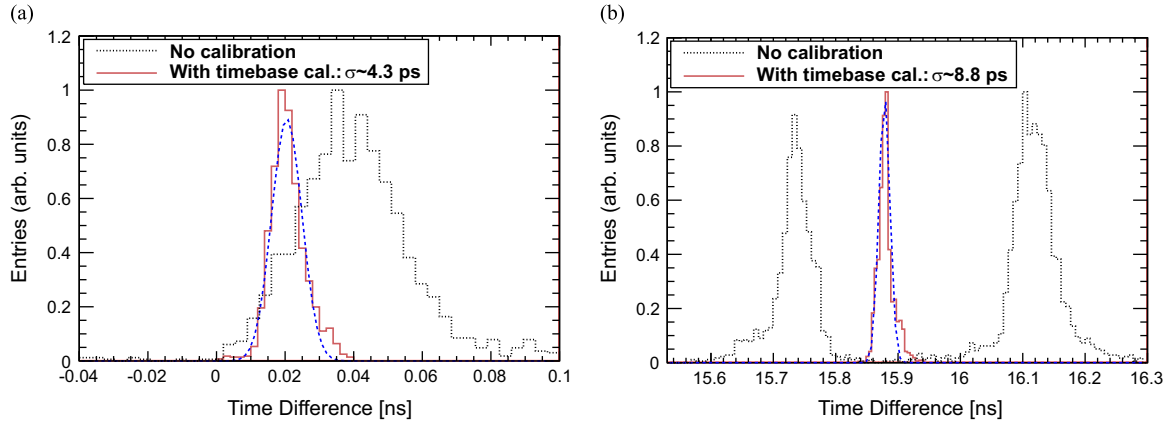

Fig. 20. Time resolution results before (black-dashed) and after (maroon-solid lines) applying timebase calibrations. Pulses were injected asynchronously into two channels of PSEC4. Data are shown for pulse separations of (a) ~0 ns, and (b) ~16 ns. The bimodal distribution in the pre-calibration data of (b) corresponds to the fixed DLL wraparound offset. (For interpretation of the references to color in this figure caption, the reader is referred to the web version of this article.)

Table 1
PSEC4 architecture parameters and measured performance results.

Parameter	Value	Comment
Channels	6	Die size constraint
Sampling rate	4–15 GSa/s	Servo-locked on-chip
Samples/channel	256	249 Samples effective
Recording buffer time	25 ns	At 10.24 GSa/s
Analog bandwidth	1.5 GHz	
Crosstalk	7%	Max. over bandwidth
	$<1\%$	Typical for signals <800 MHz
Noise	700 μV	RMS (typical). RF-shielded enclosure. After calibration
DC RMS dynamic range	10.5 bits	12 Bits logged. Linearity calibration for each cell
Signal voltage range	1 V	After linearity correction
ADC conversion time	4 μs	Max. 12 bits logged at 1 GHz clock speed
	250 ns	Min. 8-bits logged at 1 GHz
ADC clock speed	1.4 GHz	Max.
Readout time	$0.8n$ μs	n is a number of 64-cell blocks to read ($n=24$ for entire chip)
Sustained trigger rate	50 kHz	Max. per chip. Limited by [ADC time + readout time]$^{-1}$
Power consumption	100 mW	Max. average power
Core voltage	1.2 V	0.13 μm CMOS standard

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