A Fast Waveform-Digitizing ASIC-based DAQ for a Position & Time Sensing Large-Area Photo-Detector System

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on behalf of the LAPPD collaboration

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Argonne NATIONAL LABORATORY

HIGH ENERGY PHYSICS
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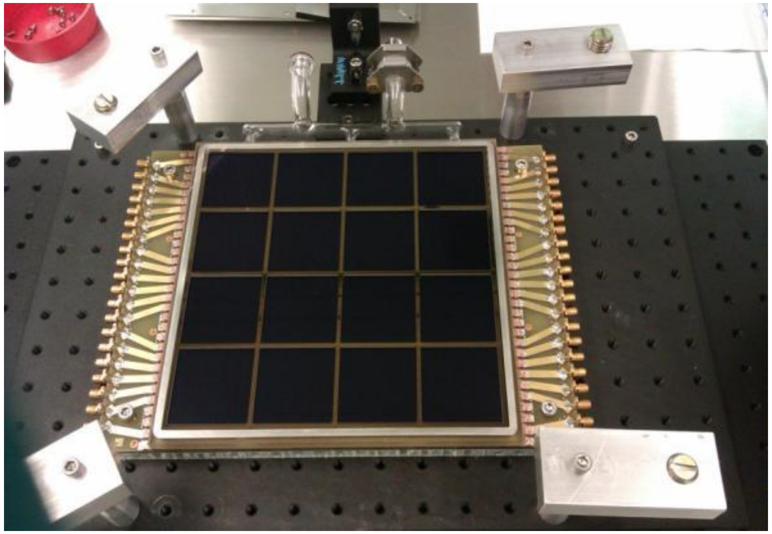
Outline

- **LAPPD overview:** development of low-cost, large-area micro-channel plate photo-detectors (MCP-PMTs) for fast timing
- **Front-end electronics**: custom gigahertz waveform digitizing ASICs
- **System:** DAQ and detector readout/integration



The 400 sq. cm `Demountable' LAPPD MCP detector

Large-Area Picosecond Photo-Detector Collaboration (LAPPD)

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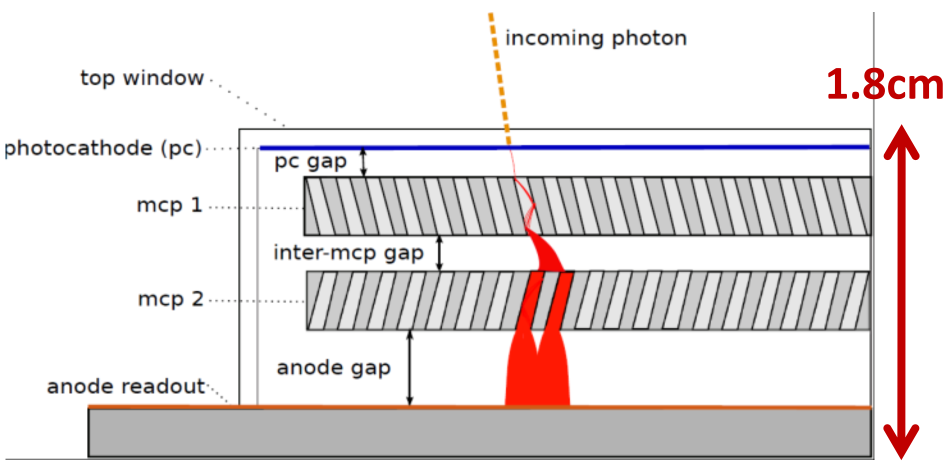
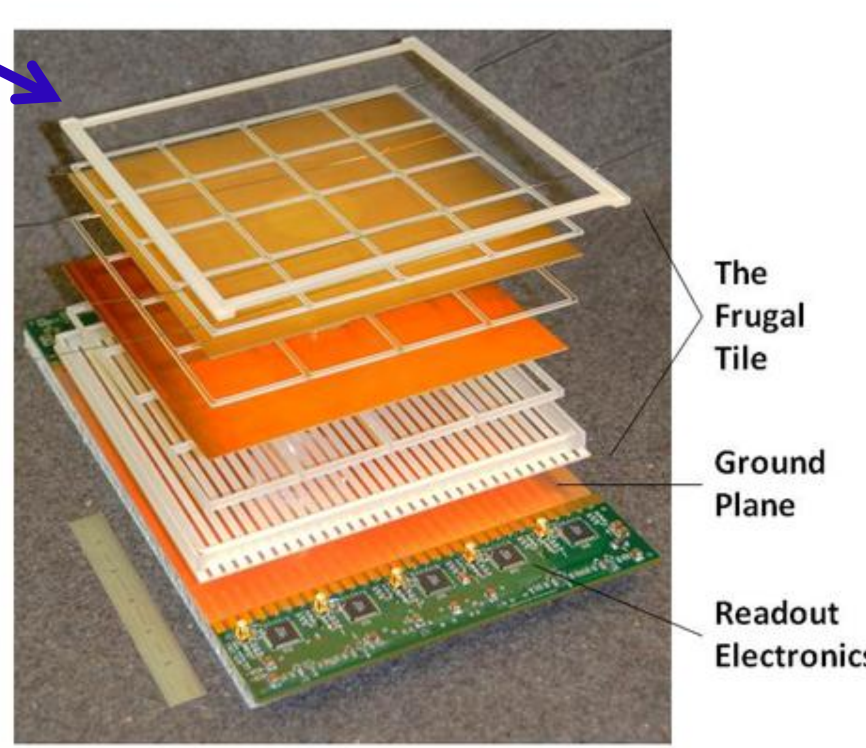
- **Goals:** Large-area, relatively low-cost, ~picosecond timing
- **Span of R&D efforts:** photocathode, MCP, **integrated electronics,** hermetic packaging
  - 20 x 20 cm^2 phototubes = **'tile'**
  - Gain >= 10^6 with two MCP plates
  - RF Transmission line anode (30 CH/side)
  - Internal HV distribution
  - SEE layer deposited with ALD



Limited sensitivity to magnetic field…?



The Frugal Tile - Detector Assembly

Super Module (SuMo) MCP Photodetector

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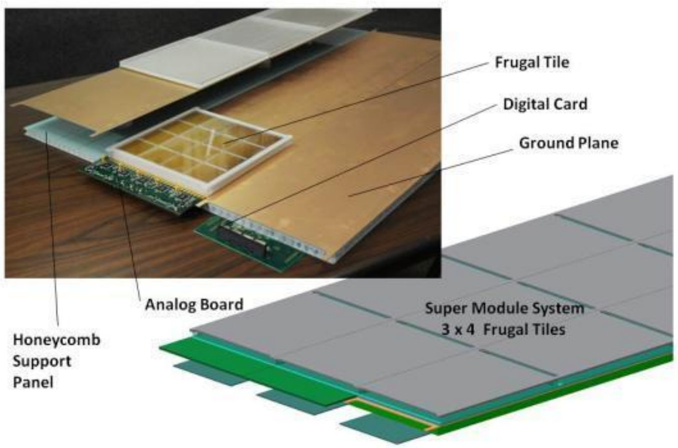
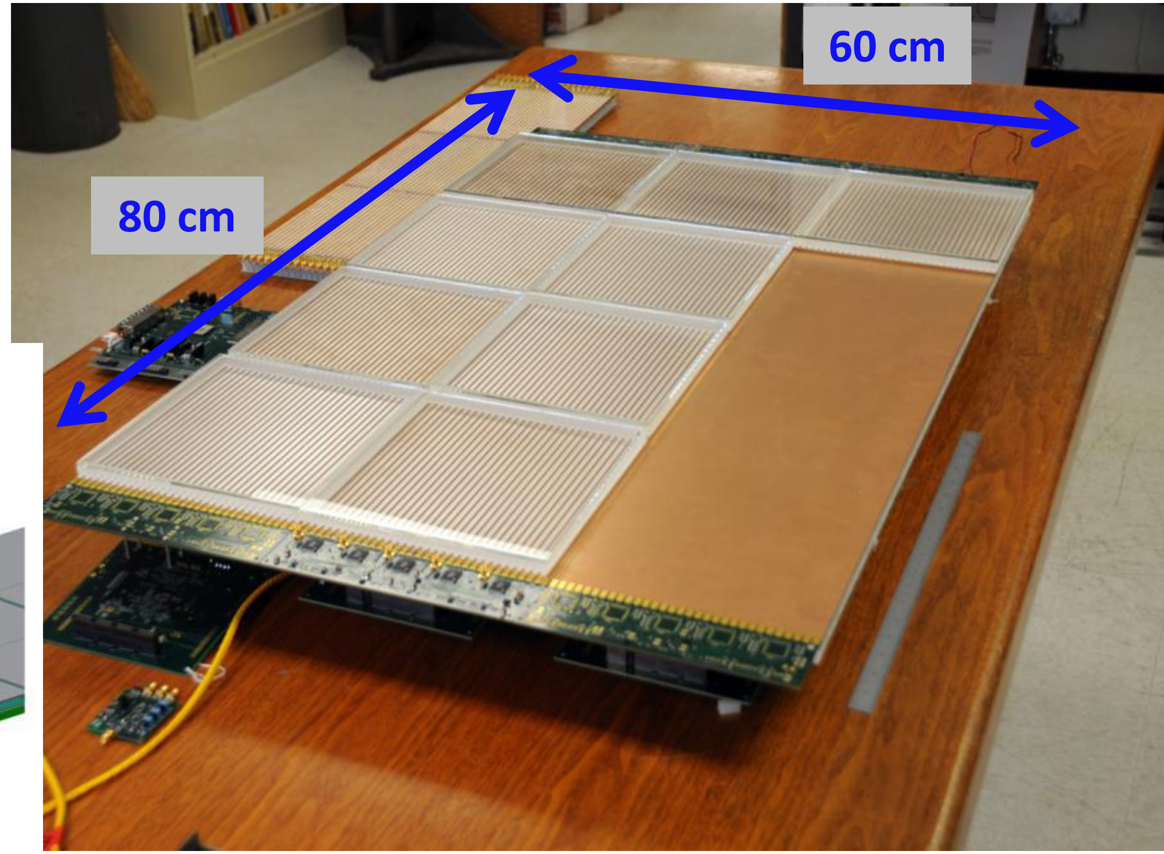
- **<u>0.5m²</u> of photo-sensitive area:** 3x4 array of 20cm LAPPD MCP tiles
- **Thin profile glass packaging**
- **Highly integrated electronics:** 180 channels of fast waveform digitization
  → <u>input</u>: *high voltage + system clk, etc.*; <u>output</u>: *gigabit Ethernet*

System bandwidth ~400 MHz



Tray and Tiles - The Super Module System



LAPPD 20cm anode

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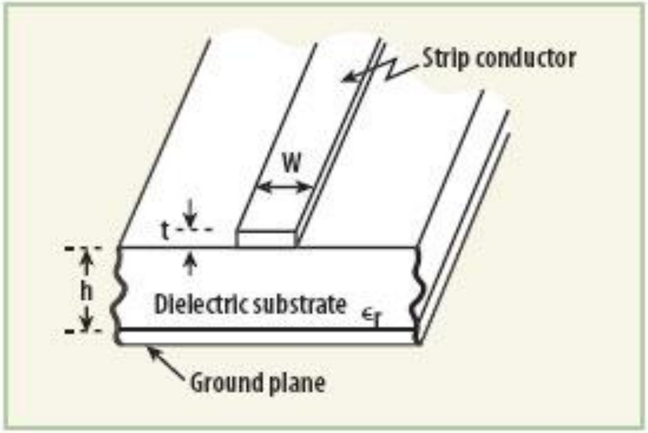
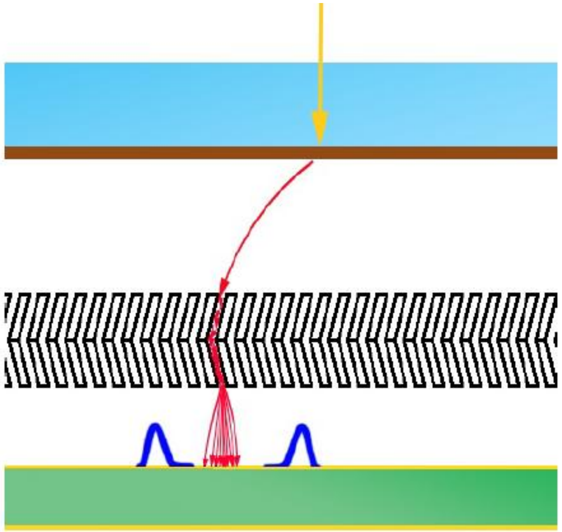


1. Microstrip transmission lines consist of a strip conductor and a ground metal plane separated by a dielectric medium.

Microwaves & RF



After final amplification, the shower of electrons is accelerated towards the anode, inducing EM waves that propagate in both directions along transmission line. (ABW ~3 GHz for 20cm anode)

First 20cm MCP tests

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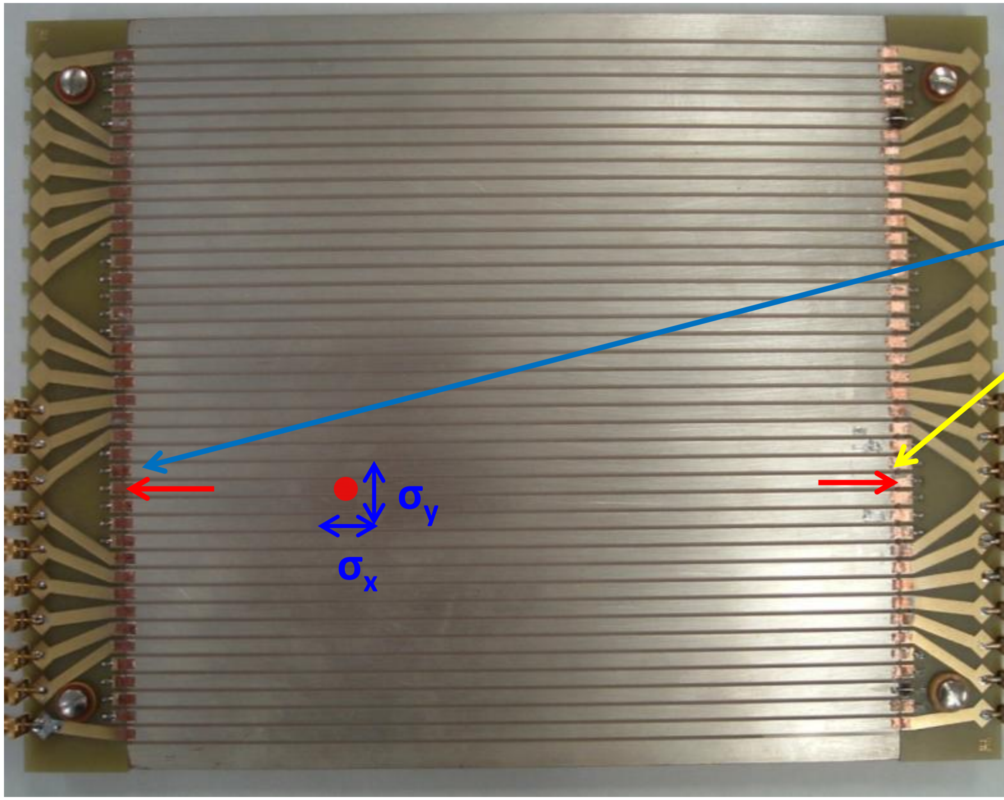
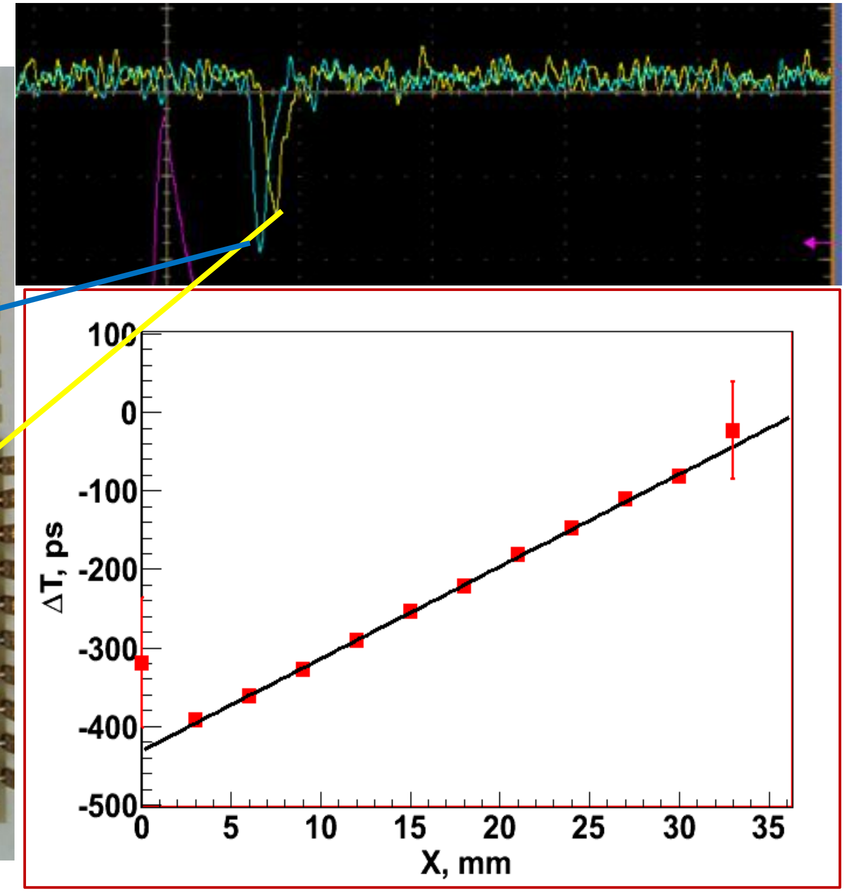


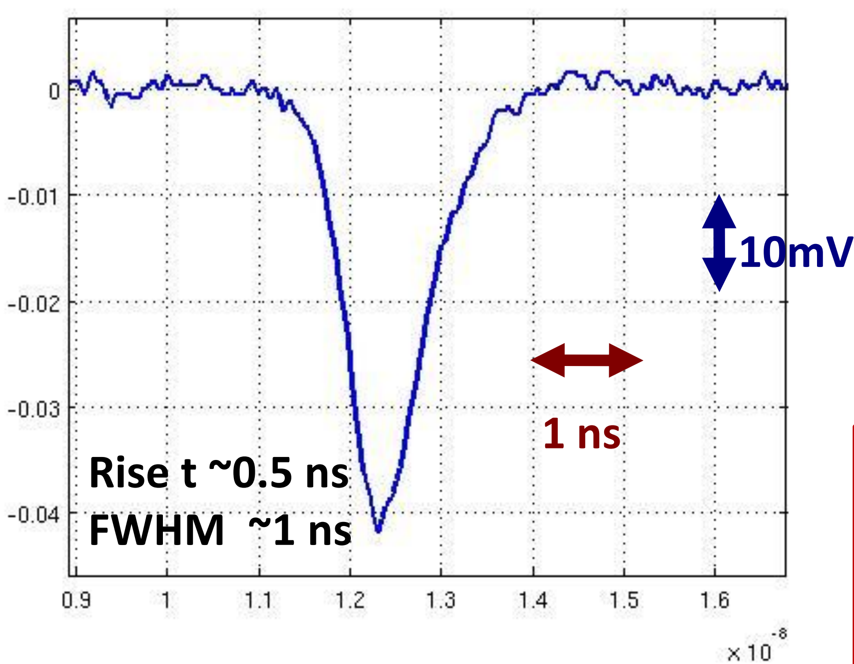


Location of event (x,y) determined by the time difference of signal on two ends (x) and the charge-centroid of adjacent strips (y)

- Position resolution <--> time resolution **[$\sigma_x = \sigma_t * v_{prop}$]**
  - **100 ps ~ 1.5 cm**
  - **10 ps ~1.5 mm ...etc.**

33mm MCP position scan:
V_{prop} ~ 2/3c
along stripline
(σ_t ~15 ps).

MCP pulses & timing

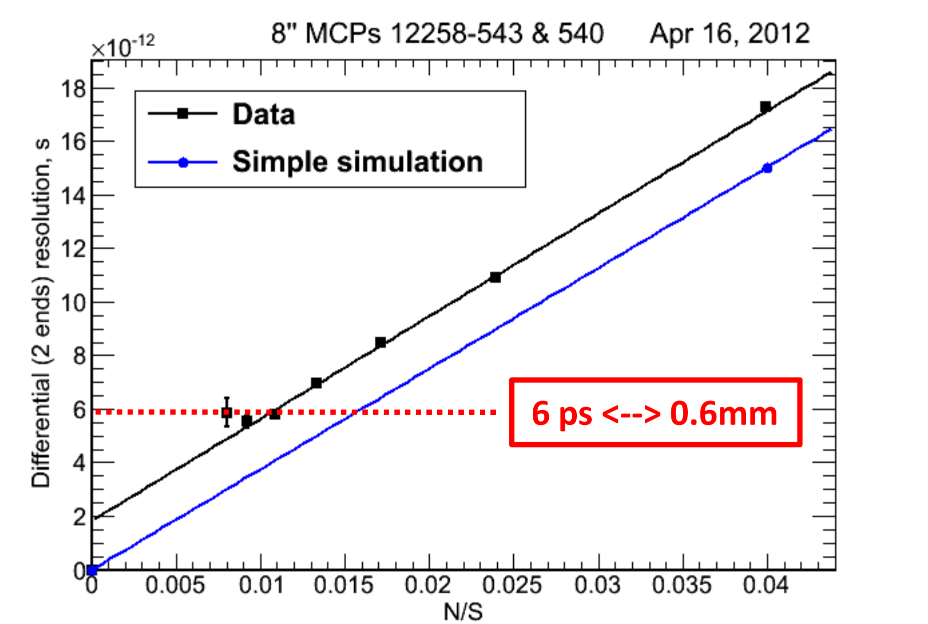


Timing analysis approach:

1) **Save digitized waveform (scope/ASIC)**
2) **Pick algorithm in software/firmware:**
   - Fit rising edge
   - constant fraction discrimination (CFD)
   - χ^2 template fit to waveform

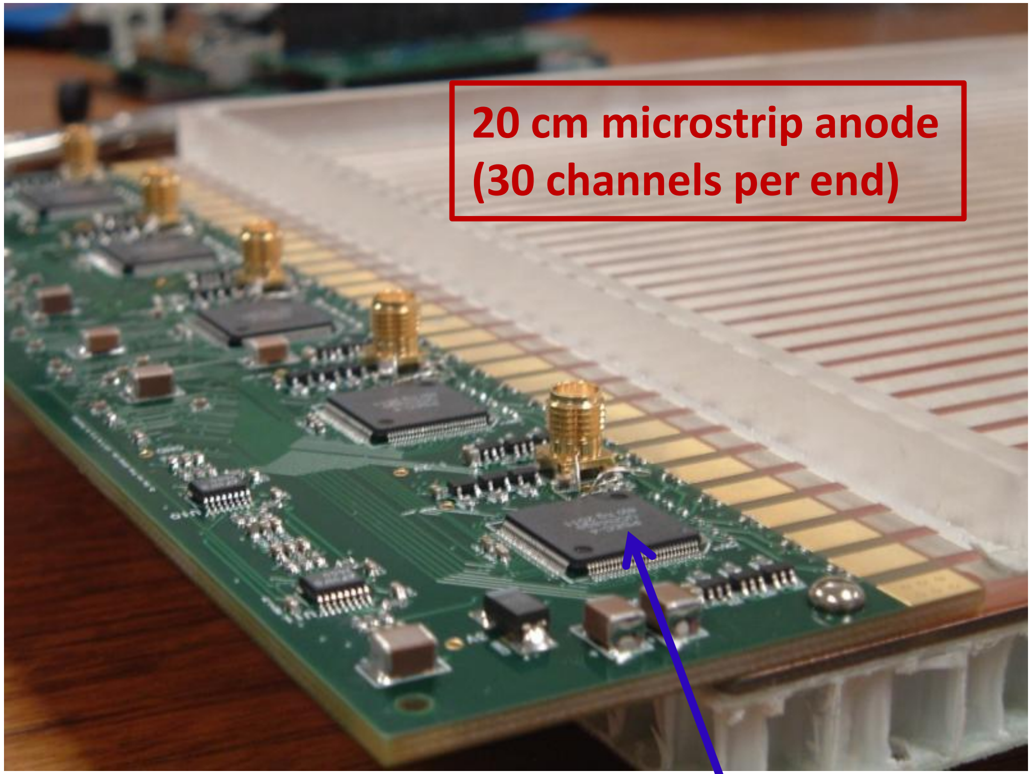
Time resolution determinants:

1) Signal to noise
2) Analog Bandwidth
3) Sampling rate
4) Signal statistics



Detector-integrated Front-end Readout

- Custom waveform sampling ASICs record signals from both ends of microstrip anode
  - → High channel density
  - → Compact electronics integration with detector
  - → Low power
  - → Low cost per channel (<$20 per channel in volume)
  - → Handle noise and poorly formed pulses
  - → Preserve timing information



'Analog Card'

PSEC-4: 6-channel fast waveform digitizing ASIC using switched capacitor array architecture

Switched capacitor array sampling: *'analog down-conversion'*

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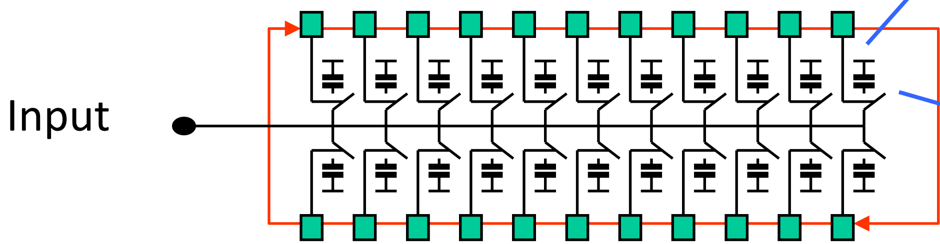
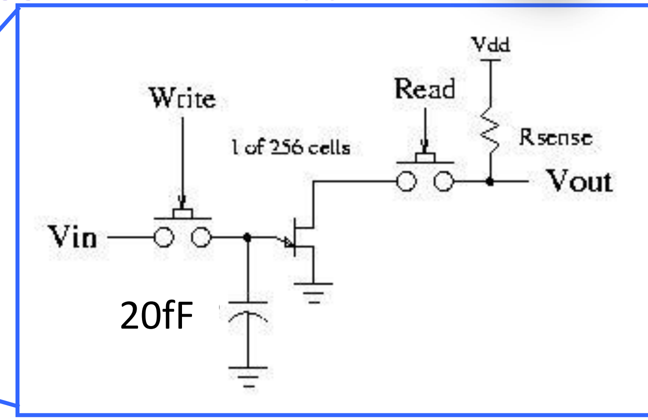
[GHz sampling→ 10-100 MHz readout: useful in most 'triggered event' applications]

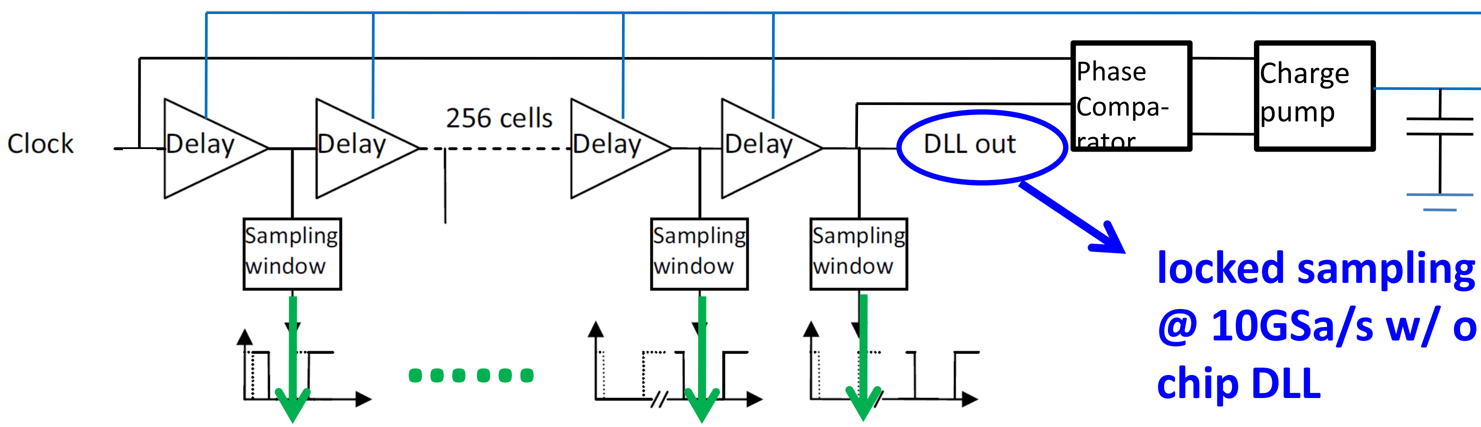
Write pointer passed along array - generates 'sampling window' (~5-10 switches closed at once):





Tiny charge: 1mV ~ 100e$^-$

Timing generation with a delay locked loop (DLL):



locked sampling @ 10GSa/s w/ on chip DLL

To switched capacitor array – sample & hold

PSEC-4 ASIC

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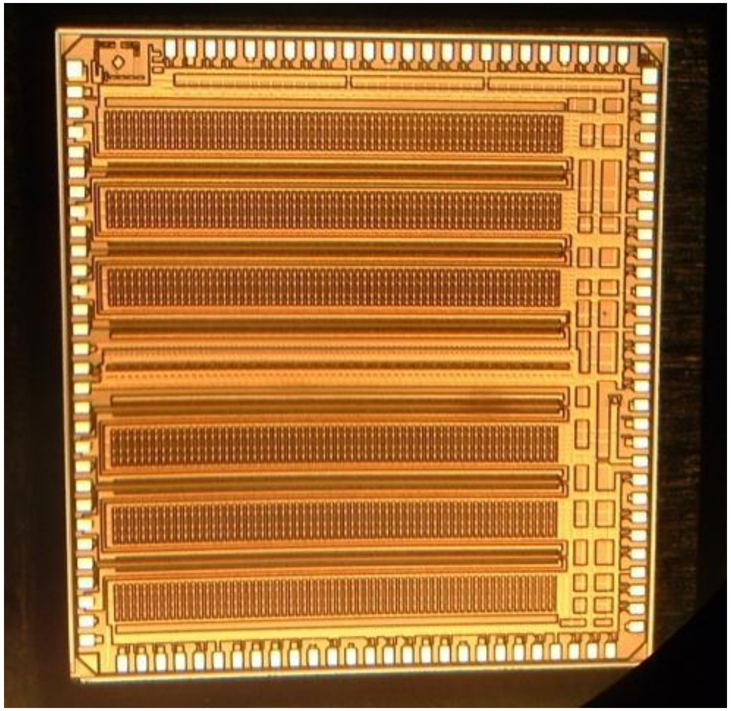
10-15 GSa/s Waveform Sampling ASIC

	ACTUAL PERFORMANCE
Sampling Rate	2.5-15 GSa/s
# Channels	6
Sampling Depth	256 points (17-100 ns) per channel
Input Noise	<1 mV RMS
Analog Bandwidth	1.5 GHz (f_{3dB})
ADC conversion (ramp-compare)	Up to 12 bit (10 ENOB) clocked @ 1.6 GHz
Dynamic Range	0.1-1.1 V
Readout Latency	2 μs (min) – 16 μs (max)

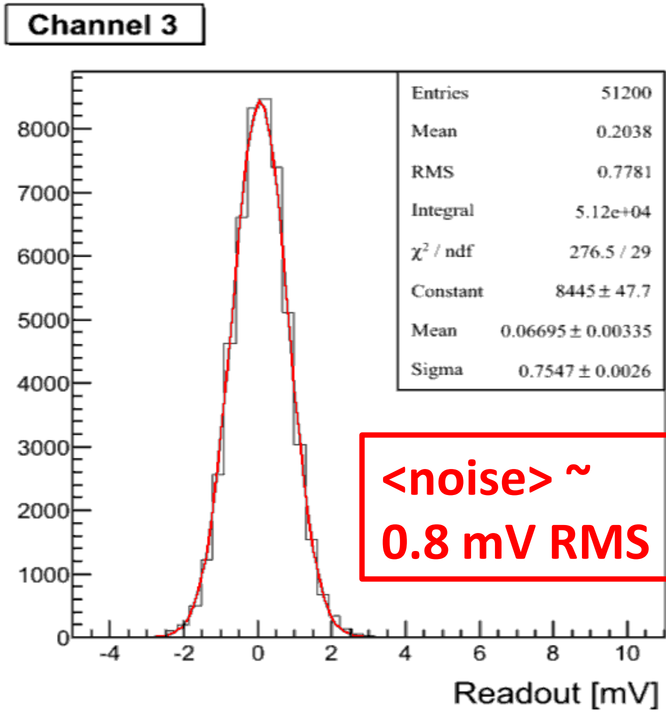


Designed to sample & digitize fast pulses (MCPs):

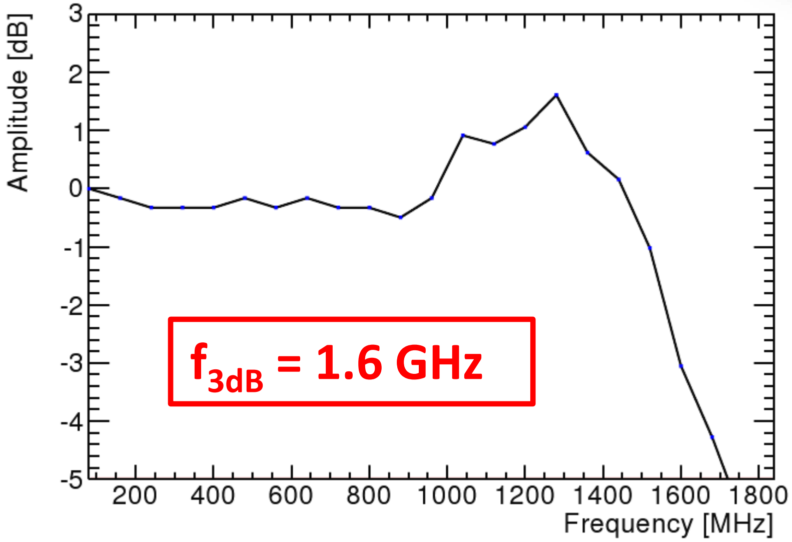
- Sampling rate capability > 10GSa/s
- Analog bandwidth > 1 GHz   (challenge!)
- Relatively short buffer size
- event-rate capability ~100 KHz

→ ***130 nm CMOS***

PSEC-4 Performance



<noise> ~ 0.8 mV RMS



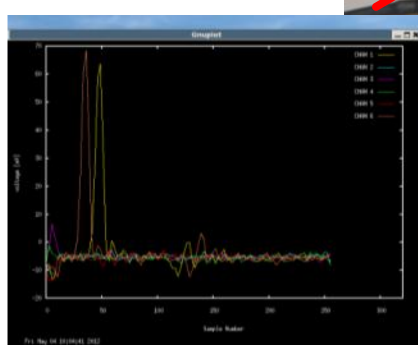
f_{3dB} = 1.6 GHz

PSEC-4 evaluation <u>board</u>

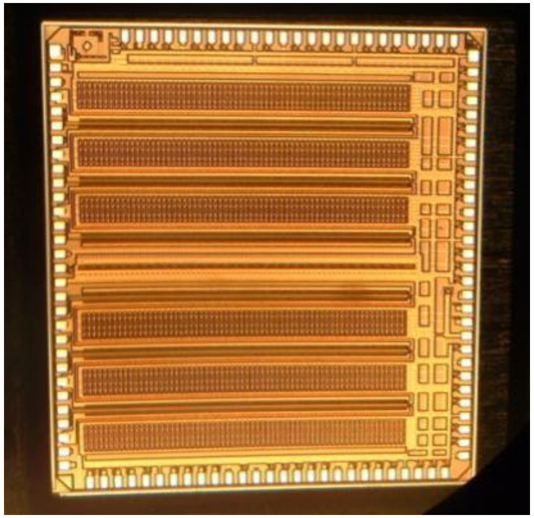
6 channel, 10 GSPS

'oscilloscope on a chip'

– **USB 2.0 interface**



Oscilloscope on a Chip?



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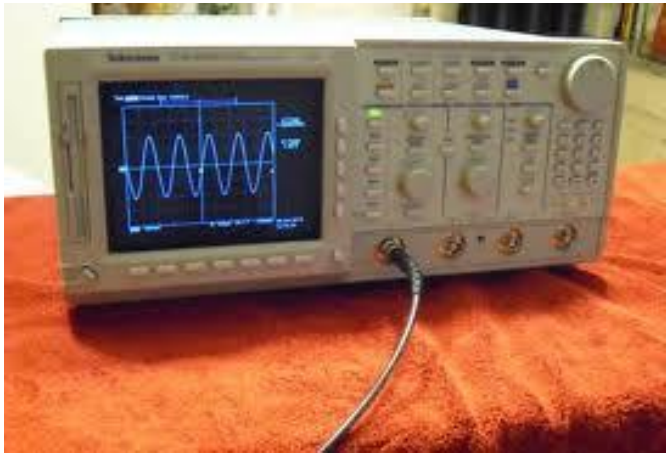
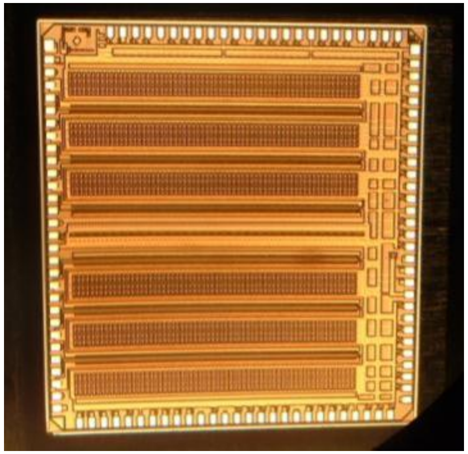


Oscilloscope on a Chip?

Not quite…a modified approximation:



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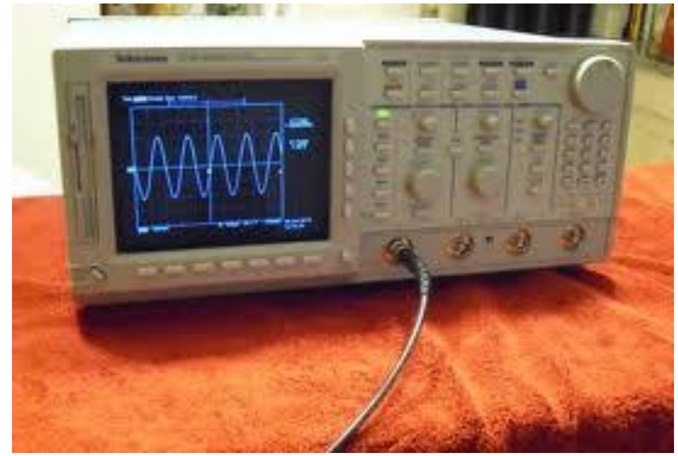
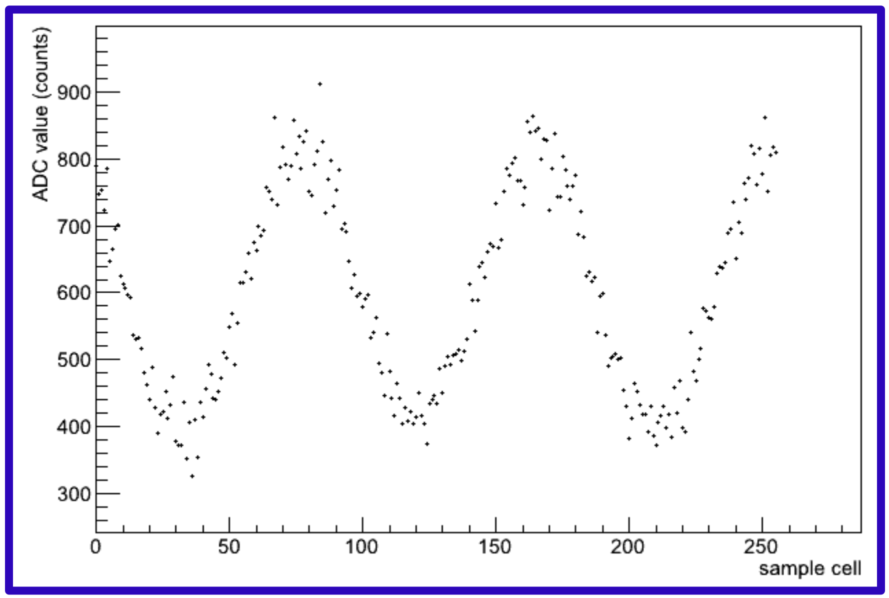


For example, a raw **PSEC-3** readout (10 GS/s) of 120 MHz, 150 mV_{rms} sine wave:



Waveform Digitizer (Voltage) Calibration

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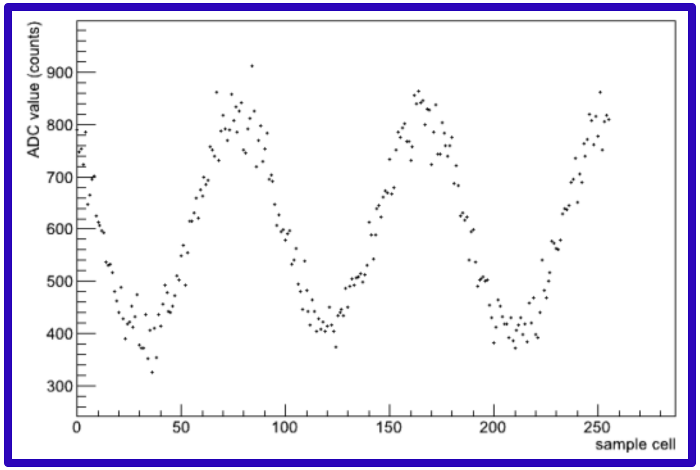

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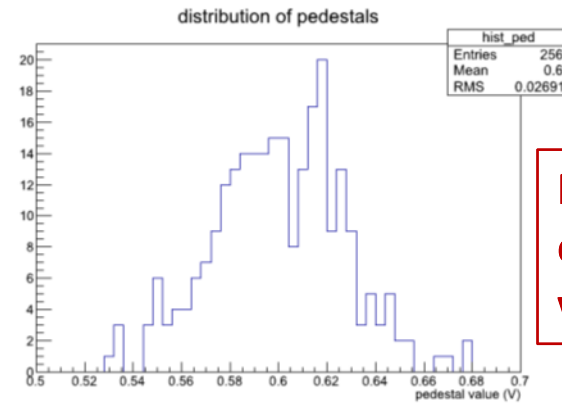

Fixed cell-to-cell pedestal variations

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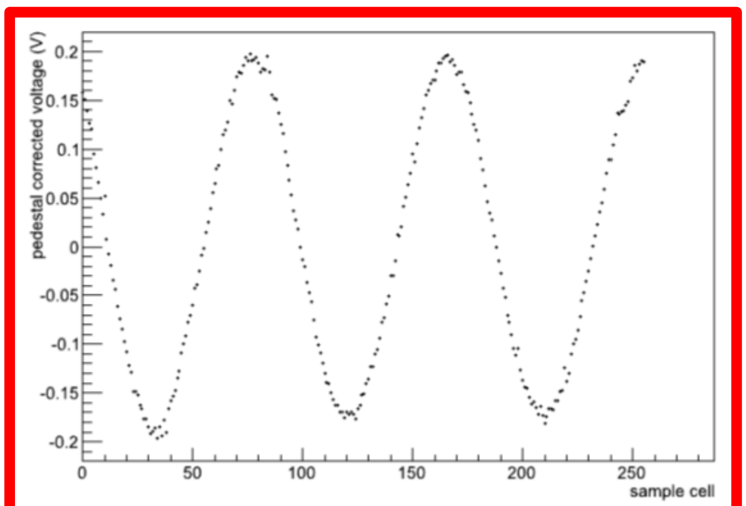
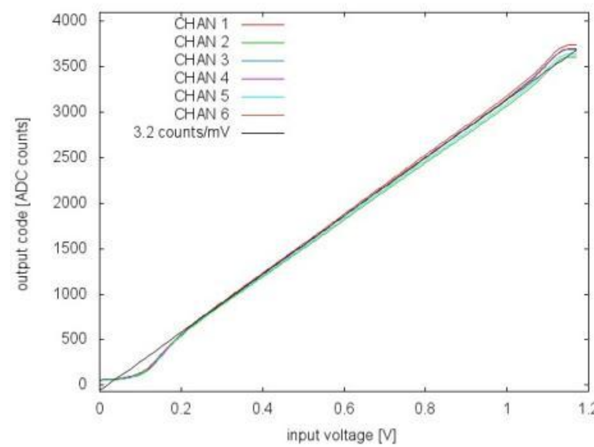




ADC count-to-Voltage LUT

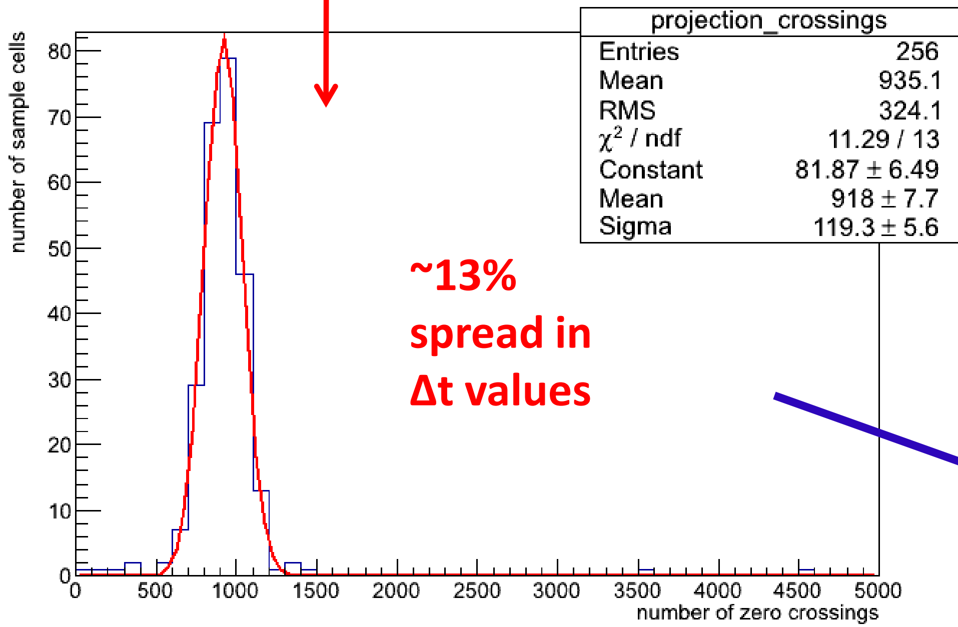
Straightforward to implement these corrections in an FPGA
(need to apply these calibrations in order to further process data)

Further Calibrations…

Time base correction:

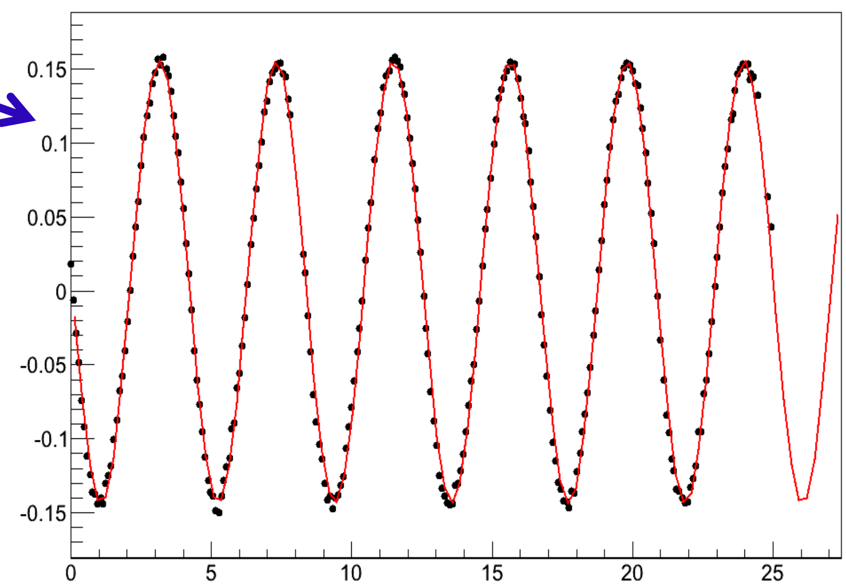
Keep overall sampling rate constant (or correct for drift) – **DONE** w/ on-chip DLL

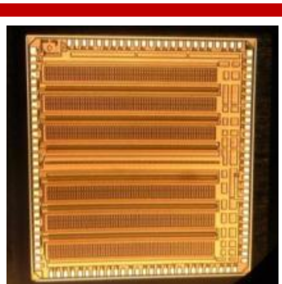
Correct for cell-to-cell variations in sampling rate (nominal Δt~100ps @ 10 Gsa/s)



~13% spread in Δt values

240 MHz sine with 'all' calibrations applied (PSEC-4)





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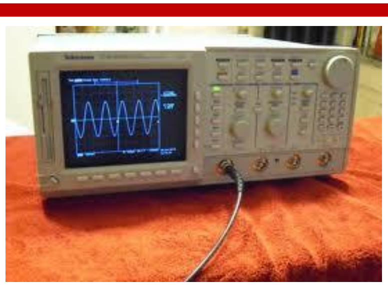

Ready to go

PSEC-4 Performance revisited

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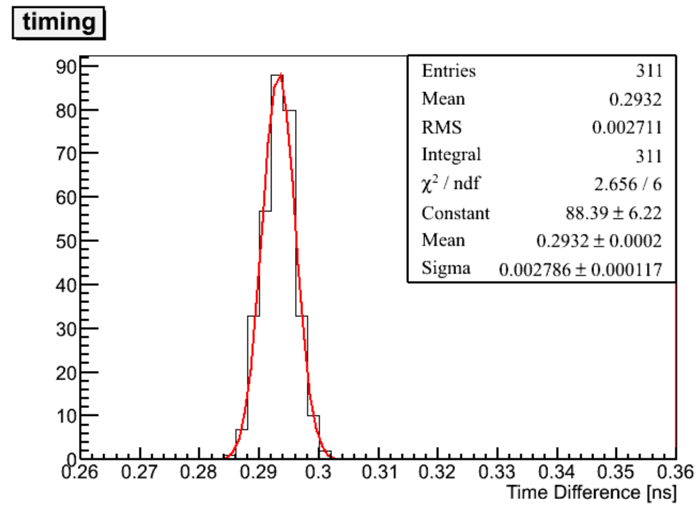
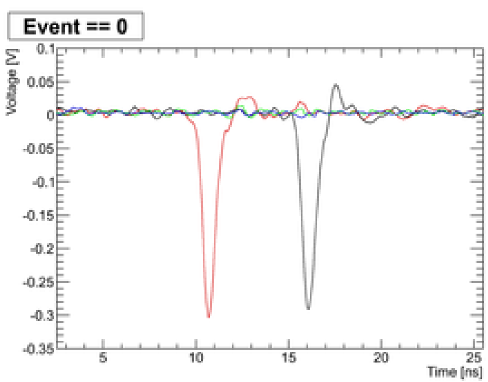
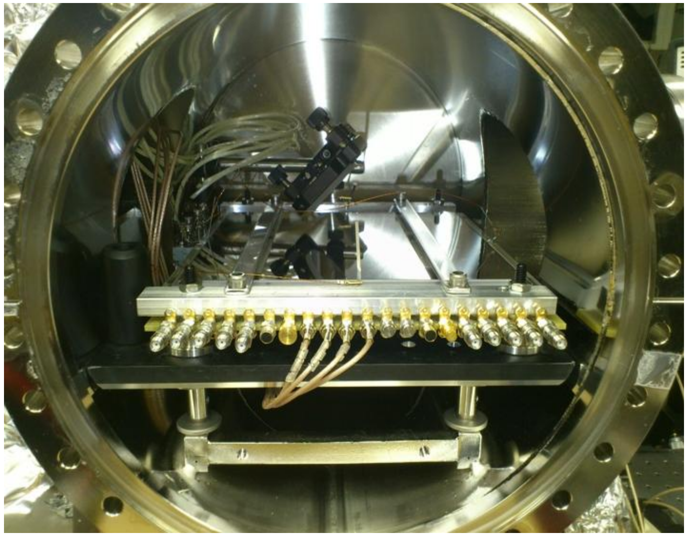
Applying calibrations, bench test (ideal) timing measurement yields **σ_t ~ 3 ps** (2-channel timing on single PSEC-4 ASIC)



[preliminary]

PSEC-4 Eval board has begun active use as readout platform in **20 cm MCP testing** →





with only 6 channels, a full DAQ is required to readout the full anode of the 20 cm detectors…

Super Module DAQ

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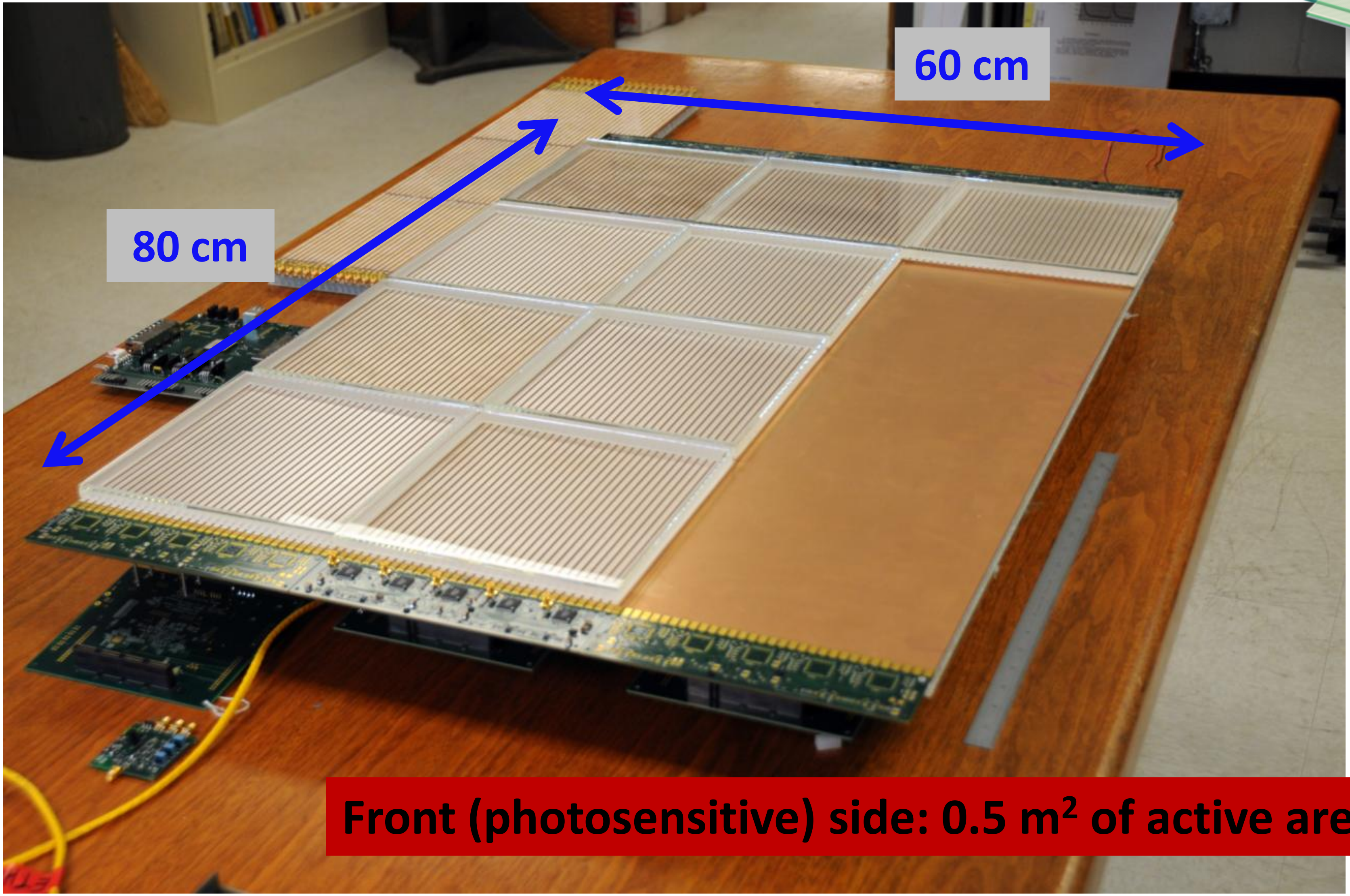
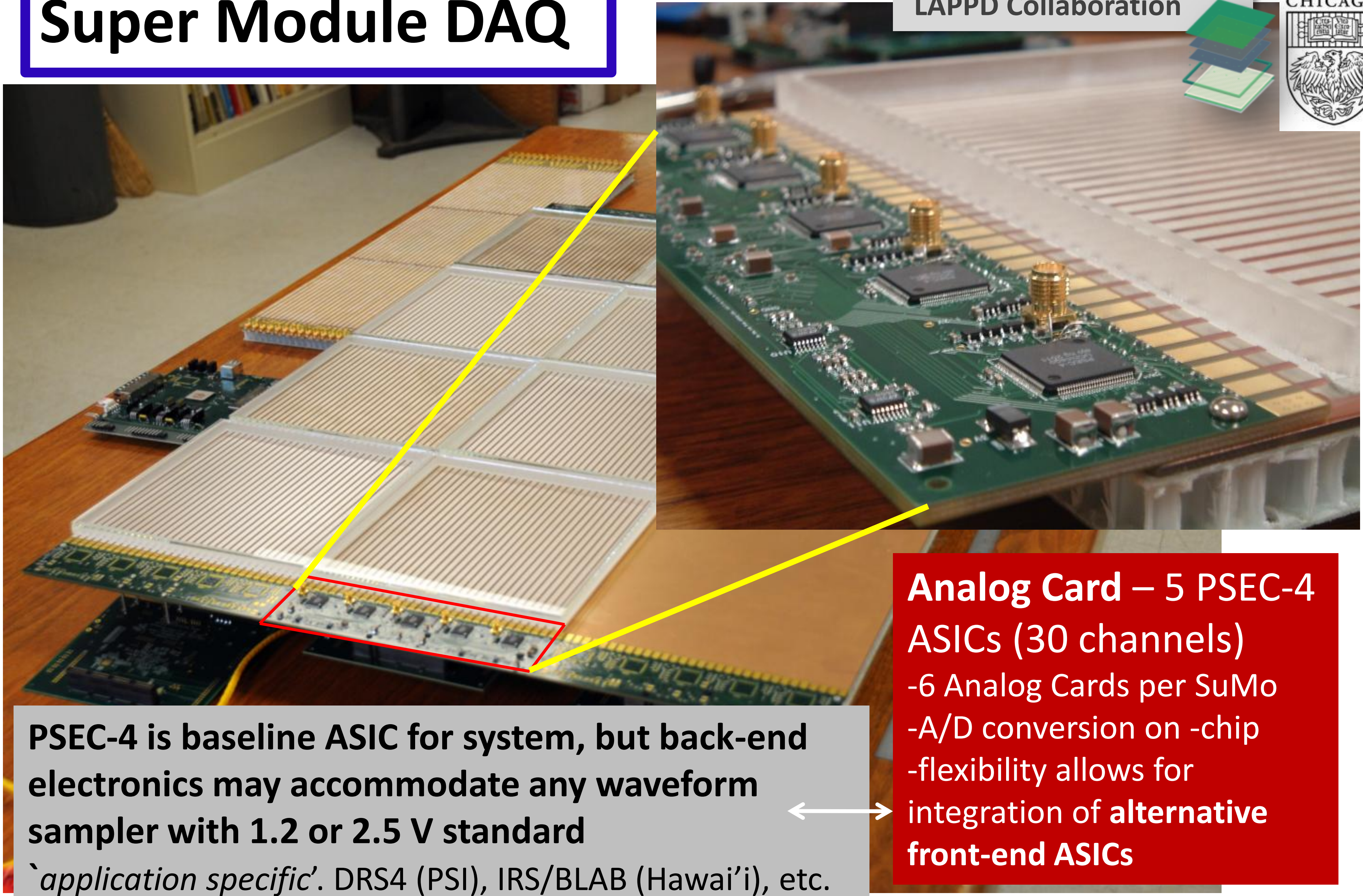


Front (photosensitive) side: 0.5 m^2 of active area

Super Module DAQ



Analog Card – 5 PSEC-4 ASICs (30 channels)
- -6 Analog Cards per SuMo
- -A/D conversion on -chip
- -flexibility allows for integration of **alternative front-end ASICs**

PSEC-4 is baseline ASIC for system, but back-end electronics may accommodate any waveform sampler with 1.2 or 2.5 V standard `*application specific*'. DRS4 (PSI), IRS/BLAB (Hawai'i), etc.

Super Module DAQ

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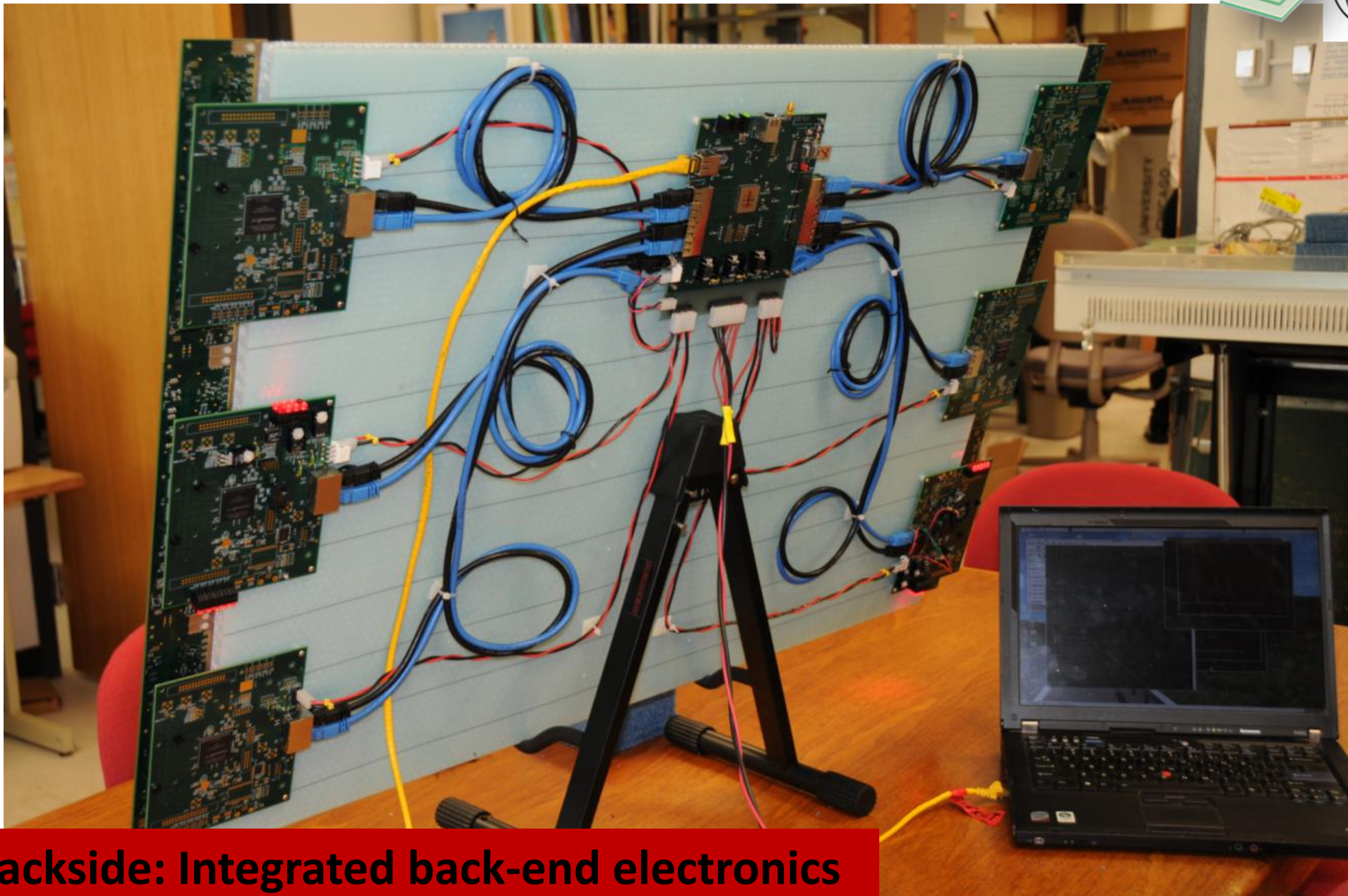

Backside: Integrated back-end electronics

Super Module DAQ

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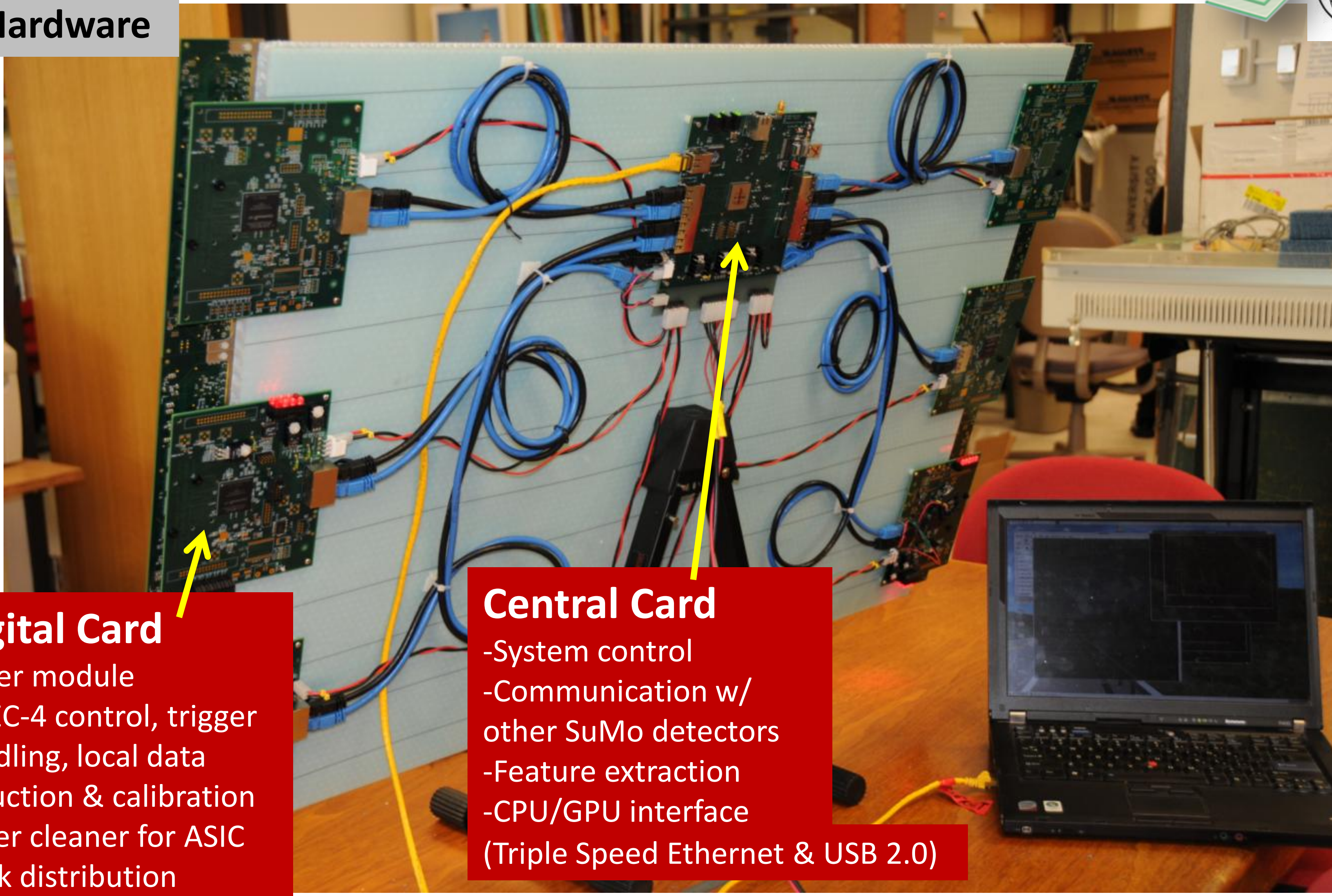
Hardware



Digital Card

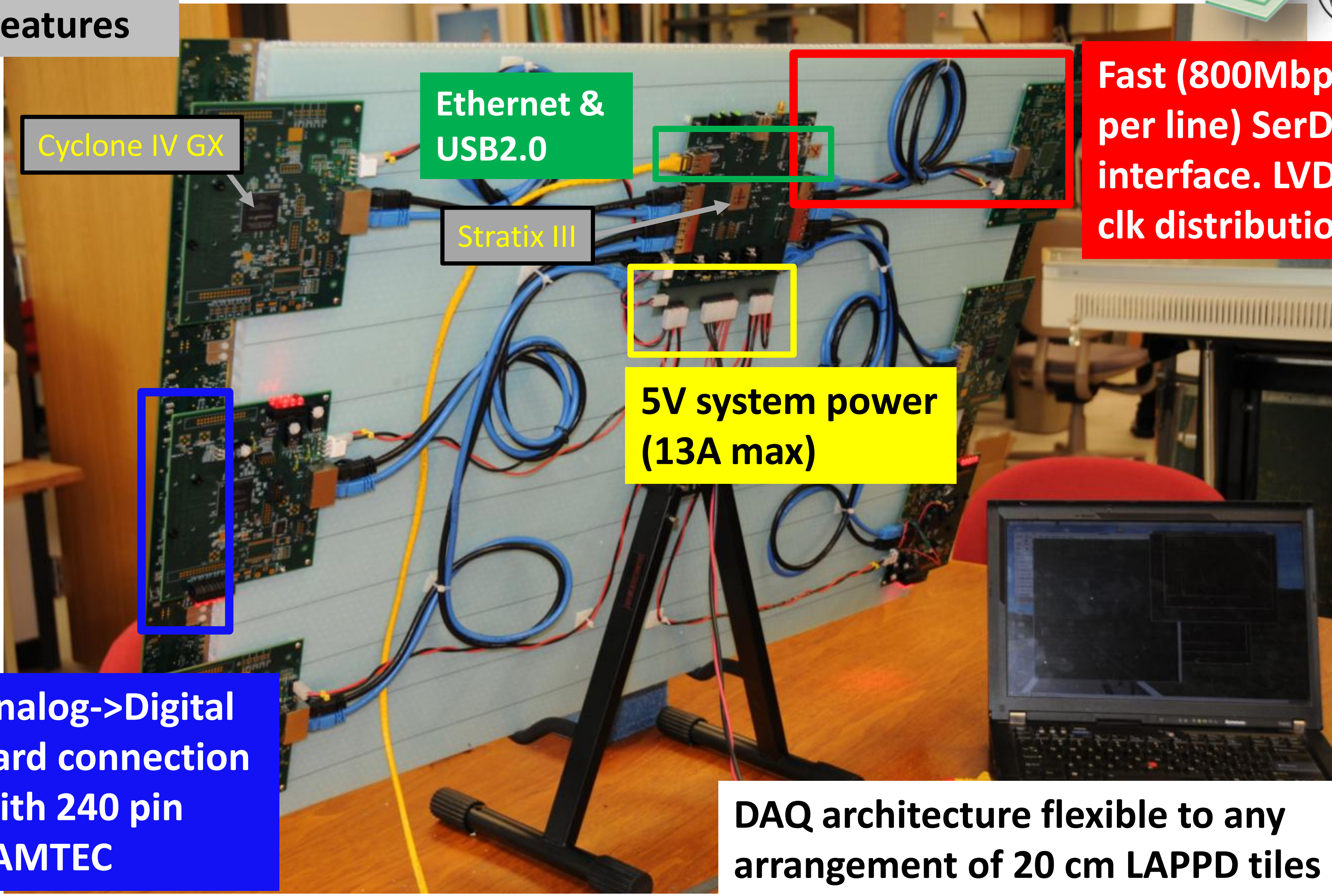
- -6 per module
- -PSEC-4 control, trigger handling, local data reduction & calibration
- -Jitter cleaner for ASIC clock distribution

Central Card

- -System control
- -Communication w/ other SuMo detectors
- -Feature extraction
- -CPU/GPU interface (Triple Speed Ethernet & USB 2.0)

Super Module DAQ

Features



Super Module DAQ Status

- **Full system readout of raw data via USB 2.0 has been achieved.**
- Upcoming:
  - -Ethernet development
  - -Event Display
  - -Implement first data reduction algorithms

System `Protocols':

- 48 bit system instruction set
- USB raw data packets 256 x 16 bit (1 channel PSEC-4) + 4 x 16 bit header/footer
- System trigger + resets along dedicated LVDS line
- 40MHz system clock

Electronics Instruction Set

The electronics use a fixed-width 48 bit instruction set. The first 4 bits are the next 6 bits are the channel mask, the next 11 bits are options, and the last 16

INS	DC	PSEC4	CHAN	OPTS	VAL
0010	001111	01110	111111	000000000000000	000000000000

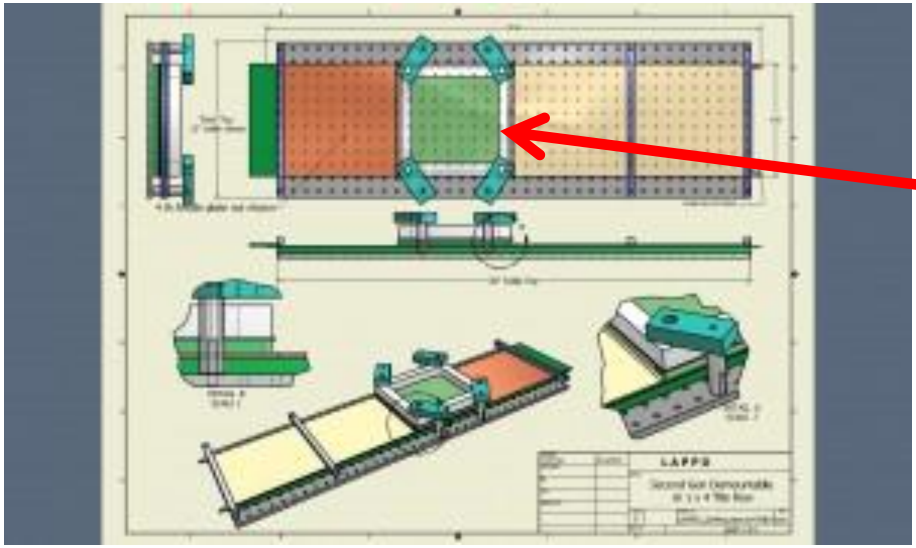
would acquire the data from the 18 central channels on each analog card.

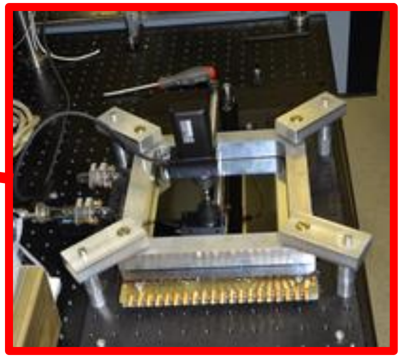
List of instructions.

Name	Hdr	Opts	Purpose
No-Op	0x0	NULL	Does nothing.
Trigger	0x1	NULL	Tells the PSEC to collect data.
Acquire	0x2	NULL	Tells the DC to pass PSEC data to DC.
Raw Read	0x3	NULL	Read the raw DC data to the CC.
Evt Read	0x4	NULL	Read the event DC data to the CC.
Get Evts	0x6	NULL	Reads VAL CC events from the CC FIFO to the PC.
Set	0x5	*	Sets pedestal and calibration values on the AC.
Reset	0xF	*	Resets components specified by opts.

(Immediate) Next Steps

- Super Module 'proof of principle' using 1x4 tile row electronics + 20 cm LAPPD MCP



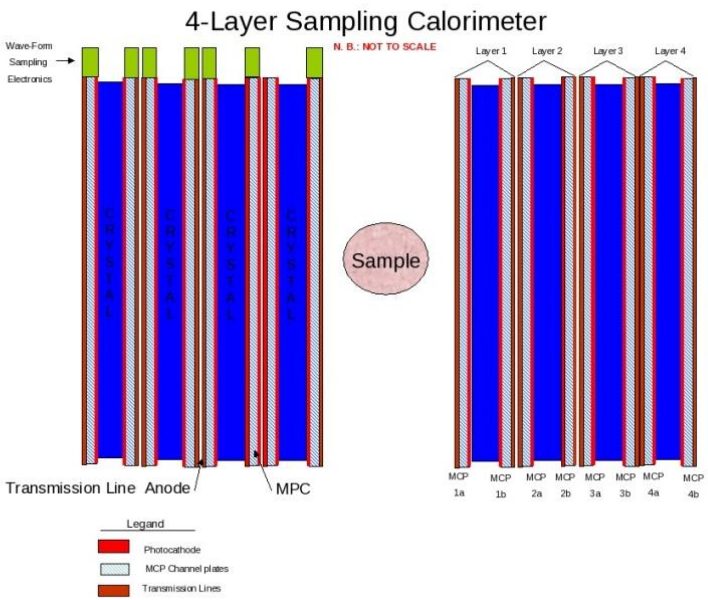


At the cusp of integrating the PSEC-4 Super Module DAQ with the LAPPD large-area MCPs. Sub-10ps resolution has been shown with MCP and ASIC separately…challenge to preserve this in a full system!

Many thanks to A. Elagin, M. Wetstein, K. Nishimura, H. Frisch, R. Northrup and the entire LAPPD collaboration

Applications?

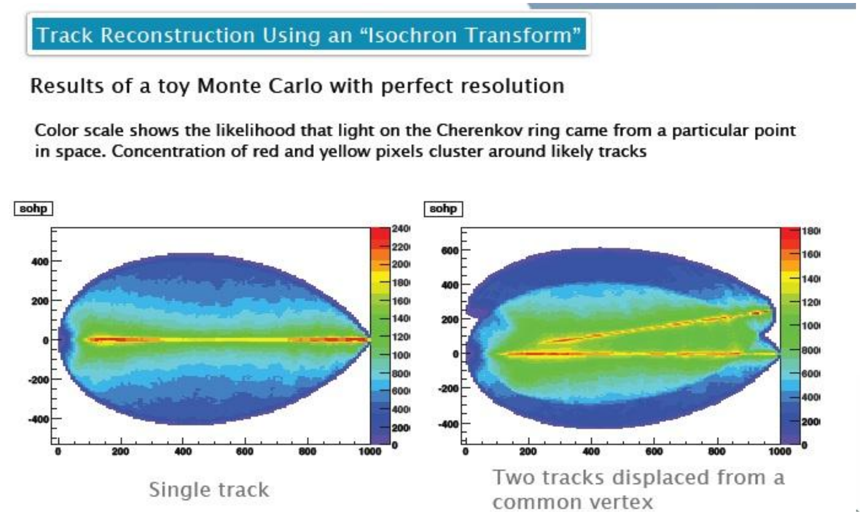
TOF PET sampling calorimeter



Approach: precise Time-of-Flight, sampling, real-time adaptive algorithms in local distributed computing, use much larger fraction of events and information

Benefit: higher resolution, lower dose to patient, less tracer production and distribution, new hadron therapy capabilities

Photon TPC – neutrino application



Δx, Δy << 1 cm
Δt < 100 psec
Magnetic field in volume

Idea: to reconstruct vertices, tracks, events as in a TPC (or, as in LiA).