Development of Large Area, Pico-second Resolution Photo-Detectors and associated Readout Electronics

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***Abstract*– The Large Area Pico-second Photo-Detectors presented in this contribution integrate a photocathode, glass capillary micro-channel plates (MCP) activated by atomic layer deposition (ALD) of independent layers of secondary electron emitter and resistive materials, and collecting anodes. Applications range from medical imaging (positron emission tomography) to tracking and calorimetry for high energy physics experiments. These devices are read out from both ends of a set of GHz-bandwidth transmission lines. This allows daisy-chaining of multiple devices to achieve large area detectors with time resolutions on the order of 10-100 pico-seconds and position resolutions of less than one millimeter in each of two spatial dimensions. First tests with pairs of small glass capillary have demonstrated gains of 10^5 to 10^7. A new 6-channel ASIC has been designed in 130 nm CMOS technology to sample and digitize detector data. This ASIC can sample at 15 GS/s with an intrinsic analog bandwidth above 1.5 GHz, and digitizes 1280 cells in parallel in two micro-seconds with 12-bit resolution. Digital signal processing of sampled waveforms from MCP devices is expected to achieve timing and position resolutions comparable to those obtained with digital oscilloscopes.**

I. Introduction

MICRO-CHANNEL PLATE based photo-detectors [1][2] are efficient tools to detect levels of signals down to single photo-electrons, with pico-second timing and sub-millimeter space resolutions for larger signals. This contribution presents developments toward large area detectors, with 1 to 100 pico-second timing resolutions depending on dimensions (present detectors are 20 x 20 cm^2), and position sensing down to a few hundreds of microns through use of GHz-bandwidth transmission lines. Signals from these transmission lines will be recorded by a 6-channel waveform digitizing readout ASIC, PSEC-4, which has been prototyped in 130 nm CMOS technology [3].

Innovative techniques such as atomic layer deposition (ALD), packaging under vacuum without electrical feedthrough pins, ASIC technology for the implementation of fast analog memories and associated analog to digital converters and advanced signal processing methods are planned to help achieve this goal at reasonable costs in production.

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II. Photocathodes

Alkali (potassium, sodium and cesium) photocathodes are presently developed at the UC Berkeley Space Science Laboratory and the Brookhaven National Laboratory Center for Functional Nano-materials, taking benefit of existing growth and diagnostics facilities such as mass spectrometry, X-ray photoelectron spectrometry, X-ray diffraction, low energy electron diffraction, and standard STM/AFM techniques. Models are developed with feedback from measurements to predict work functions and quantum efficiencies.

III. Micro-channel plates

The devices consist of two borosilicate glass plates (provided by Incom), each having 80 million pores of 20 μm diameter. These pores are tilted by 8° with respect to the plate surface, with a ratio of channel length to channel diameter of 60. The plates are separated by a thin spacer to obtain an overall gain in the range of 10^5 to 10^7.

The plates are functionalized using ALD which allows controlled deposition of secondary emitters. A resistive layer of controlled conductivity is also deposited. Resistive spacers control the three gaps:

- Photocathode to first MCP entrance,
- First MCP output to second MCP entrance,
- Second MCP output to anodes.

Fig. 1. Chamber for tests under vacuum with a 20 x 20cm^2 glass tile patterned with transmission lines and a holder for a 33mm diameter MCP (mock tile MCP).

The spacers will be processed with ALD to incorporate the resistances providing the bias voltages. The two faces of the plates are covered with a conductive layer where the high voltage biases are applied. A vacuum chamber for 20 x 20cm^2 devices is shown in Figures 1 and 2. Figure 1 also shows a holder for an MCP of 33mm in diameter.

Fig. 2. 20 x 20 cm^2 vessel made of glass, and anodes.

A mock-up of a 6-tile panel is shown Figure 3, with the electronics cards intended to sit behind the plates.

Facilities for testing of photocathodes and MCPs have been set up at the Femto-second Laser laboratory at the Advanced Photon Source at the Argonne National Laboratory, and at the Space Science Laboratory in Berkeley.

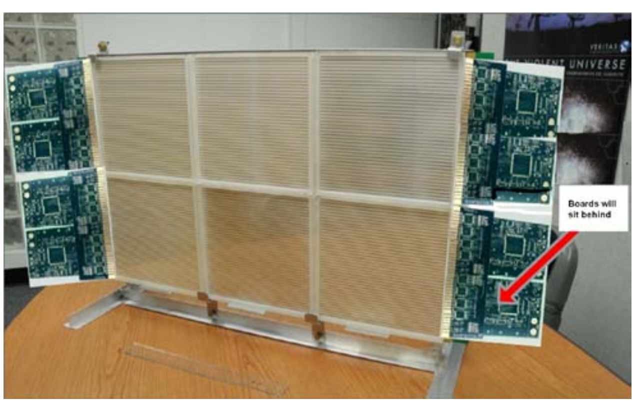

Fig 3. A panel of 6 tiles of 60 x 40 cm^2. The anodes are daisy-chained as 60 cm long transmission lines with timing readout at the two ends.

V. Transmission line anode readout

The introduction of transmission-lines anodes with time measurements taken on each end provides the ability to cover large areas and yet retain good time resolution, two attributes that are typically mutually exclusive. Since the MCPs provide fast signals with sub-nanosecond rise-times, the propagation of these signals along anodes patterned as transmission-line can provide both pico-second timing and sub-millimeter position in the two dimensions. Moreover, the transmission line geometry makes it possible to daisy-chain detectors and propagate signals on long distances maintaining this position resolution.

Each strip line is composed of metal traces on one side and a ground plane on the other side, with borosilicate glass in between. The impedance of the line depends on the ratio of the width of the strip to the vertical spacing, as well as the dielectric constant of the glass.

Figure 4 shows signals measured with a 25 μm pores MCP from Burle-Photonis for various high voltage values. Figure 5 shows the first signals obtained from an MCP functionalized with ALD and measured at Argonne National Laboratory.

Figure 5 shows the first signals which have been obtained at either end of an anode implemented as a transmission line on borofloat glass, the first stage being a 33 mm diameter MCP, the second stage being a 20x20 cm^2 MCP with 40-μm pores that was functionalized with ALD. The MCPs are positioned as shown in Figure 1.

The signal waveforms in these two figures are qualitatively similar, although the pore size, high voltage, and number of photo-electrons are different.

Measurements using Rogers 3054 high frequency ceramic as dielectric have shown that the transmission lines can have an impedance matched to 50 Ohms. A differential timing resolution of 2 ps has been obtained with a photocathode MCP signal of 158 photo-electrons, digitized with a Tektronix TDS6154C oscilloscope and analyzed with digital signal processing. This corresponds to a longitudinal position accuracy of 100 μm.

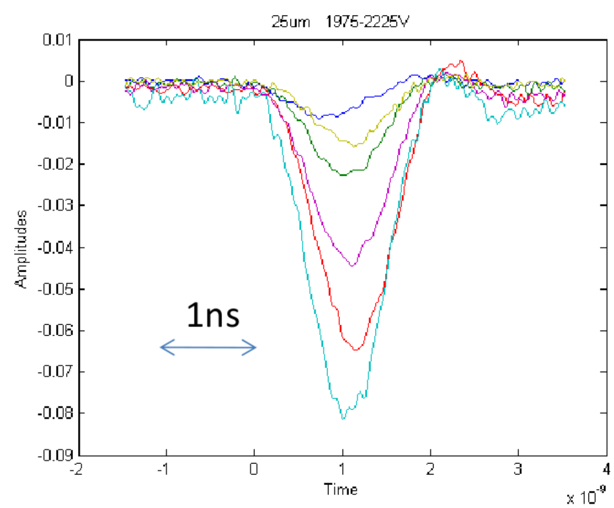

Fig. 4. Signals from MCPs with pore diameters of 25μm (Burle-Photonis), for an input of 18 photoelectrons.

VI. FRONT-END ASIC

The pulse waveform is sampled using a switched capacitor array of 256 cells operating at 10 GS/s sampling rate with > 1 GHz analog bandwidth. Upon a readout request, all samples are digitized in parallel, using on-chip Wilkinson ADCs capable of a 12-bit conversion in 2 µs. These features have been implemented in a deep sub-micron CMOS technology (IBM 130 nm) available as multi-project wafers (MPW) from the academic facility MOSIS. After digitization, which can be triggered by either a system or channel trigger, further signal processing allows accurate extraction of charge, amplitude, and time [4-7]. Such signal processing can be used to calibrate the front-end ASIC gain, bandwidth, and the transmission line propagation velocity.

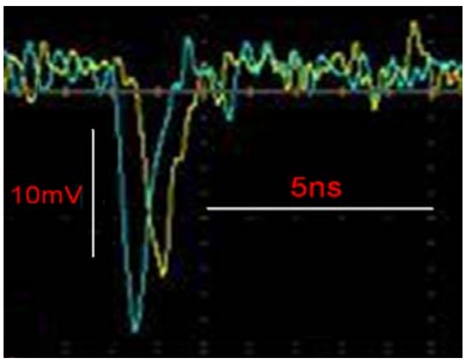

Fig. 5. First signals produced at either end of one anode implemented as a transmission line on borofloat glass. The anode reads out a signal from a two-stage device, the first a 33 mm diameter MCP, the second a 20x20 cm^2 MCP with 40-µm pores that was functionalized with ALD.

Figure 6 shows a sketch of the assembly of the anodes for a 20 x 20 cm^2 MCP coupled to traces drawn on FR4 connected to the sampling readout ASICs, all matched to 50 Ohms. A picture of the ASIC is shown in Figure 8.

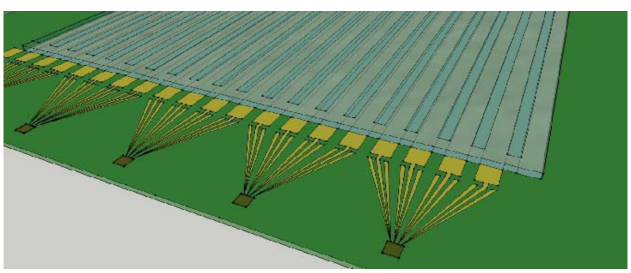

Fig. 6. Sketch of the planned readout layout showing the strip line anodes and their connection to the front-end ASIC electronics.

Figure 10 shows the front-end ASIC test cards. Each includes five analog inputs, a clock input, one front-end PSEC-4 ASIC, the FPGA managing the ASIC control signals and data transfers, and the USB interface to a laptop running the test software.

The measured noise induced by the sampling process is less than 1 mV RMS. Sampling rates up to 15 GS/s and an analog bandwidth of 1.5 GHz has been obtained with this ASIC.

The measured dynamic range is 1 V, limited by the supply voltage of 1.2 V used in this 130 nm CMOS technology.

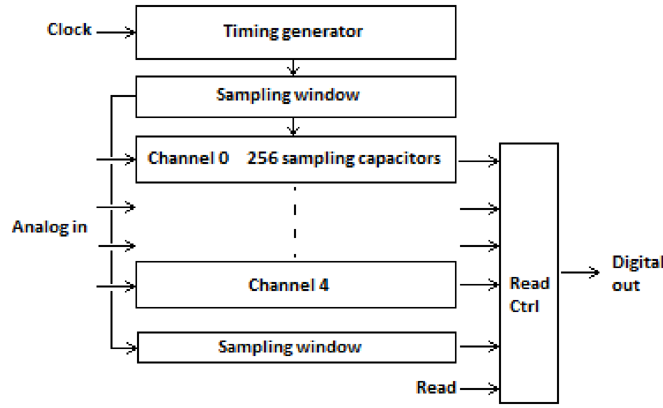

Fig.7. Block diagram of the front-end ASIC showing the 15 GS/s timing generator, five input channels, and a timing calibration channel storing the sampling window.

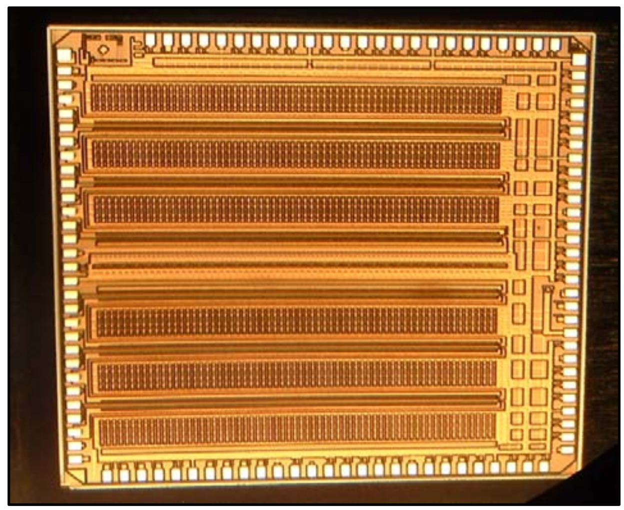

Fig. 8. A photograph of the 6-channel PSEC-4 front-end ASIC.

	ACTUAL PERFORMANCE
Sampling Rate	2.5-15 GSa/s
# Channels	6
Sampling Depth	256 points (17-100 ns)
Input Noise	<1 mV RMS
Analog Bandwidth	1.5 GHz
ADC conversion	Up to 12 bit @ 1.5 GHz
Dynamic Range	0.1-1.1 V
Latency	2 µs (min) – 16 µs (max)
Internal Trigger	yes

Table 1. Measured performance of the PSEC-4 ASIC.

VII. SUMMARY

Large area micro-channel plate detectors and their associated readout electronics are being designed and evaluated for imaging and pico-second timing applications where accurate time of flight is needed such as large detectors used in high energy physics, medical imaging, new acceleration techniques, and security applications.

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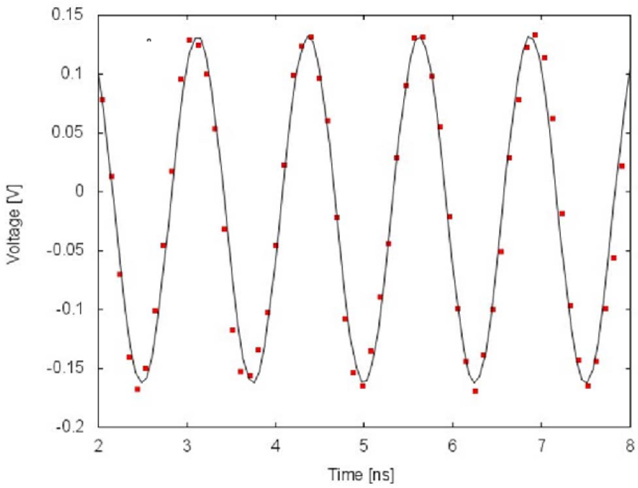

Fig. 9. A 800 MHz sine wave signal recorded at 10 GS/s with the PSEC-4 ASIC. Red: digitized data, blue: best fit sine wave.

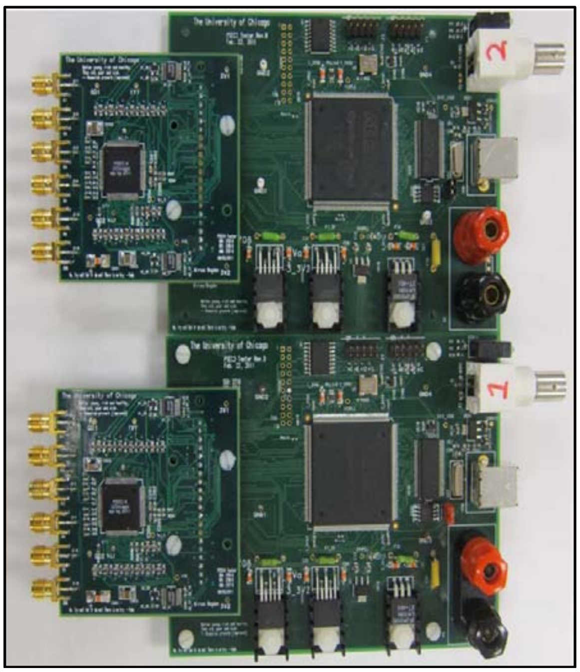

Fig. 10 Photograph of two PSEC-4 ASIC test cards.

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