A 6-Channel Fast Waveform Sampling ASIC in 0.13µm CMOS technology

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Abstract

We describe here the design characterization of PSEC-4: a custom analog and digital integrated circuit designed in the IBM-8RF 0.13 µm process intended for fast (>10 GSa/s), low-power waveform digitizing. As part of the Large-Area Picosecond Photo-Detector (LAPPD) collaboration, this ASIC has been designed for the front-end transmission line readout of large area micro-channel plates (MCP), among other potential applications. With 6 channels, PSEC-4 has a buffer depth of 256 analog samples on each channel, a chip-parallel 1.5 GHz Wilkinson ADC, and a serial data readout that includes the capability for region-of-interest windowing to reduce dead time. A switched-capacitor array architecture was implemented and sampling lock is possible with an on-chip delay locked loop (DLL) with a measured jitter of better than 15 ps. Chip performance results, including sampling rates up to 17 GSa/s, RMS noise less than 1 mV, and an analog bandwidth (ABW) of 1.6 GHz, are presented.

Principle of Operation

Sample & Hold:
- Delay line generates timing strobe with 100ps separation between cells (@ 10GSa/s):

Channel Block Diagram
- 256-sample switched capacitor array architecture
- Parallel 1.5 GHz Wilkinson digitization
- Serial data readout (token)

PSEC-4 die & Evaluation Board
- 6-channel "oscilloscope on a chip" (1.6 GHz, 10-15 GSa/s)
- Evaluation board uses USB 2.0 interface + PC data acquisition software

PSEC-4 ASIC

<table>
<thead>
<tr>
<th>ACTUAL PERFORMANCE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling Rate</td>
</tr>
<tr>
<td># Channels</td>
</tr>
<tr>
<td>Sampling Depth</td>
</tr>
<tr>
<td>Sampling Window</td>
</tr>
<tr>
<td>Input Noise</td>
</tr>
<tr>
<td>Analog Bandwidth</td>
</tr>
<tr>
<td>ADC conversion</td>
</tr>
<tr>
<td>Dynamic Range</td>
</tr>
<tr>
<td>Latency</td>
</tr>
<tr>
<td>Internal Trigger</td>
</tr>
</tbody>
</table>

PSEC-4 Results

- Digitized Waveforms
- Sampling rate : 10 GSa/s
- Sampling rate : 13.3 GSa/s

Input: 800MHz, 300 mVpp sine
- Only pedestal correction applied to PSEC-4 output
- Time-base calibrations in progress

- Sampling Rate
- Frequency Response
- Linearity
- Noise

σ ~ 0.75mV

Output

- 6-channel "oscilloscope on a chip" (1.6 GHz, 10-15 GSa/s)