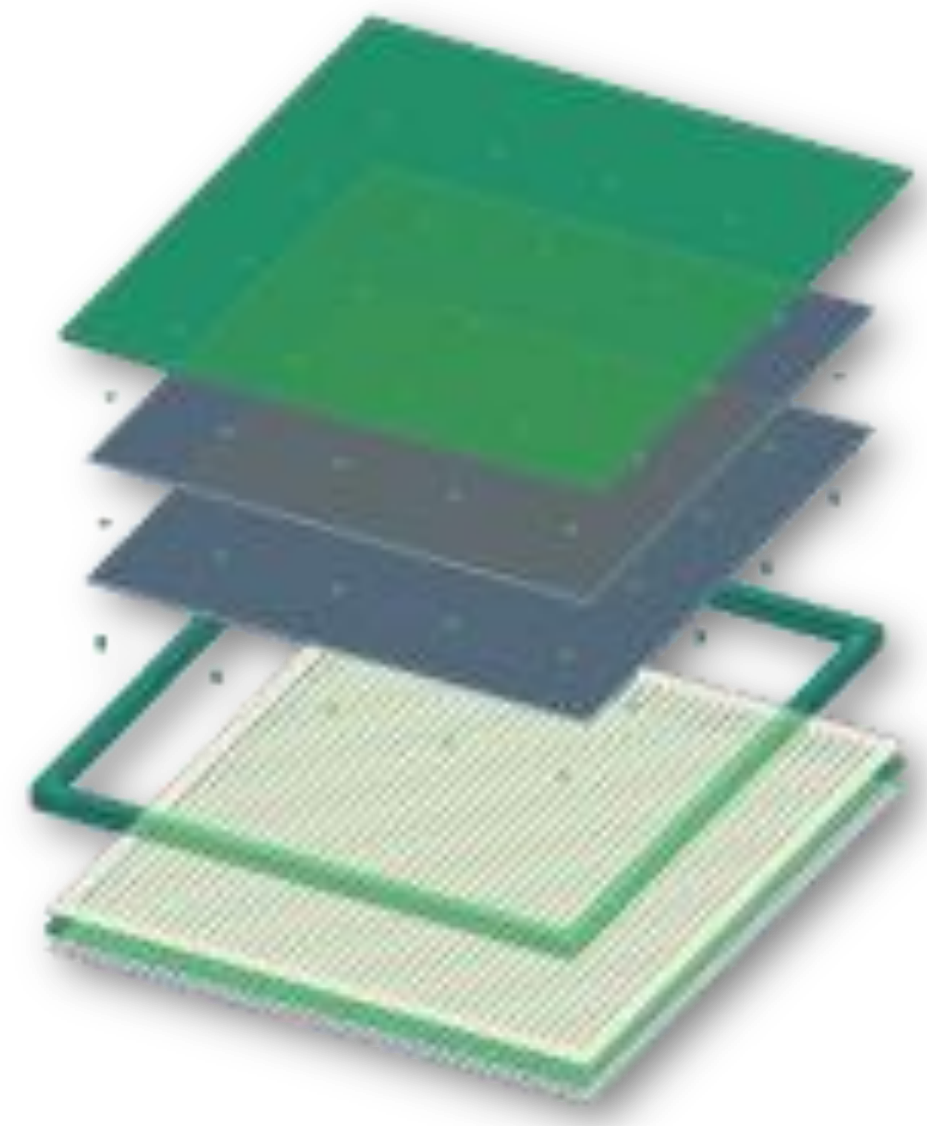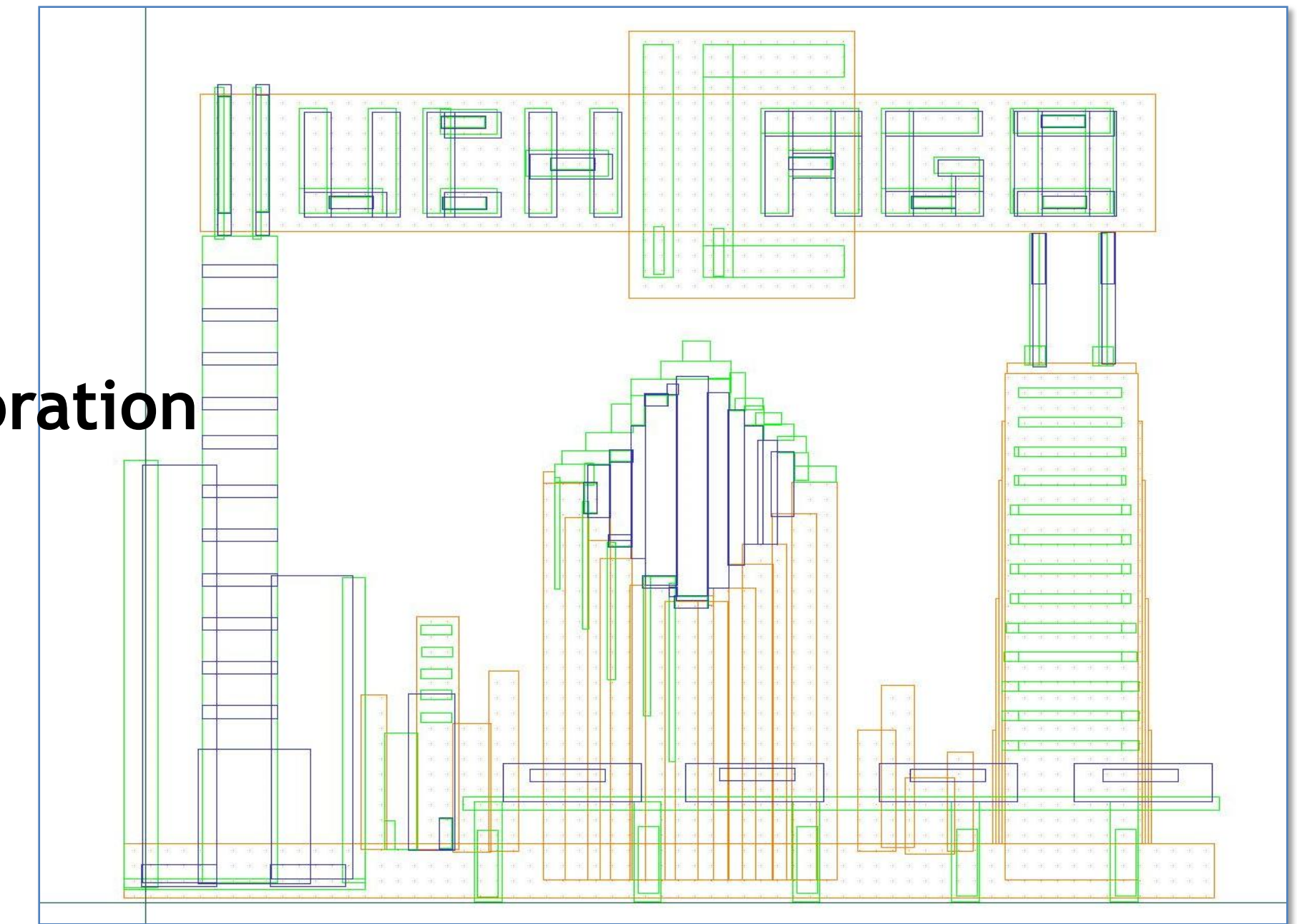# A 6-Channel Fast Waveform Sampling ASIC in 0.13μm CMOS technology

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on behalf of the Large-Area Picosecond Photo-Detectors (LAPPD) Collaboration
(http://psec.uchicago.edu)

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Abstract

We describe here the design characterization of PSEC-4: a custom analog and digital integrated circuit designed in the IBM-8RF **0.13 μm** process intended for fast (>10 GSa/s), low-power waveform digitizing. As part of the Large-Area Picosecond Photo-Detector (LAPPD) collaboration, this ASIC has been designed for the front-end transmission line readout of large area micro-channel plates (MCP), among other potential applications. With 6 channels, PSEC-4 has a buffer depth of 256 analog samples on each channel, a chip-parallel 1.5 GHz Wilkinson ADC, and a serial data readout that includes the capability for region-of-interest windowing to reduce dead time. A switched-capacitor array architecture was implemented and sampling lock is possible with an on-chip delay locked loop (DLL) with a measured jitter of better than 15 ps. Chip performance results, including sampling rates up to 17 GSa/s, RMS noise less than 1 mV, and an analog bandwidth (ABW) of 1.6 GHz, are presented.

Principle of Operation

Channel Block Diagram

- 256-sample switched capacitor array architecture
- Parallel 1.5 GHz Wilkinson digitization
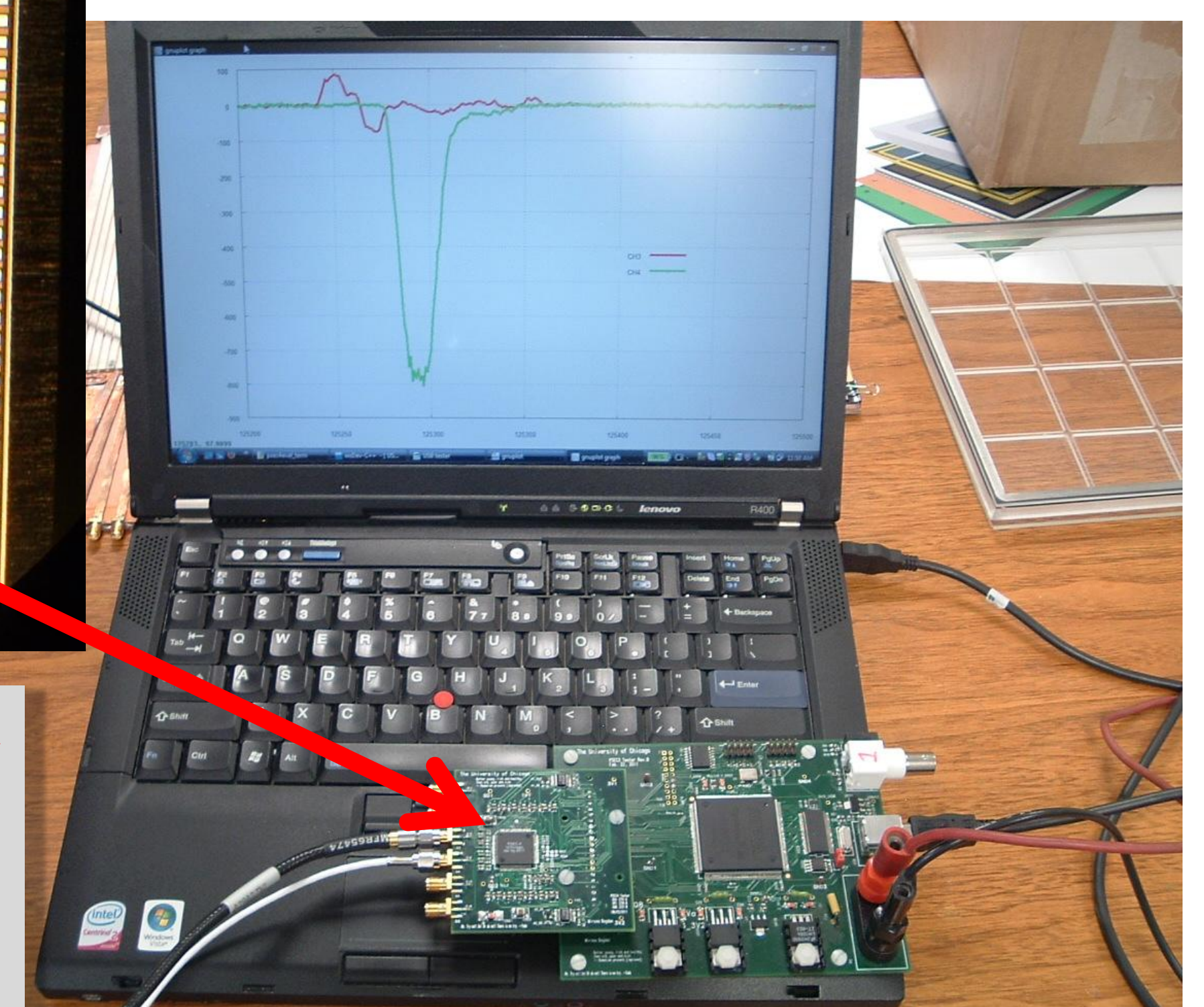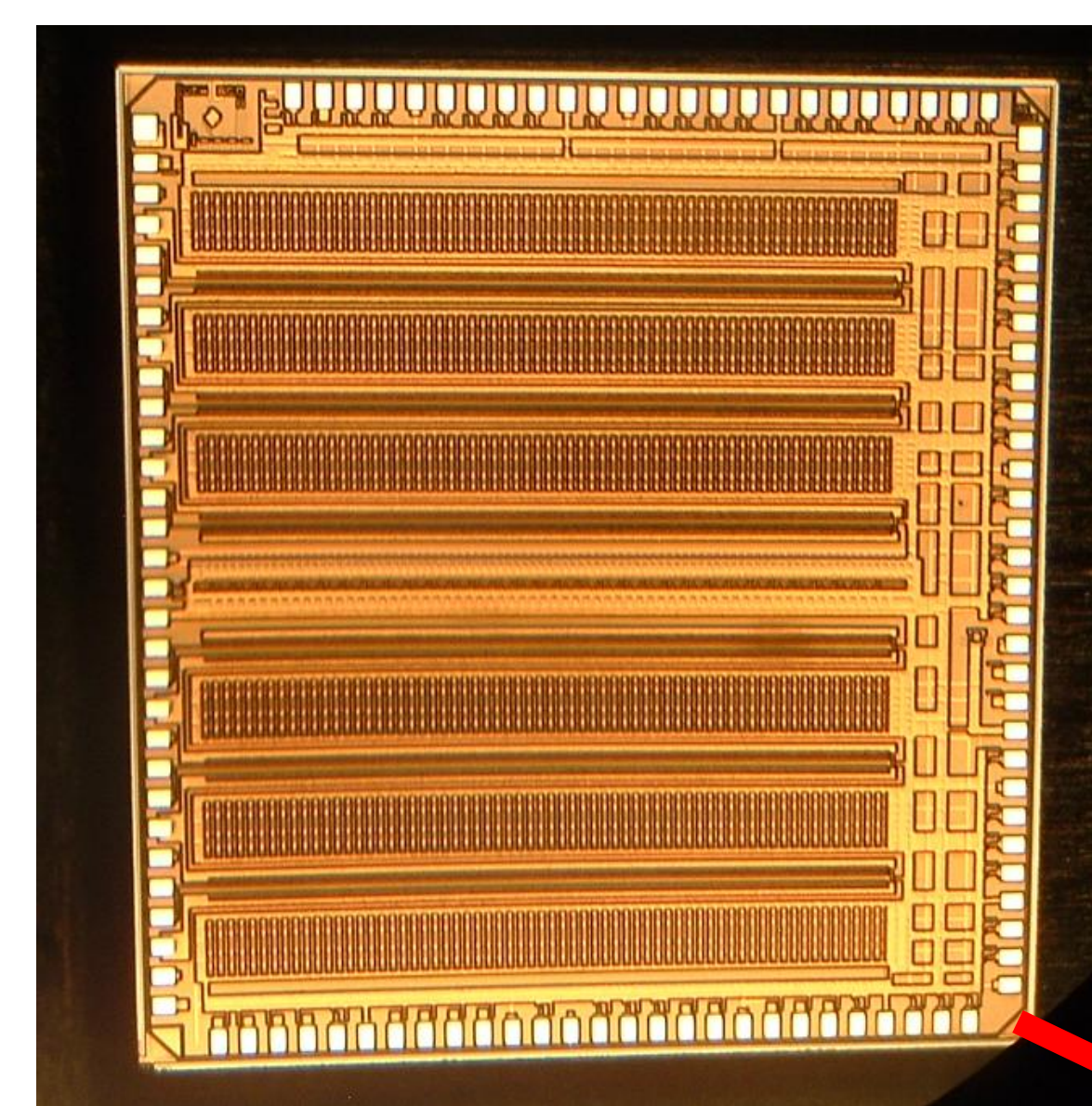- Serial data readout (token)
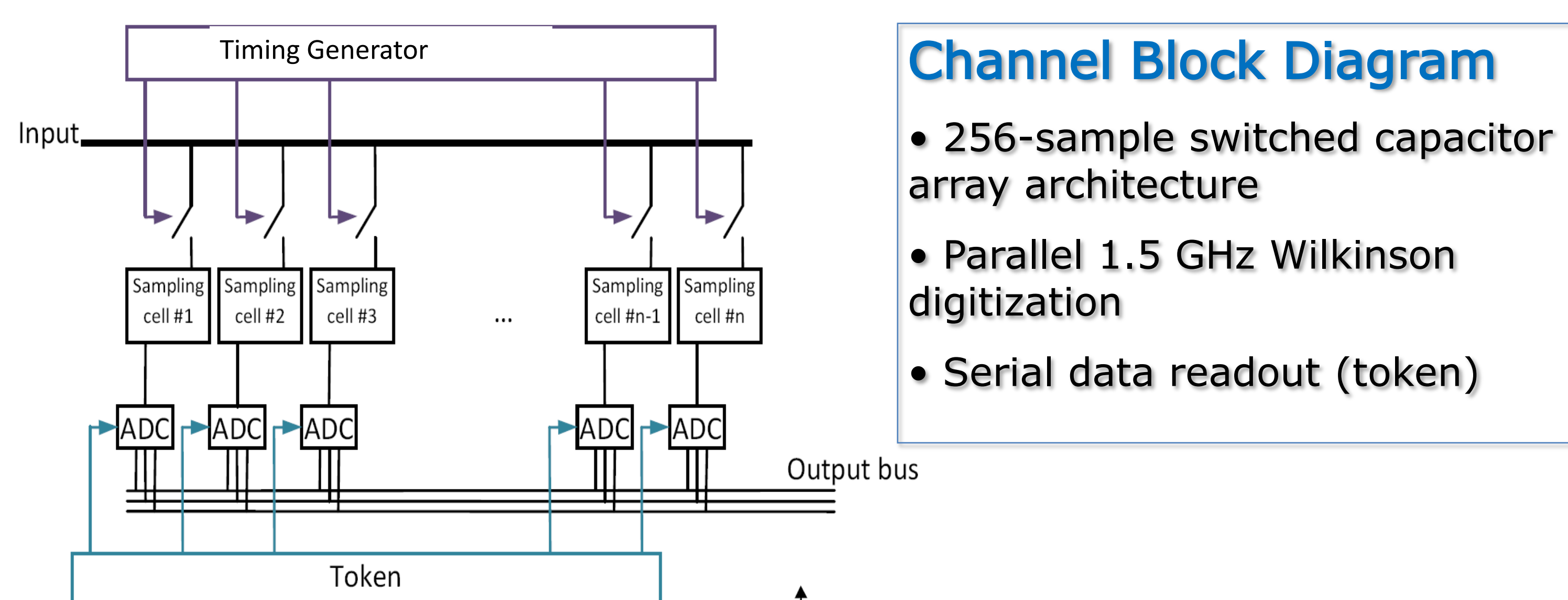
Sample & Hold:

- Delay line generates timing strobe with 100ps separation between cells (@ 10GSa/s):
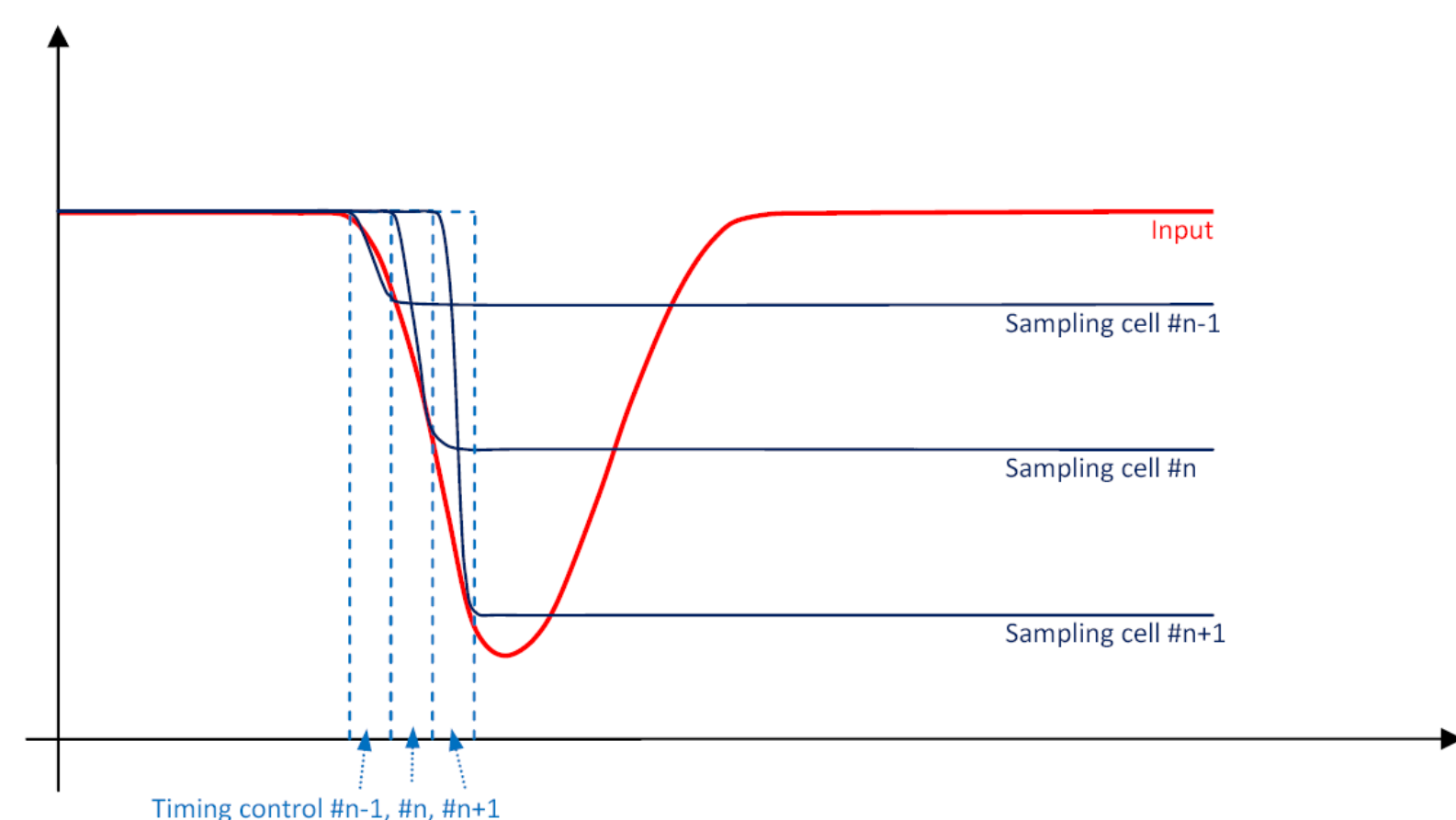
PSEC-4 die & Evaluation Board


- 6-channel "oscilloscope on a chip" (1.6 GHz,10-15 GS/s)
- Evaluation board uses USB 2.0 interface + PC data acquisition software

PSEC-4 ASIC

	ACTUAL PERFORMANCE
Sampling Rate	2.5-15 GSa/s
# Channels	6 (or 2)
Sampling Depth	256 (or 768) points
Sampling Window	Depth*(Sampling Rate)$^{-1}$
Input Noise	<1 mV RMS
Analog Bandwidth	1.5 GHz
ADC conversion	Up to 12 bit @ 1.5 GHz
Dynamic Range	0.1-1.1 V
Latency	2 μs (min) – 16 μs (max)
Internal Trigger	yes

PSEC-4 Results

Sampling Rate

Noise

$\sigma \sim 0.75$ mV
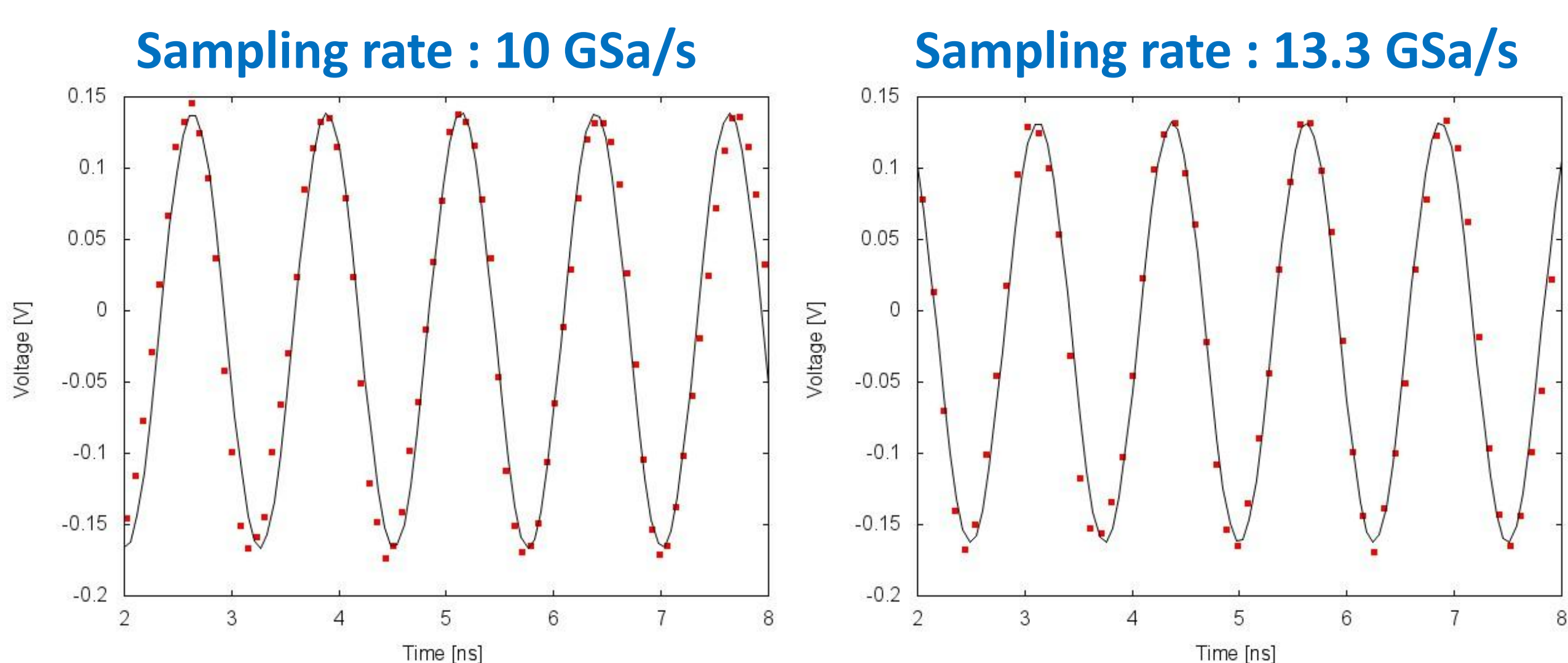
Digitized Waveforms

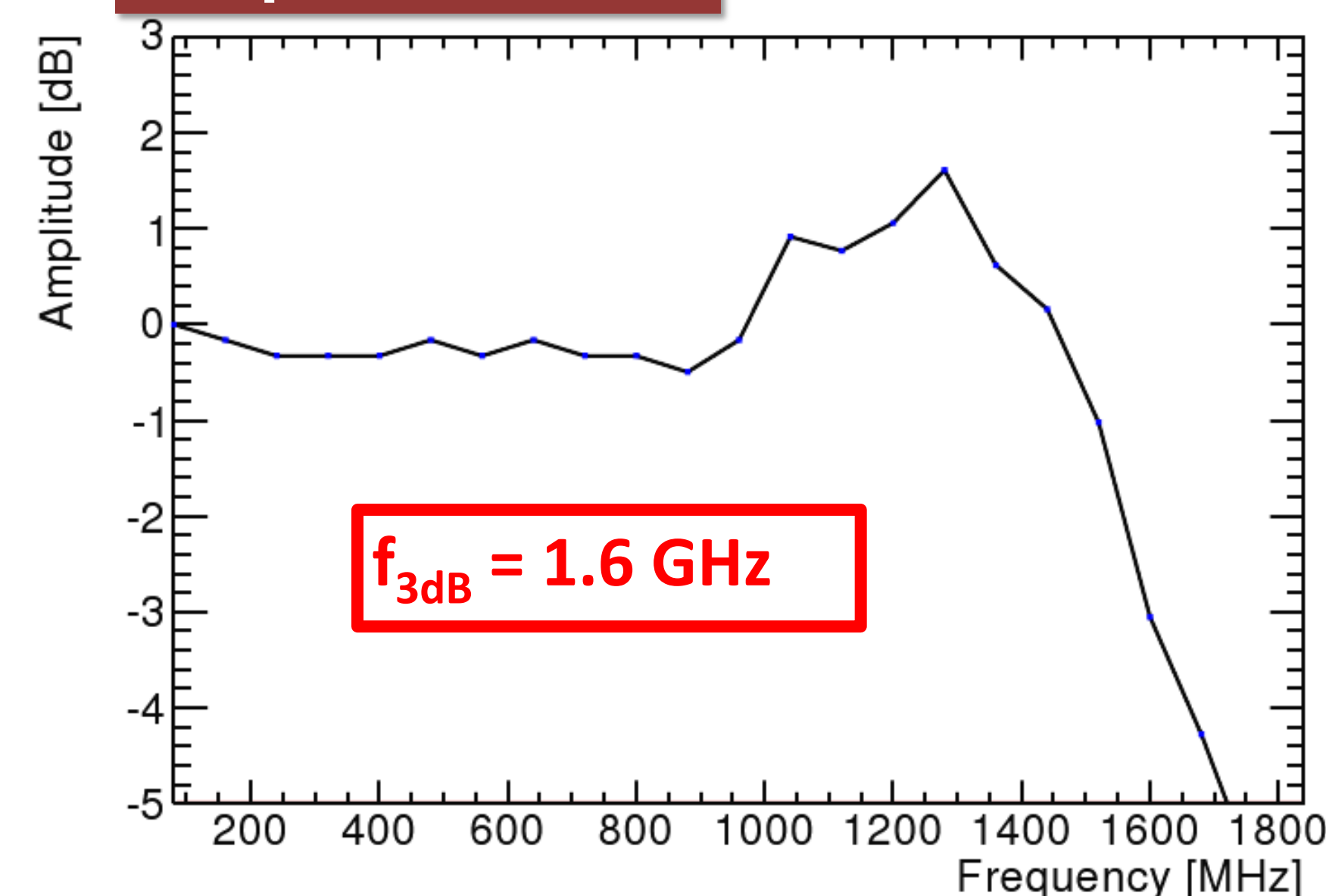#### Sampling rate : 10 GSa/s
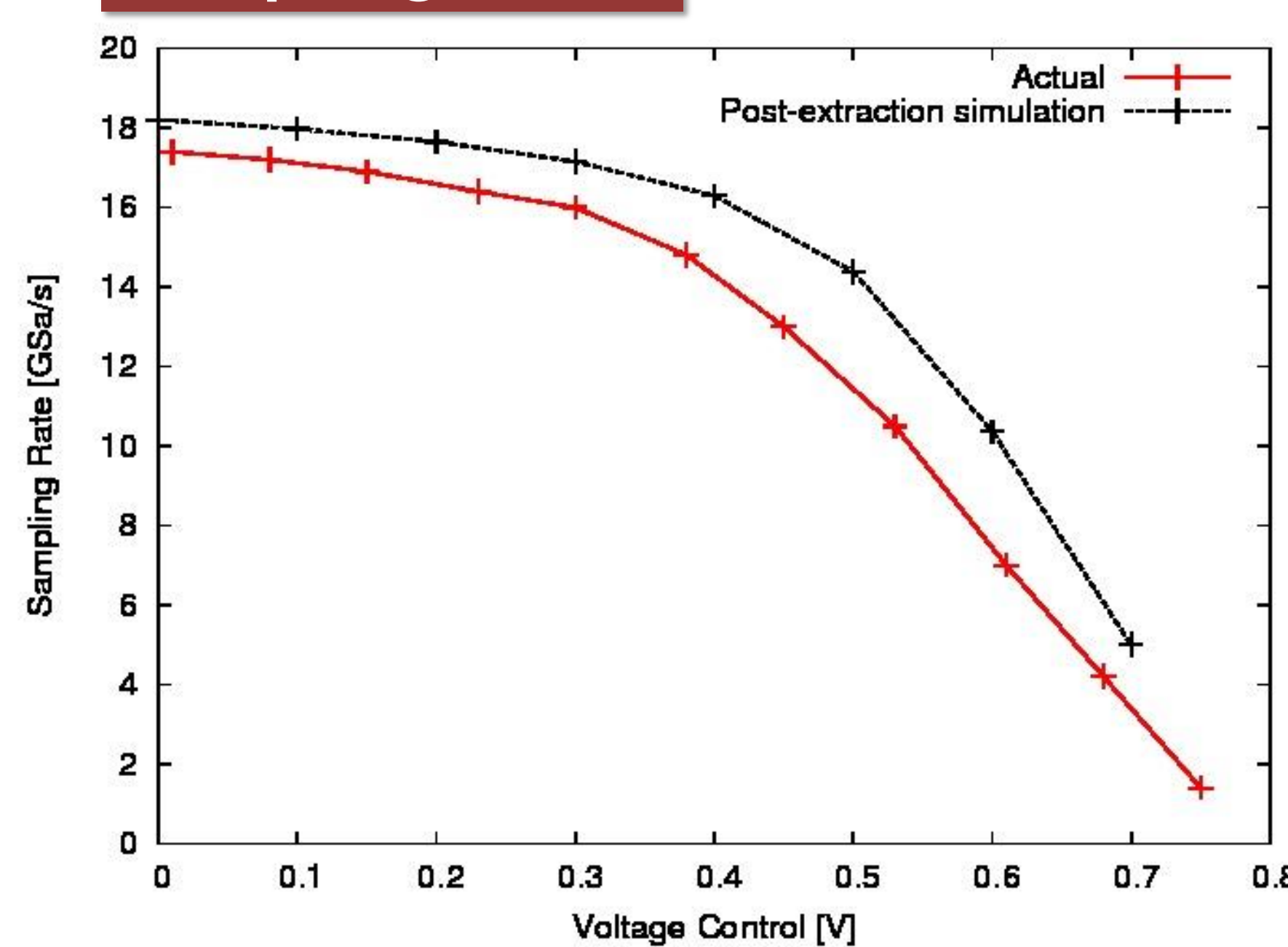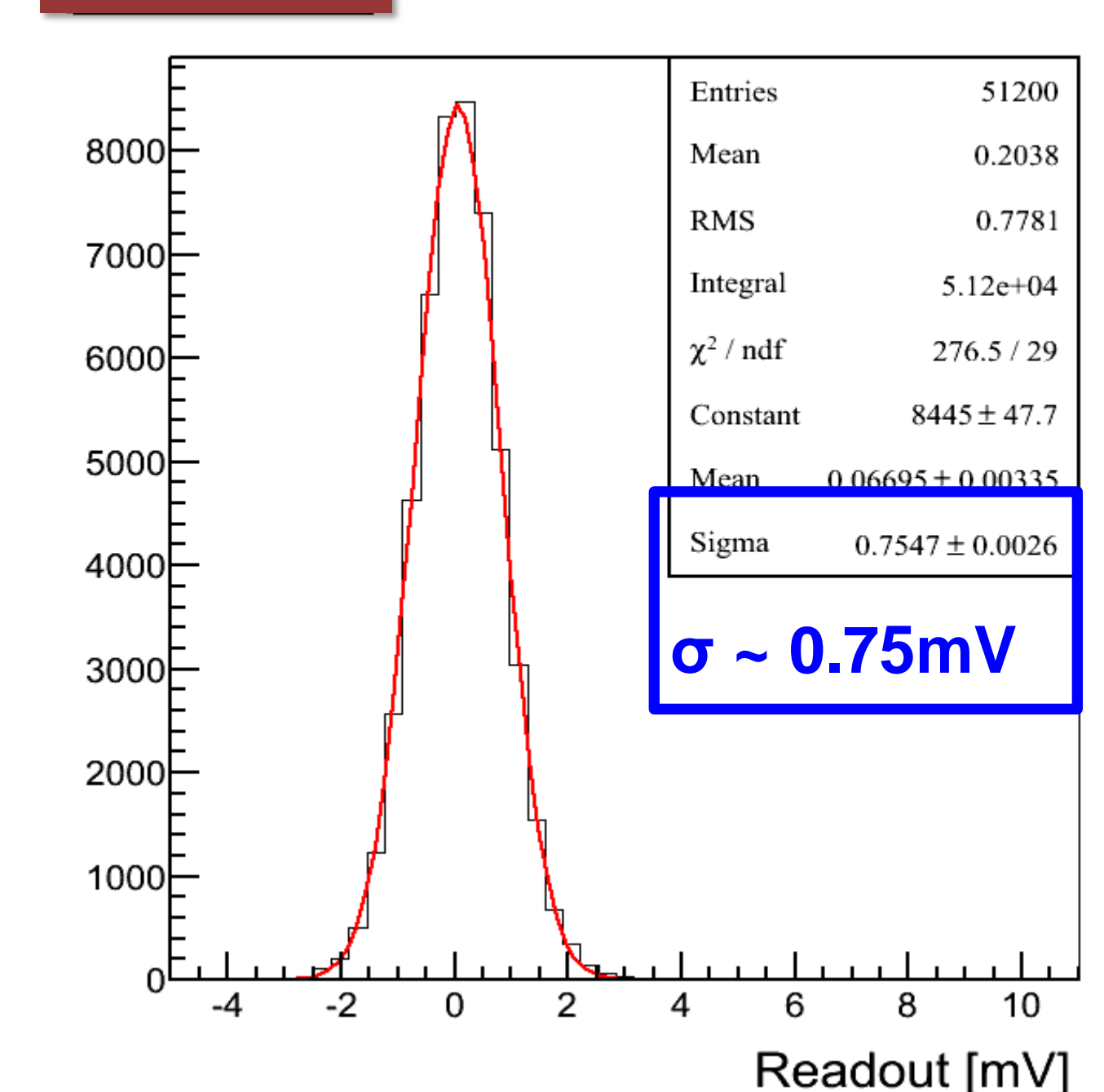
Sampling rate : 13.3 GSa/s

Input: 800MHz, 300 mV$_{pp}$ sine

-Only pedestal correction applied to PSEC-4 output

-Time-base calibrations in progress

Frequency Response

f_{3dB} = 1.6 GHz

Linearity