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A correlation-based timing calibration and diagnostic technique for fast digitizing ASICs

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Abstract

A general procedure for precision timing calibration of waveform digitizing systems is presented. Application specific integrated circuits (ASICs) implementing this functionality are increasingly used in high-energy physics as replacements for stand-alone time-to-digital and analog-to-digital modules. However, process variations cause such ASICs to have irregularly spaced timing intervals between samples, so careful calibration is required to improve the timing resolution of such systems. The procedure presented here exploits correlations between nearby samples of a sine wave of known frequency to obtain the time difference between them. As only the correlations are used, the procedure can be performed without knowledge of the phase of the input signal, and converges with smaller data samples than other common techniques. It also serves as a valuable diagnostic tool, allowing a fast, visual, qualitative check of gain mismatches between sampling cells and other ADC artifacts. Work is continuing to extend the procedure to fit for timing intervals in the face of such non-idealities.

We present both the algorithm and example calibration results from a commercial oscilloscope and the PSEC-3 ASIC. For the latter, we have also applied the calibration to improve timing resolution in the readout of a prototype microchannel plate photomultiplier tube with a stripline anode configuration.

Keywords:
switched capacitor arrays, precision timing, waveform sampling, timing calibration

1. Introduction

Waveform sampling and digitizing ASICs are becoming increasingly popular as a front-end readout solution for many high energy physics experiments [2, 3, 4]. Systems based on these ASICs digitize front-end waveforms event-by-event, in contrast to crate-based time-to-digital and analog-to-digital modules, which typically provide only a characteristic time and an integrated charge for each event. Once the full waveform is digitized, the data path is flexible, allowing the user to process waveforms with customized algorithms, or even to read full waveforms for each event. This feature of full waveform readout has led many to refer

[1]For the Large Area Picosecond Photodetector Collaboration [1]

to these ASICs as "oscilloscopes-on-a-chip," and acquisition interfaces to such systems often mimic oscilloscpe functionality. These systems can, with relatively minor effort, give performance comparable to high precision time-to-digital modules [5]. By retaining access to the full waveform, one can perform in-situ monitoring, debugging and optimization of signal processing algorithms.

These ASICs have further advantages. They are often significantly more compact than crate-based modules, allowing for large channel density and digitization of signals very close to the detector. They can be designed with a specific detector or class of detectors in mind, and allow a degree of customization not available in many commercial modules, such as satisfying low-power requirements or the addition of on-chip front-end amplification.

Although waveform digitizing is an extremely powerful tool, it takes a significant effort to turn a series of raw ADC counts that these ASICs produce into a stream of time-voltage pairs that accurately represents the input waveform. In this paper, we describe a technique that can be used to calibrate the timing of these ASICs, based on measurements of correlations between the voltages in pairs of sample points when a sine wave of known frequency is applied as an input. This procedure converges with relatively small sample sets, and this technique provides helpful visual feedback to quickly locate and diagnose malfunction or non-idealities of the waveform digitizer. This technique was developed to calibrate time delays of waveform sampling ASICs, but is equally applicable to any waveform sampling system with fixed time offsets: for example, interleaving of commercial ADCs to effectively increase sampling rates.

Initial tests of this technique have been conducted on a fast oscilloscope, where the timing delays between samples are assumed (and verified) to be precisely calibrated by the manufacturer. We have also performed the calibration procedure on the PSEC-3 ASIC, which has been developed as part of the Large-Area Picosecond Photo-Detector (LAPPD) Project [6]. This project aims to produce large-area microchannel plate photomultiplier tubes (MCP-PMTs) with excellent timing resolution, allowing for affordable, high-performance instrumentation of a wide variety of detectors in collider, neutrino, and medical applications, among others. The PSEC-3 is designed to digitize pulses from stripline anodes of an LAPPD device. We report preliminary results on the calibration of the PSEC-3, including a measurement of timing resolution for data taken with a prototype stripline MCP-PMT, both before and after this calibration is applied.

2. Timing Calibration with Correlated Sampling

A number of calibrations are required before the raw data from a waveform sampler or digitizer can be considered a true representation of the input waveform. Among the most common calibrations are the following:

1. Voltage calibration - Raw ADC counts must be converted to voltage, either by a linear scaling factor or a nonlinear formula or lookup table.
2. Pedestal correction - Each sampling cell has a characteristic DC voltage offset, which must be subtracted from the cell's voltage value.
3. Time-base correction - The average sampling rate over the full array must be determined, as well as the individual timing offsets from sample to sample. Due to process variations in ASIC fabrication, these offsets can vary by tens of percent from the nominal interval [3]. If one ignores these variations and assumes the nominal sample time between all cells, waveforms can be systematically misreconstructed, as shown in Figure 1.

Our procedure is designed to handle item 3 above, though it is also capable of determining the pedestal voltages described in item 2. We require that the voltage calibration in item 1 has already been handled, or that the ADC values are either perfectly linear. If this condition is not satisfied, this method can still give valuable feedback into the ADC performance, but may not be suitable to accurately determine time delays between samples.

The general problem of timing calibration is to determine the time difference between two sampling points, i and j, with a delay between them, $\Delta t_{ij} = t_i - t_j$. These two samples may be adjacent in time, but

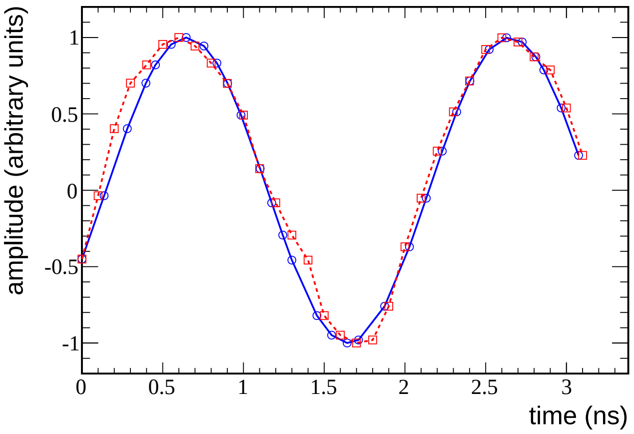

Fig. 1. Simulated sampled points of a 500 MHz sine wave at their proper temporal locations (blue - circles and solid line), and misreconstructed by assuming nominal time spacing between all cells (red - squares and dashed line). The nominal sampling rate is 10 GSa/s, and the true delays between samples are Gaussian distributed with $\sigma_{\Delta t}/\Delta t_{\text{ave}} = 30\%$. Lines between points are based on linear interpolation.

this is not a requirement. If we apply a sine wave of frequency f_{in}, we expect the following responses in each sample:

$$V_i = A sin(2\pi f_{\text{in}} t_i + \phi) + P_i$$

$$V_j = A sin(2\pi f_{\text{in}} t_j + \phi) + P_j$$

where A is the amplitude of the input sine wave, ϕ is its arbitrary phase, and P_i and P_j are the pedestal voltages for sample cells i and j. We can redefine variables and make use of trigonometric identities to obtain the following:

$$x \equiv V_i + V_j = 2A\cos(\pi f_{\text{in}} \Delta t_{ij}) \sin[\pi f_{\text{in}}(t_i + t_j) + \phi] + x_0$$

$$y \equiv V_i - V_j = 2A\sin(\pi f_{\text{in}} \Delta t_{ij}) \cos[\pi f_{\text{in}}(t_i + t_j) + \phi] + y_0$$

where $x_0 = (P_i + P_j)$ and $y_0 = (P_i - P_j)$ We then redefine the phase $\phi' = \phi + \pi f_{\text{in}}(t_i + t_j)$, leaving us with the parametric description of an ellipse, as swept out by the parameter ϕ'. The features of this ellipse give insight into the parameters of the input sine wave and, more importantly, the timing and pedestals of the sample cells themselves. One unique ellipse exists for each possible pair of sampling points.

The calibration is then performed as follows for each desired pair of sampling points. A series of events is taken with a sinusoidal input signal of well-known frequency. The phase of each event should be varied so that the full ellipse is swept out. In practice, this phase is often randomly and uniformly sampled. The parameters of an ellipse that best fits the data are determined. Our implementation utilizes the MINUIT [7] package, now built into the ROOT analysis framework [8], to minimize the χ^2 based on the sum of squares of shortest distances between each data point to the fitted ellipse. The geometrical parameters of the ellipse, the two radii (r_1 and r_2), and the center positions (x_0 and y_0), are related to the physical parameters of the sampling cells as follows:

$$r_1 = 2A\cos(\pi f_{\text{in}} \Delta t_{ij})$$

$$r_2 = 2A\sin(\pi f_{\text{in}} \Delta t_{ij})$$

$$x_0 = P_i + P_j$$

$$y_0 = P_i - P_j$$

A geometric representation of these features is shown in Figure 2. Of particular note is that although deviations from ideal behavior of the sample cells used for the correlation plots can distort the ellipse, this distortion can manifest with distinct properties easily identified by eye from the plot. For example, if the two cells have a mismatched gain, such that one is more responsive to the input signal than the other, the ellipse will appear rotated.

3. Validation

The procedure has been validated using data collected with a Tektronix TDS6804B oscilloscope, operating at 5 GSa/s. A 235 mV_{rms} sine wave input was provided by an Agilent E4428C signal generator. A total of 2000 waveforms were acquired, with 500 samples for each waveform. The ellipse fitting procedure was applied to pairs of samples to determine the time intervals between the samples. At the given combination of sampling rate and input frequency, adjacent samples could not be used for the calibration, as the ellipse collapses to a line for large values of f_{in}/f_s.[2] To compensate, fits were performed for pairs of cells separated by 10 cells, then for pairs of cells separated by 9 cells. The individual cell-to-cell delays were then calculated as $\Delta t_{i,i+1} = \Delta t_{i,i+10} - \Delta t_{i+1,i+10}$.

An example fit to a single pair of cells is shown with the corresponding data in Figure 3. The distribution of delays between single sample pairs is shown in Figure 4. The distribution of Δt values is consistent with the nominal sampling rate of the oscilloscope. The spread in these timing intervals from sample to sample is approximately 1.8 ps. We attribute the dominant contribution to this value as the 1.5 ps aperture jitter quoted in the manufacturer's datasheet.

4. Preliminary results with the PSEC-3 ASIC

This calibration procedure has also been used on the PSEC-3, a waveform digitizing ASIC that operates between 2.5 and 17 GSa/s [6]. Though the first attempts at application of this procedure to PSEC-3 data were not successful in determining timing constants, they did quickly reveal deficiencies in the datasets and operating points, all through simple visual inspection of the correlation plots. Two examples of such visual diagnostics are shown in Figure 5. This type of fast visual interpretation of the data has proven quite useful during the ongoing characterization of this chip.

A dataset was collected and successfully analyzed, consisting of a 120 mV_{pp}, 100 MHz sine wave input, digitized at 5 GSa/s. An example fit to this data and the distribution of fitted times is shown in Figure 6.

Proper calibration is vital for determining timing of fast MCP-PMT signals. Since precision timing is a primary design goal for the PSEC-3, we recorded a dataset taken with a prototype MCP-PMT with a stripline anode structure [9]. The pulses from this MCP-PMT are expected to be similar to the LAPPD devices that PSEC-3 was designed to read out. The MCP-PMT was illuminated with a 406 nm PiLas laser diode, model EIG1000D, from Advanced Laser Diode Systems. Output signals from two ends of a single anode stripline were each amplified with a MiniCircuits ZKL-1R5 amplifier, providing roughly 40 dB of gain. These amplified signals were then digitized with the PSEC-3. Timing on the digitized signals was performed using a simple software constant-fraction discrimination method. This method is implemented by first determining the minimum value of the negative-going pulse, then searching backwards from this minimum to locate the time when the voltage passes through a given fraction of the minimum, in this case 20%. This point typically falls between digitized samples, so a simple linear interpolation between the last point above this voltage and the first point below this voltage is used to determine the time of the pulse. Example digitized pulses, as well as timing resolutions obtained before and after timing calibration, are shown in Figure 7. A notable improvement was observed in timing resolution after application of the calibration constants. Work continues to improve the quality of the PSEC-3 operating point, calibration, and timing algorithm.

[2]This configuration was chosen to match that used for the PSEC-3 later in this document.

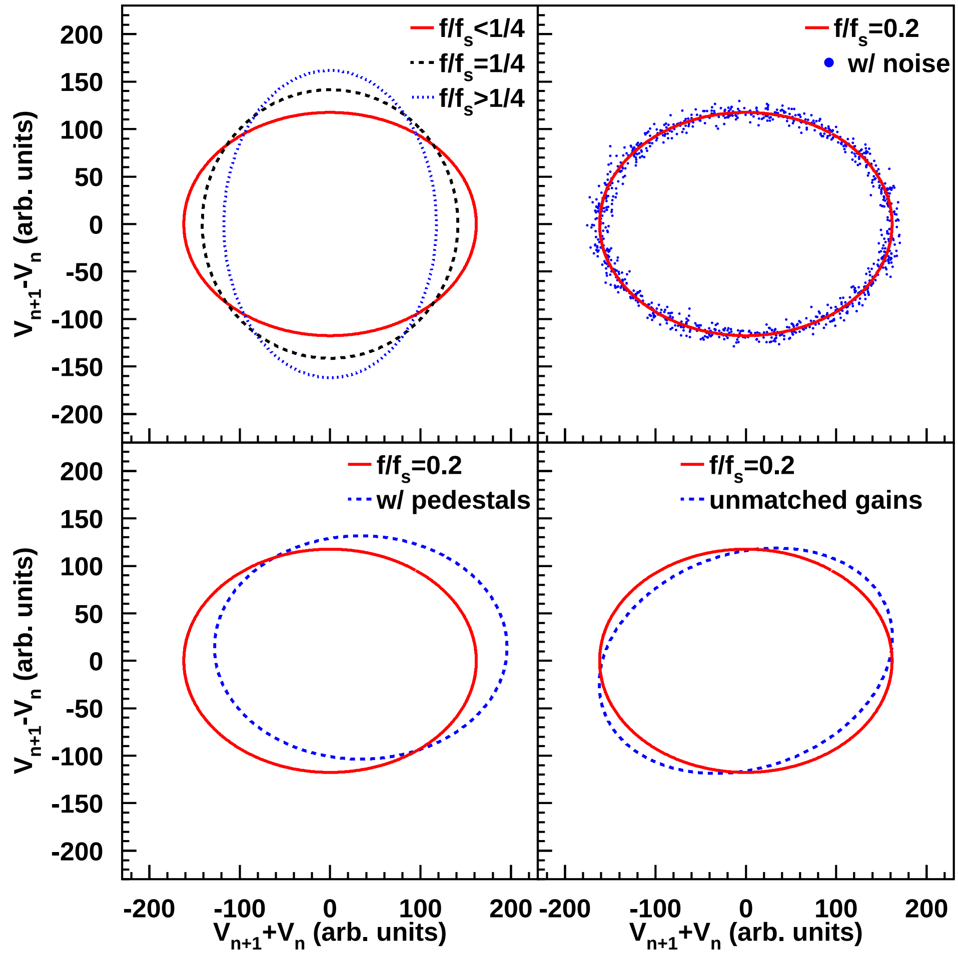

Fig. 2. Geometric effects of various parameters influencing the correlation of the sum and difference of the sine-wave induced voltages on two neighboring sampling points operating at a sampling rate f_s. (Top left) A sine wave with frequency set at 1/4 the sampling frequency the correlation produces a circle. If $f_{in}/f_s < 1/4$, the curve is an ellipse with a horizontal major axis, while for $f_{in}/f_s > 1/4$ the ellipse has a vertical major axis. (Top right) Example ellipses with and without noise. In this example, the sine wave amplitude is 25 times greater than the noise rms voltage. (Bottom left) The origin of the ellipse is shifted in the presence of pedestal voltages. (Bottom right) If the sample gains are mismatched the correlation ellipse is visually rotated. A gain mismatch of 20% is shown here.

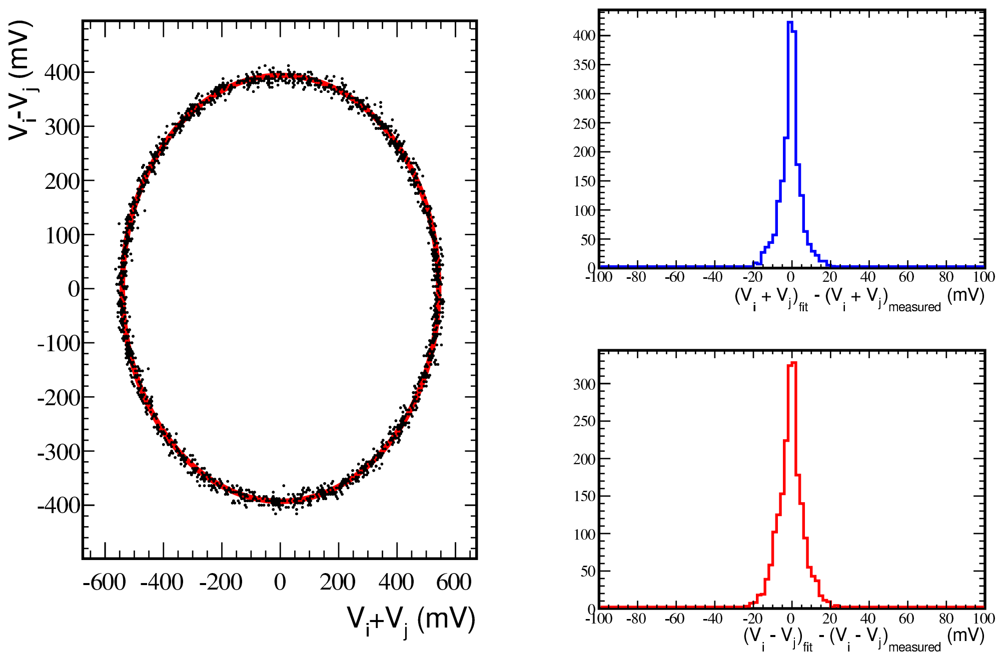

Fig. 3. (Left) An example correlation plot for the oscilloscope data (points) and the corresponding fit (solid red line). (Upper right) Residuals of the fit in the x-dimension of the left plot. (Lower right) Residuals of the fit in the y-dimension of the left plot.

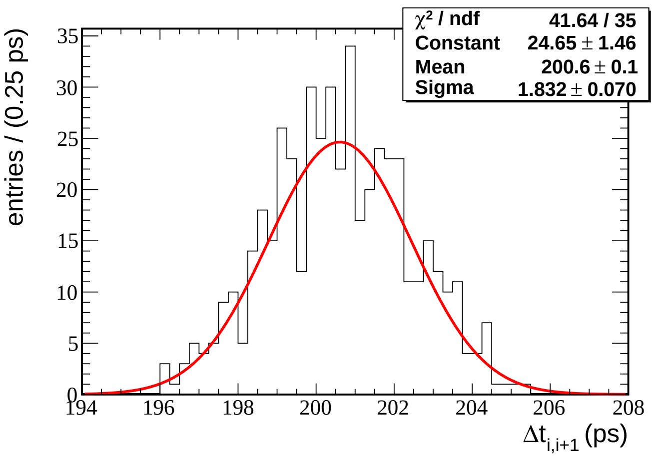

Fig. 4. Distribution of time intervals between all pairs of adjacent samples for the fast oscilloscope data. The red solid line is a Gaussian fit to the data.

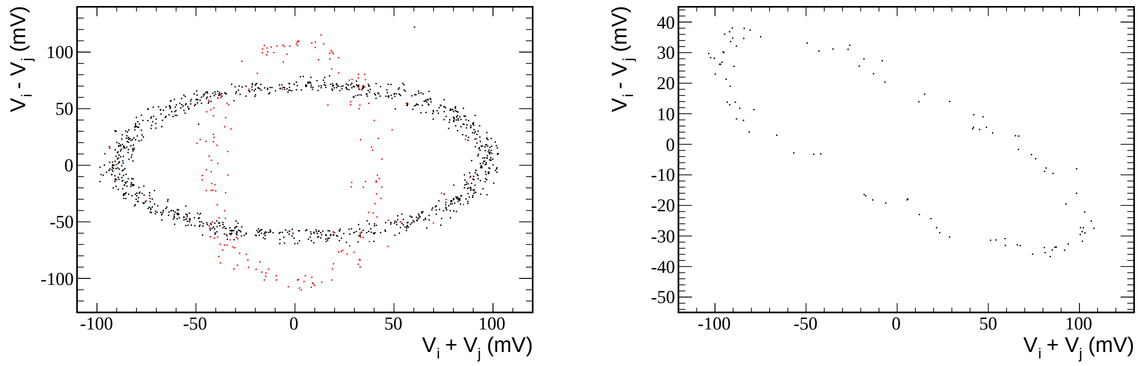

Fig. 5. (Left) A correlation plot for a PSEC-3 dataset demonstrating malfunction of the DLL controlling the sampling rate, causing fluctuation between operation at 5 GSa/s (black points) and 10 GSa/s (red points). (Right) A correlation plot for the PSEC-3 indicating significant gain variation between cells. This feature is due to the internal layout of the PSEC-3 input line.

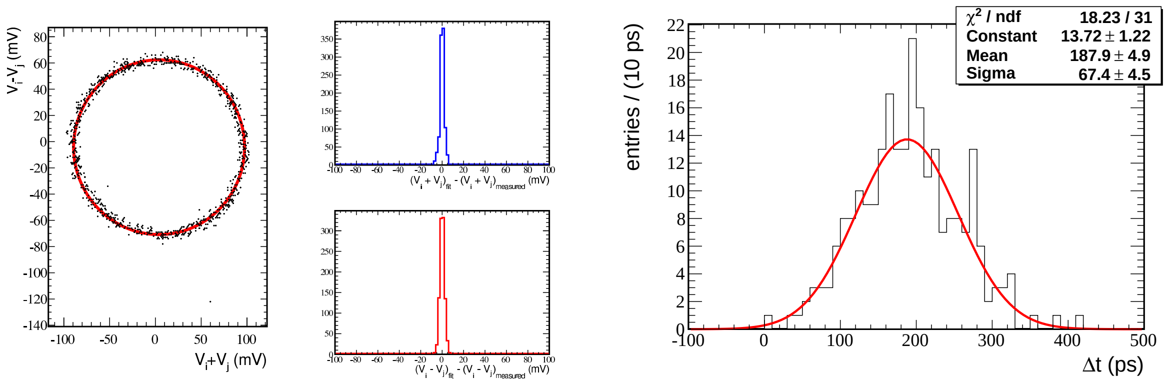

Fig. 6. (Left) A typical correlation plot for the PSEC-3, operating at 5 GSa/s with a 100 MHz input signal. Black points correspond to data and the solid red line to the best fit ellipse. (Right) The distribution of fitted Δt values for the PSEC-3. input signal. The histogram indicates the results of the fits, and the red solid line is the result of a Gaussian fit to the data.

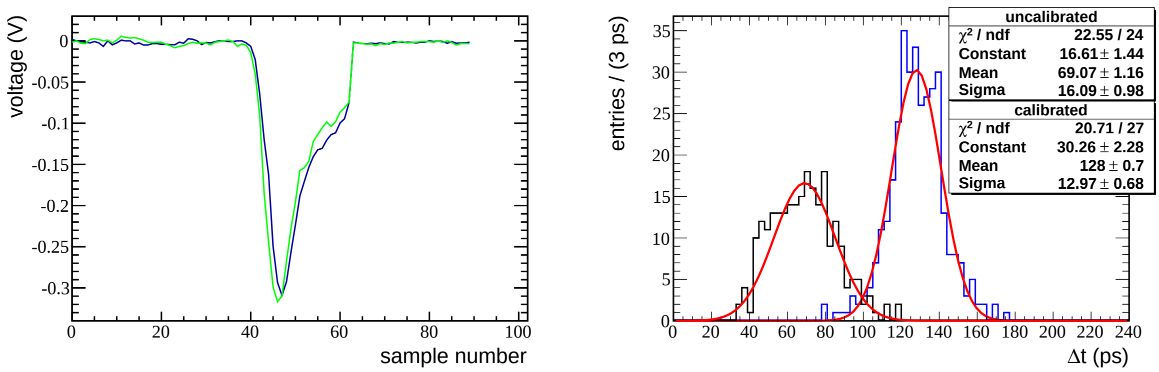

Fig. 7. (Left) Typical digitized MCP-PMT pulses with the PSEC-3 in channels 3 (blue) and 4 (green). (Right) Fitted time differences between the MCP pulses, based on a software constant fraction discriminator. The histograms correspond to the calculated time differences for uncalibrated (black) and calibrated (blue) data. Solid red lines indicate Gaussian fits used to determine the timing resolution in each case. The change in mean between uncalibrated and calibrated data indicates a significant deviation from the assumed nominal sampling rate.

5. Conclusion

We have introduced a method to calibrate timing delays between sample cells in a waveform digitizing system. The method has been successfully verified on data taken with a calibrated fast oscilloscope. Calibration of a waveform digitizing ASIC, the PSEC-3, is ongoing, with preliminary results indicating a 19% improvement in timing resolution after the calibration procedure is applied. The procedure has also proven quite useful in catching data artifacts through a simple visual inspection. Development of improvements to this technique is ongoing, with a major focus on incorporating non-idealities of the digitizer (e.g., mismatched gain) into the fitting procedure.

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