



Multipurpose Test Structures and Process Characterization using 0.13 μm CMOS: The CHAMP ASIC

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Abstract

The University of Hawaii (UH) in collaboration with the University of Chicago (UC) submitted a test Application Specific Integrated Circuit (ASIC), the Chicago-Hawaii ASIC MultiPurpose (CHAMP), composed of a number of discrete test elements in a 0.13 μm CMOS process. This paper describes the structures submitted by UH and UC. Hawaii designs include high speed flip-flops, voltage controlled ring oscillators and delay lines, an Low Voltage Differential Signal (LVDS) receiver, a set of four 64-cell waveform samplers with shared input, an analog storage and comparator structure, as well as a 12-bit Digital to Analog Converter (DAC). The Chicago designs include voltage controlled delay lines, delay locked loops, voltage controlled ring oscillators, transmission lines, and resistors. Each of the structures will be described, with simulation and test results presented.

Keywords: CMOS ASIC, integration, transmission line, DAC

1. Introduction

The Chicago-Hawaii ASIC MultiPurpose (CHAMP), is a joint ASIC submission between the University of Chicago and the University of Hawaii Manoa. The purpose for the ASIC was two-fold: the Chicago group wanted to submit test structures to test and validate their PSEC-3 design [1]; the Hawaii group submission was part of an ASIC design course taught by Dr. Varner to lay the groundwork for future ASIC submissions. Both building reusable components as well as training future designers. All of the designers, from both groups, were physics and engineering graduate students.

The CHAMP was undertaken as part of the Large Area Picosecond Photo-Detectors Project (LAPPD) [2]. The goal of LAPPD is to develop economical large-area photodetectors with excellent space and time resolution. A 1 picosecond timing resolution requires very high speed electronics and was a key motivator for using the IBM 0.13 μm CMOS process for manufacturing.

The process chosen for the design was the IBM CMOS 8RF-DM 0.13 μm fabricated through a CERN MultiProject Wafer run in May of 2010. The submission was a first using the IBM process for the University of Hawaii, while the University of Chicago had previously submitted designs and were in charge of final tape out and overall integration.

All of the structures were designed for this submission with an eye towards future reuse in designs and, as such, designed for ease of reuse and an ability to test each design. The components used in the CHAMP have been used in two further designs with little modification. A photo view of the CHAMP is seen in Figure 1.

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2. Test Structures and Results

The CHAMP ASIC is comprised of a number of independent test structures. A list of the structures and the relevant designer can be found in Table 1. Each of the Chicago structures was relevant for showing their simulation was accurate in order to create a final ASIC in their PSEC chip family. The test structures also were meant to further hone their design skills in the 0.13 μm process.

The Hawaii structures were each independently selected by the designer responsible. Most designers chose structures with an eye towards the future: most structures have been implemented in ASICs which have been submitted or are returned from the foundry. For most Hawaii designers, the submission was a first using ASIC tools, and as such, relatively straightforward designs were chosen.

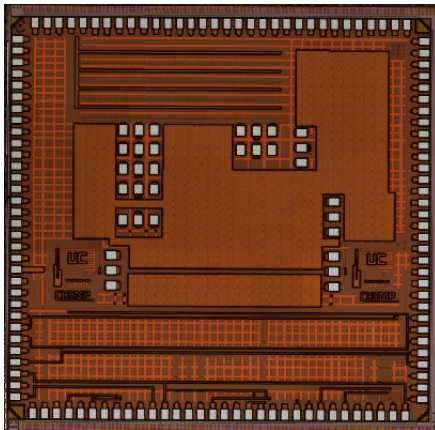


Figure 1: Photo view of the CHAMP ASIC. The ASIC is 4mm by 4mm. The Waveform sampler is the long, center top structure. The VCDLs are primarily located in the bottom of the design (under the logos).

Table 1: Structures on the CHAMP ASIC and the corresponding designer. More than 16 structures were designed by 7 individuals.

Design Name	University	Designer
VCDLs w. delay locked loops (DLLs) [18GHz and 25GHz]	Chicago	Eric Oberla
VCRO's with counters [3GHz and 4GHz]	Chicago	Eric Oberla
Independent DLL	Chicago	Hervé Grabas
Digital to Analog Converter	Hawaii	Larry Ruckman
Analog Storage Cells with built in comparator	Hawaii	Larry Ruckman
VCDLs (x2)	Hawaii	Matt Andrew
VCRO	Hawaii	Matt Andrew
Waveform Sampler Array (x4)	Hawaii	Kurtis Nishimura
LVDS Receiver	Hawaii	Michael Cooney
D Flip Flops	Hawaii	Matt Andrew

2.1. Voltage Controlled Delay Lines

Inverter chain delay lines are an important component in waveform sampling ASICs. The CHAMP included four VCDLs, two designed in Chicago and two designed in Hawaii. The Chicago designs were initially designed to operate at 18 GSa/s and 25 GSa/s using transistors with different threshold voltages. The normal threshold transistors were targeting an 18 GSa/s operation and the low voltage transistors were targeting operation at 25 GSa/s. Figure 2 shows the post simulation results between the two included designs as well as a similar VCDL in another ASIC, the PSEC3. The large range of potential operation, from 10 GSa/s to 29 GSa/s, across a wide range of bias voltages, allows great flexibility in future designs.

Figure 3 compares simulations using an earlier version of the post-layout tools and the same simulation using a more recent set of tools indicating additional parasitics. The more recent simulation tools much more accurately reflects the fabricated design. The improved simulations show a maturing design skill-set and has directly contributed to subsequent successful ASIC submissions.

2.2. Digital to Analog Converter

The DAC was designed using a classical R-2R design, with a serial interface for loading values, to save external pins on pin limited packages. The layout of the DAC can be seen in Figure 4. A resolution of 12 bits was selected to give adequate selection of output voltages. A key design metric was to have no gaps in the output voltage coverage, rather than focusing on perfect non-linearity. The non-linearity can be calibrated and corrected for as long as all analog output voltages are covered.

The plotted residuals from the actual and ideal results are plotted in Figure 5. The basic DAC elements, with changes as required, have been used in two subsequent designs. A further exploration and comparison of the DAC can be seen in the paper submitted for these proceedings [3].

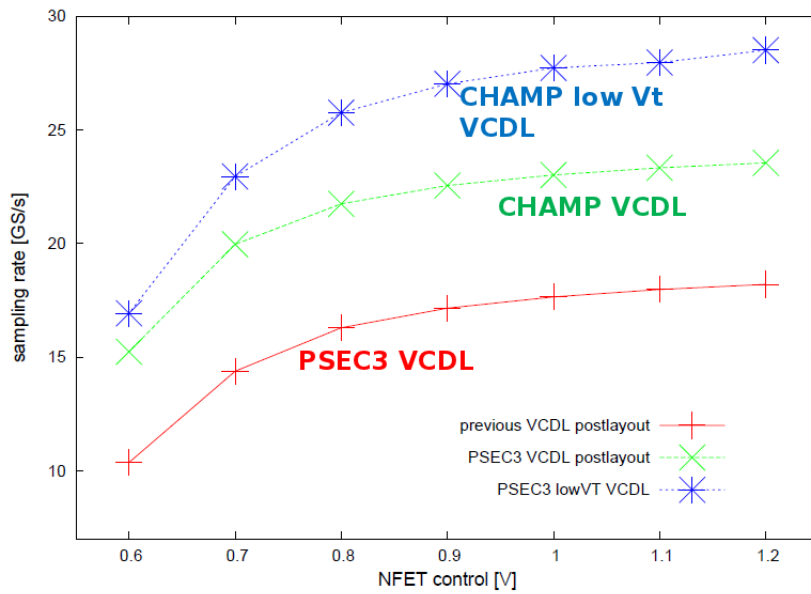


Figure 2: The CHAMP VCDL low voltage (fast, top curve) and normal voltage (slow, middle curve) sampling rate compared to the PSEC3 VCDL (bottom curve) as a function of the control voltage. The low voltage (low Vt) transistors give between 10% and 30% speed improvement with no further design changes.

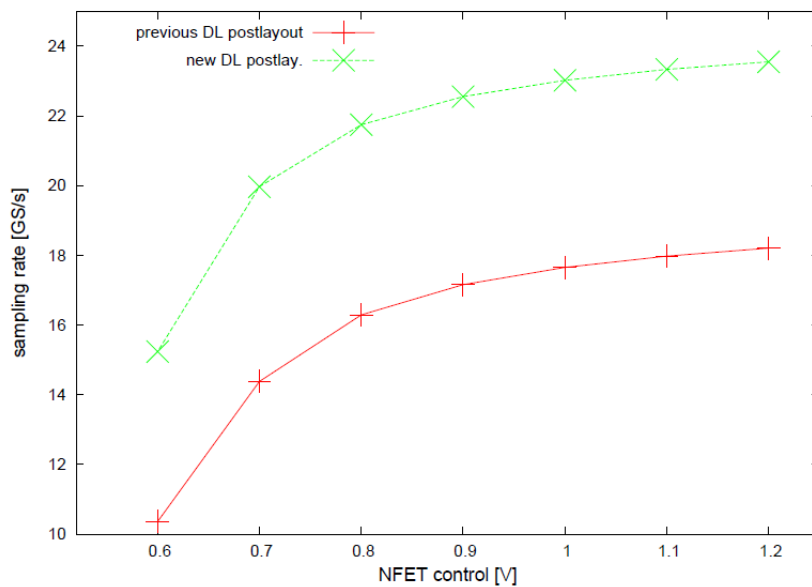


Figure 3: The CHAMP normal transistor VCDL post-simulation results comparing old simulation technique (top curve) with more accurate technique (bottom curve). The more accurate simulation technique is within a few percent of the measured results for the VCDL presented.

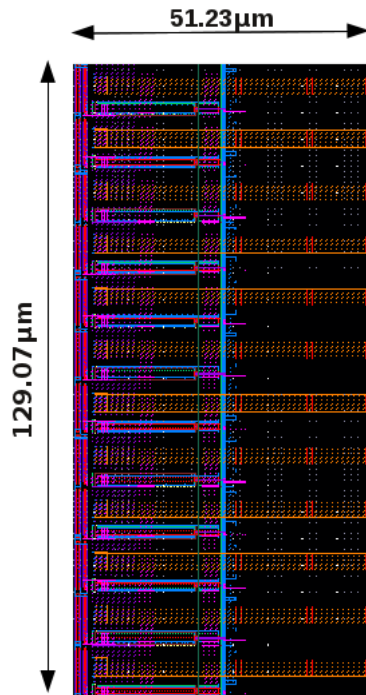


Figure 4: Layout view of the 12 bit DAC. The DAC dimensions are $129.07 \mu\text{m}$ by $51.23 \mu\text{m}$, using design kit resistors.

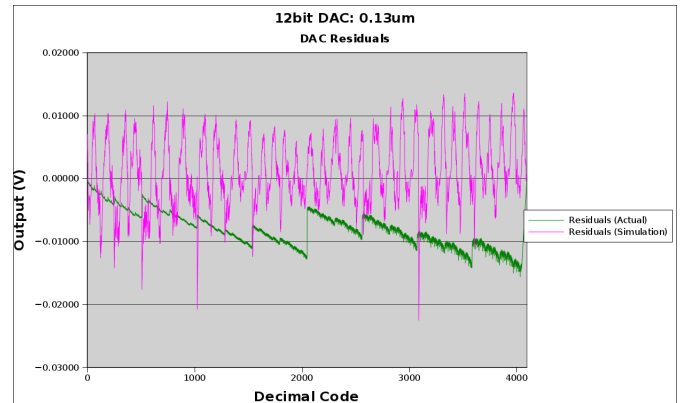


Figure 5: Plot for the 12 bit DAC showing residuals from the DAC output. The green line is the difference between the actual output from ideal output. The pink line is the difference between the simulated output and the ideal output.

2.3. Analog Storage Cells

An analog storage cell is a basic building block of a waveform sampling ASIC, with the Wilkinson Analog to Digital (ADC) a staple of designs from the University of Hawaii group. The Wilkinson ADC design is based on comparing the input voltage to the voltage produced by charging a capacitor. Once the input voltage is equal to or greater than the voltage on the capacitor, the comparator output will go high. The advantage of a deep sub-micron manufacturing process is the ability to densely pack the storage cells as well as provide a large number of cells. Small feature sizes however lead to large leakage currents requiring very fast operation and sampling.

The analog cells and comparator in the CHAMP are designed to minimize the effects of large leakage currents inherent to the $0.13 \mu\text{m}$ process. Each of the 16 total storage cells possess a 1 pF storage capacitor, using a Metal Insulated Metal (MIM) capacitor. The basic schematic is shown in Figure 6, with the capacitor and comparator highlighted. Each cell is $138 \mu\text{m}$ by $135 \mu\text{m}$ which includes address decoding logic, required for a tiled array. Such a design is suited for deep storage in a future waveform ASIC.

We have analyzed the cell to cell variation in the storage array. The cell to cell variation showed cell timing variations of up to $0.5 \mu\text{s}$, while overall, each cell exhibited similar output behavior in relation to the input voltage. Plotted in Figure 7 are the residuals from ideal when each output cell is enabled.

The noise of each cell was measured at 1.0 mV . The cell to cell variation of the noise was measured at $\pm 0.1 \text{ mV}$. This corresponds to a jitter on the cell's output of 5.23 ns .

2.4. Voltage Controlled Delay Lines

Additional VCDLs were included as designed by Hawaii. Two delay lines were included, with normal voltage threshold transistors and a low voltage threshold transistor version. Both were 64 stages long with a 9 stage delay. An 11 stage voltage controlled ring oscillator, with 9 stages of delay, was also included. NAND gates were chosen for the logic to minimize the capacitive loading of the inverter stages thereby increasing the speed and settling time

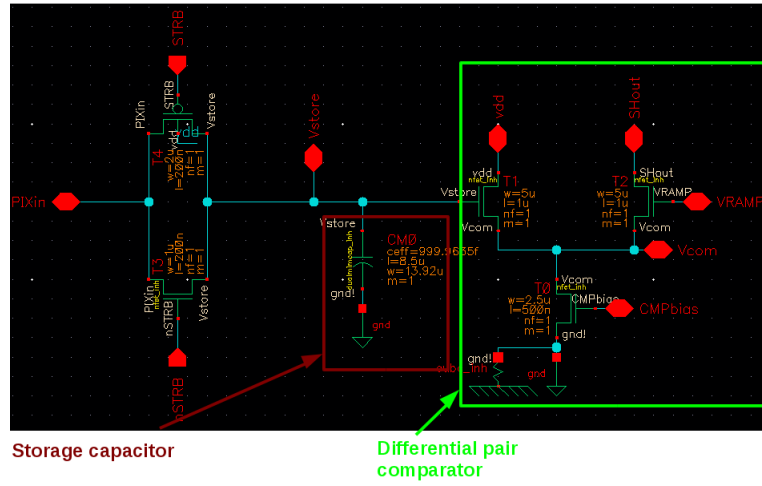


Figure 6: Schematic view of the analog storage cell with built in comparator. Each cell also contains a 1 pF capacitor.

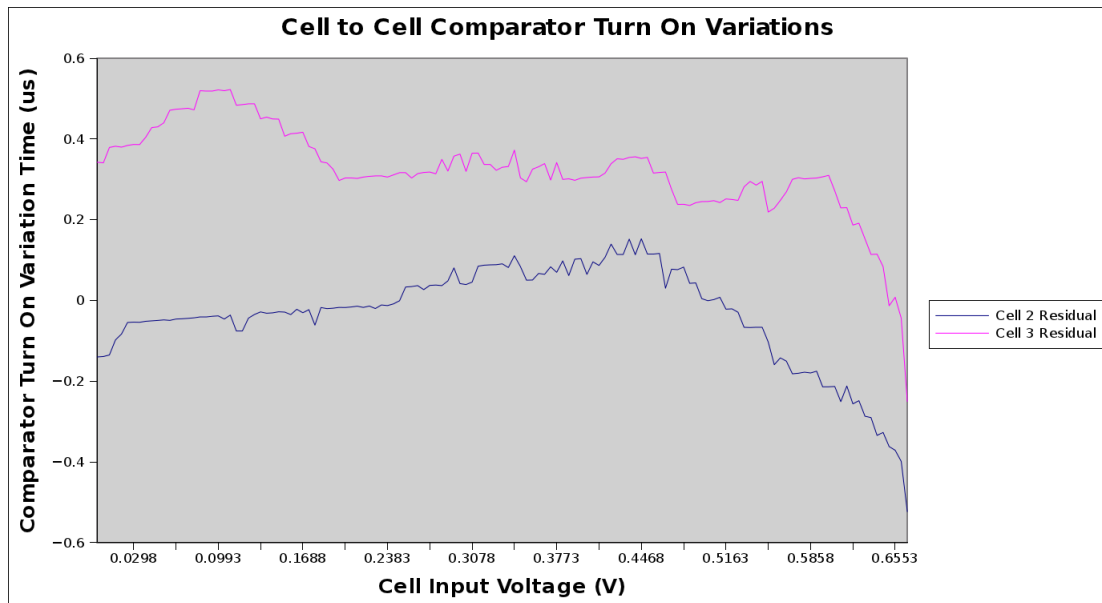


Figure 7: Time difference from ideal when each cell output should become enabled. Cell 2 and 3 are in the same column, vertically adjacent.

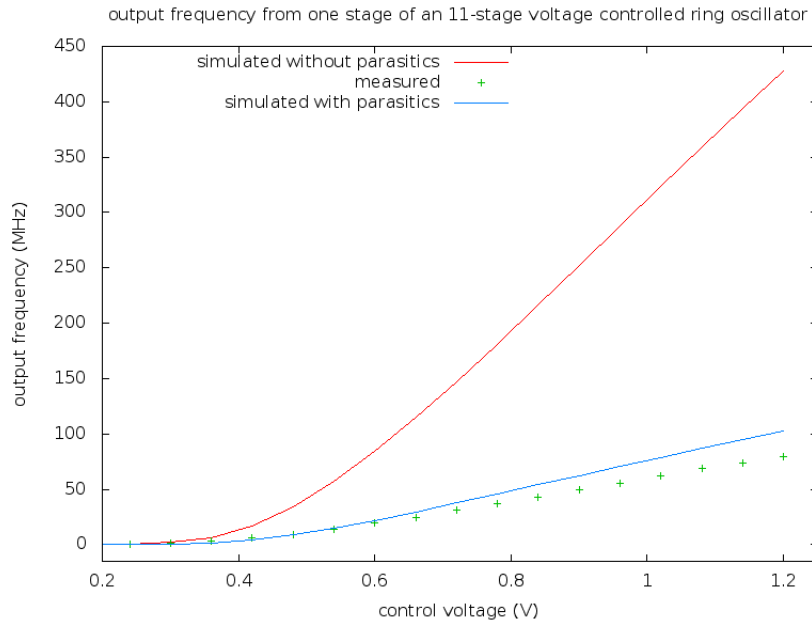


Figure 8: Simulation results plotted with measured results for the output frequency of the ring oscillator. The simulation with parasitics (solid red curve) shows a much higher output frequency compared to the simulation with parasitics (solid blue curve) and the measured results (green crosses). The simulated results with parasitics are within a few percent of the measured results.

of the device. A standard CMOS NAND gate only has 4 transistors, which allows for increased logic density and minimizing power usage.

Figure 8 shows the simulated and measured results from the ring oscillator. Of important note in this plot are the two simulation results: one without parasitics and one with parasitics. Parasitics are resistances, capacitances, and inductances introduced into a design due to wiring physical layout. Without parasitics, the oscillator operates almost 5 times faster than measured. The simulation with parasitics matches better than the non-parasitic version. Comparing the pure simulation results (without parasitics) to the measured results (and also to simulation with parasitics) helps in tracking down design and timing issues.

2.5. Waveform Sampling Array

CHAMP includes a set of four waveform sampling (WFS) arrays as part of a study on analog bandwidth for future waveform sampling and digitizing ASICs. Each array consists of 64 cells and a timing generator. A single cell, shown in Figure 9, accepts analog waveform input through a differential sampling switch. When the switch is closed, the voltage across a sampling capacitor tracks the input. This capacitor is chosen in the range of 20-40 fF to retain high input bandwidth. When the sampling switch opens, the voltage is held on the capacitor. This voltage is transferred to a larger, 200 fF, storage capacitor, via transfer switches connected to the terminals of an operational transimpedance amplifier (OTA). The larger storage capacitance mitigates leakage effects between sampling and readout. Readout is performed by an analog output buffer that drives the stored voltage to an analog switch, and ultimately, to an output pad.

The signals controlling the logic for the sampling switches are derived from a timing generator consisting of a VCDL implemented in low voltage-threshold transistors, and associated logic gates that generate the sample and hold logic for each array's differential input switches. The timing generator design is identical for each WFS, and allows operation at up to 1.2 GSa/s.

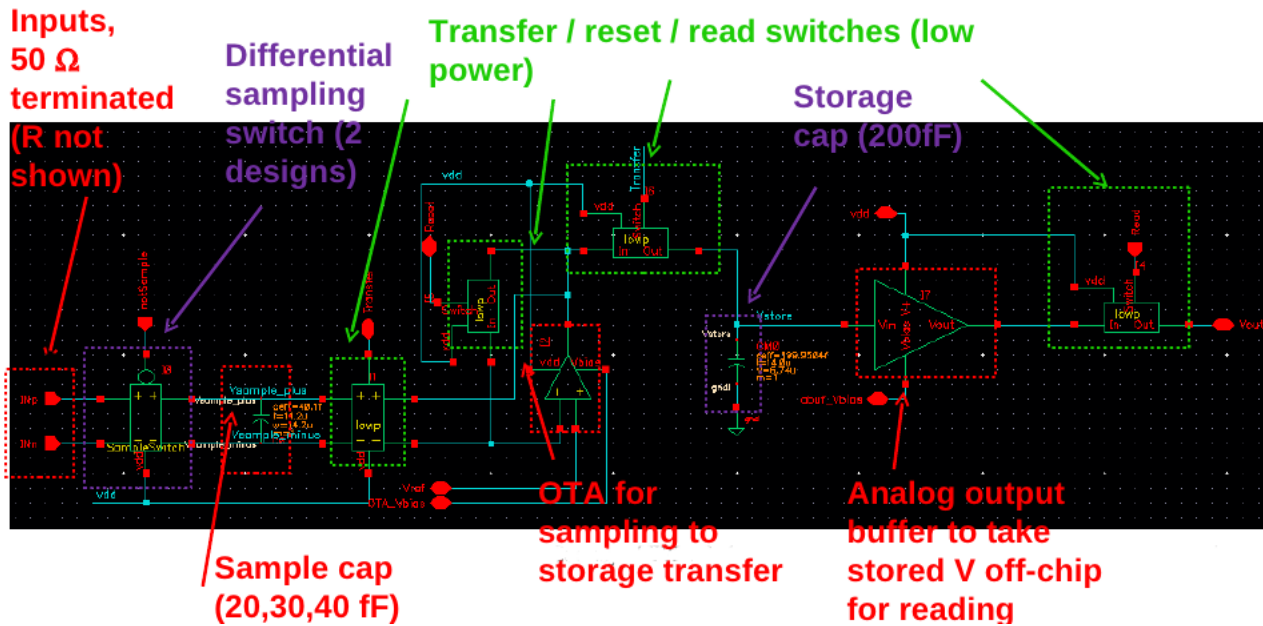


Figure 9: Waveform Sampling Array schematic of a single sampling cell. Four different types of sampling cells, differing by the capacitor size, is present on the chip.

The four WFS arrays share a common differential analog input, which is $50\ \Omega$ terminated on-chip near the analog input pads. A set of digital enable signals allows the user to choose which WFS is active at any time. The user is also responsible for controlling the logic to perform the sampling-to-storage transfer. Outputs from the switches connected to each cell's analog output buffer are wired to a common output pad. The cell for analog output is chosen by a shift register that passes a readout "token" from one cell to the next. The effective analog output then appears as a time-stretched version of the original input sample, as shown in Figure 10. The amplitude of this output signal relative to the input is used to measure the bandwidth of each array.

Three of four WFS arrays utilize the same differential input switch design and varying values of sampling capacitor (40 fF, 30 fF, 20 fF). The last array utilizes a 20 fF sampling capacitor and a different switch design. The array with the standard switch design and 20 fF sampling capacitance was found to be the best behaved, and shows an f_{3dB} of approximately 800 MHz, as shown in Figure 11. This result is not attributed to any process limits. Rather, a recent post-layout analysis indicates significant bandwidth degradation to the on-chip termination and the geometry of the coplanar waveguide connecting the analog inputs to each WFS.

2.6. LVDS Receiver

An LVDS receiver was included in the design. A standard textbook design was implemented and is undergoing further testing.

2.7. Flip Flops

Various flip flops were included in the design to gain experience with simple, yet highly important components. The flip flops were found to be functional but have not been tested for high-speed performance.

3. Readout Hardware

A dedicated readout circuit board, CHAMP_Eval, was fabricated for testing as seen in Figure ???. The CHAMP_Eval had DACs and buffer amplifiers to test the analog components on CHAMP. A single channel of slow ADC was on-board. Various SMA connectors and test points were provided. Each test structure on the CHAMP was independently



Figure 10: Analog voltage output with 100 MHz sine wave input. The input and output are analog voltages, so each step is quantized in time, hence the apparent steps.

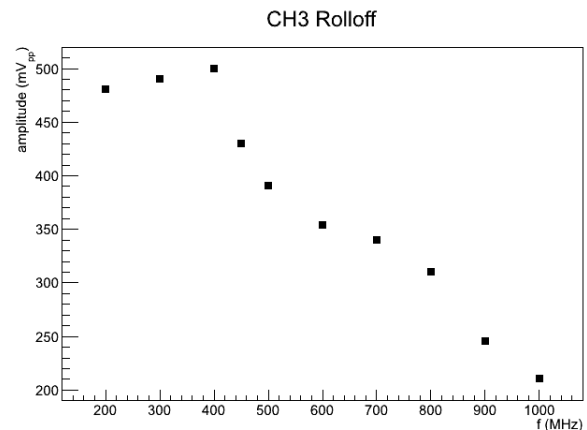


Figure 11: Measured roll-off response of channel 3 of the sampling array.

powered and power distribution was handled on the CHAMP_Eval. Digital control and readout was provided by an FPGA and USB microcontroller. The WFS, VCDLs, and VCROs were tested primarily with a signal generator and an oscilloscope via the SMA connectors and test points. The CHAMP_Eval DACs were also used to test the WFS, VCDLs, and VCROs was controlled via USB by a Linux machine running a simple command-line tool. The data was analyzed using ROOT and spreadsheet packages.

4. Conclusion

The VCDLs operated successfully between 15 Gsa/S and 28 Gsa/S, inline with what the simulations predicted. The improved simulation technique closely matches the measured results. The VCDL measurements are a useful check for their PSEC-4 ASIC which is currently being fabricated on the same process. The DAC was shown to have no gaps in output voltage from 0 V to 1.2 V. The DAC design has been used in a subsequent ASIC using a different fabrication process.

The analog storage cells showed the viability of a Wilkinson type ADC in this process, with a noise of 1.0 mV with jitter of 5.23 ns. Having shown the possibility of using the 0.13 μ m process to design a waveform sampler, a dedicated ASIC with waveform sampling using the 0.13 μ m process from the Hawaii group has been fabricated.

Two subsequent ASICs have been submitted using the knowledge and experience gained during the CHAMP submission process. Future designs using components from the CHAMP are being planned.

5. Acknowledgements

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6. References

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