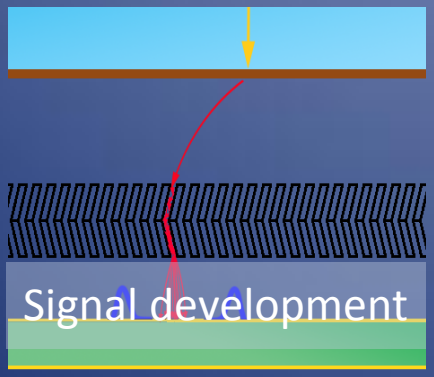
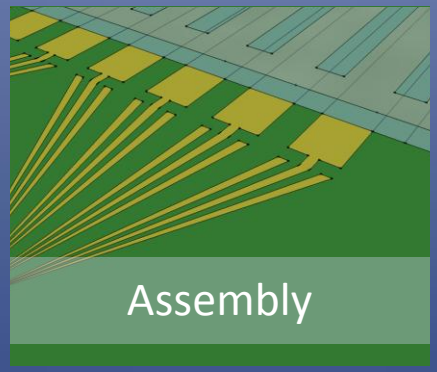
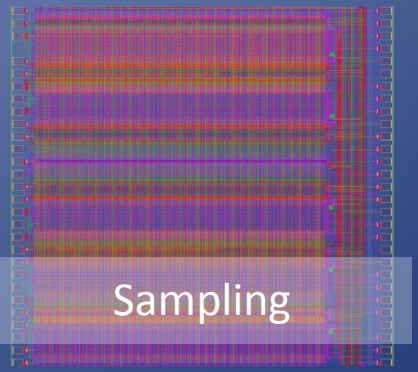
Development of a sampling ASIC for fast detector signals

Hervé Grabas
Work done in collaboration with Henry Frisch, Jean-François Genat, Eric Oberla, Gary Varner, Eric Delagnes, Dominique Breton.







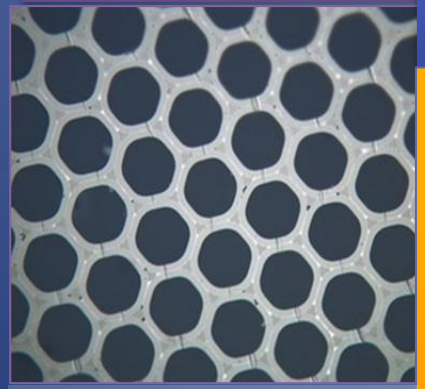
Outline

- LAPPD effort overview
- Presentation of the detector
- Simulation work
- Preliminary simulation results
- Sampling theory and chip development
- System overview
- Conclusion

LAPPD effort overview

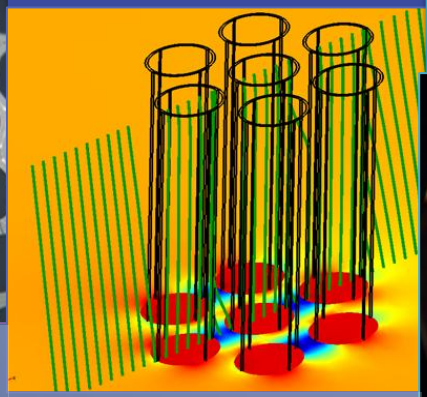
3 major axis

MCP & Photocathode



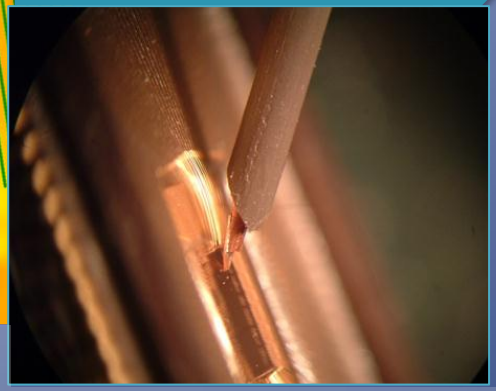
Use ALD for surface improvement

Simulation



Use simulation for design choice

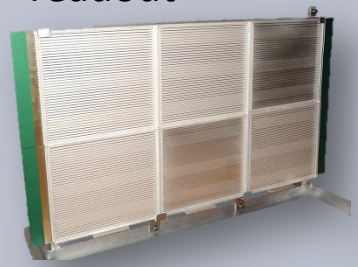
Readout



Use of fast transmission line & sampling

Large Area Photo-Detector

- High QE photocathode
- Controlled gain MCP
- Fast rising signal
- High speed readout



Detector presentation

Specification

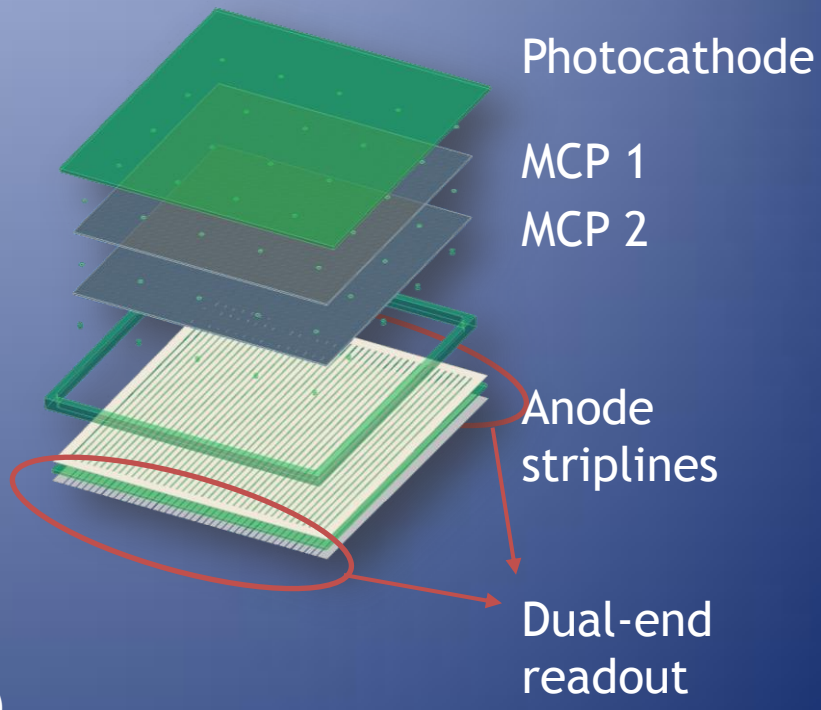
- Large area : 20×20cm²
- Cheap : less than 10$ incremental cost per in²
- Fast : ~1psec resolution at 100 PE
- Efficient : Study of high QE photocathode (>50%)

Parts

- Photocathode (2 options Ga-X or Multi-Alkali)
- MCP 1 & 2 (ALD coated)
- Anodes striplines (silkscreen)
- Glass enclosure (Borofloat 33)
- Readout electronics

Connectivity

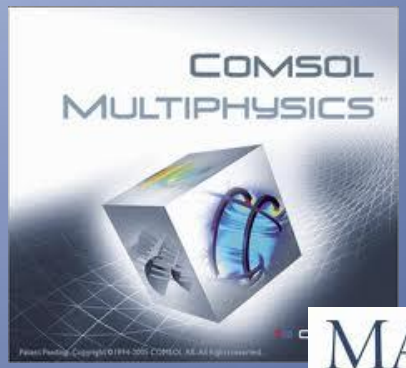
- No internal connections (HV via R divider network)
- No pins (stripline read-out)

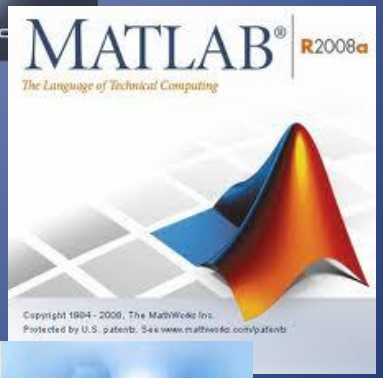


Goal : detector ready in 2 years from now.
Status end of year 1.

LAPPD: Simulation work

- As part of the understanding work done on the MCP-PMTs detector in the LAPPD we are looking at:
  - ✓ How is the signal created in the last MCP gap (between MCP and anodes).
  - ✓ How is the signal (E-field) is coupling into the micro-stripline.
  - ✓ How is the signal propagating along the striplines.
- Doing this allow several interesting development:
  - ✓ Validation of experimental results and understanding of the detector behavior.
  - ✓ Investigate and test new design to improve the detector efficiency





Electron signal from the MCPs

Signal characteristics

- Nb of output electrons: up to 10^10 per pore.
- Cloud size: 20µm (size of the MCP pore). The x-y cloud expansion is negligible in a small gap (1mm) :

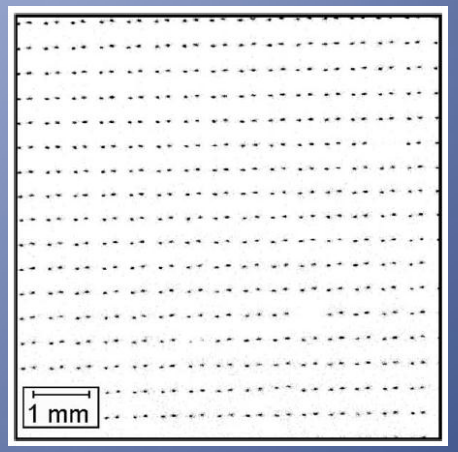
$$\frac{\text{electrons gap speed}}{\text{electron drift speed}} = 10^5.$$

Signal development

- Electron travelling in the gap induces signal on the stripline.
- The electron time of travel and speed determines the rise-time of the signal. Under simulation.

Signal limitation

- Time resolution : Cloud elongation in z-direction creates timing degradation. Under simulation.
- Spatial resolution : Pores create a shift in the direction of their bias angle for the electron clouds (~200µm @800V) .
- Noise : Photocathode thermal-emitted electrons (1PE equiv. noise).
- Saturation : each pore has a limited output current (depending on the MCP resistivity).



Superimposed pinhole mask for two voltage value in the last gap . O Siegmund (Berkeley)

Best to work at:

- Balanced number of PE
  - ✓ Insensibility to noise
  - ✓ Avoiding saturation
- High last-stage bias voltage
  - ✓ Fast rise time

Signal development theory

Signal creation

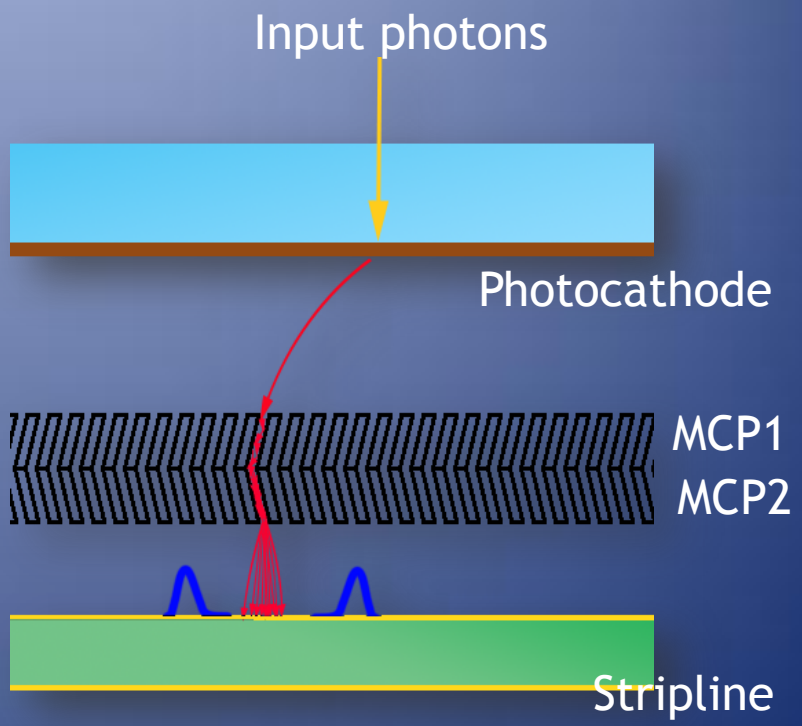
- The field radiated by the electrons as the are accelerated in the gap induces surface current on the top stripline that are the signal sources for stripline.
- The rise time is given by the traveling time of the electrons in the gap. Under simulation.
- The fall time is given by the ground return loop (to be verified). Under simulation.

Signal propagation

- After creation, signals propagate in a micro-stripline mode to both end of the detector.

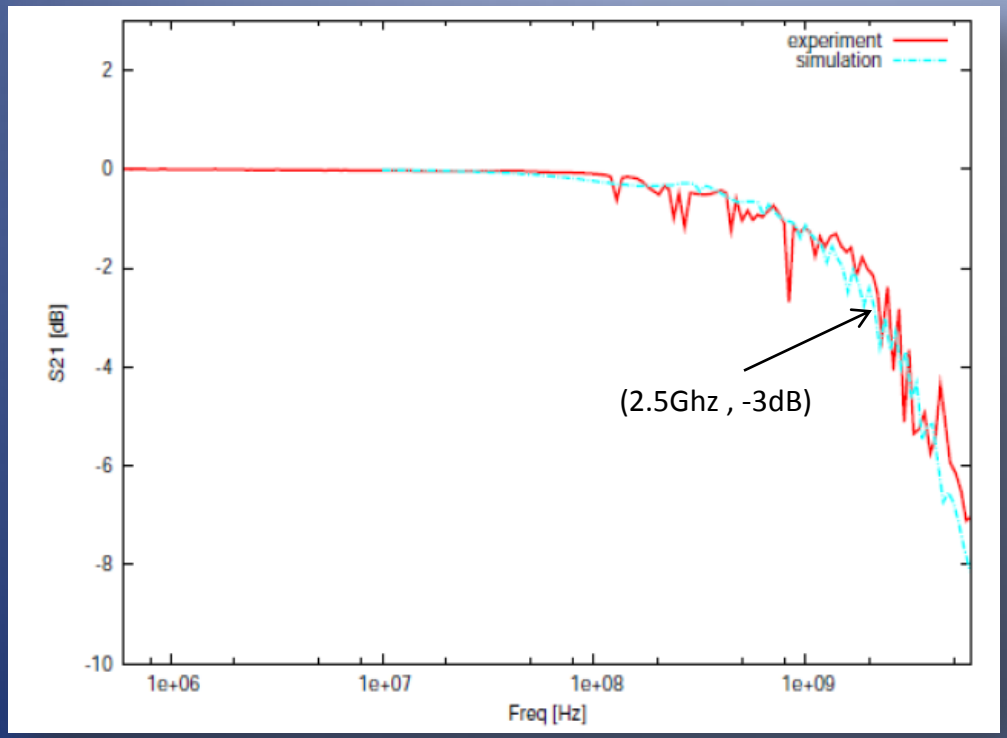
Signal limitation

- Bandwidth simulated and tested at 2.5GHz
- Field losses when coupling into microstrip lines.



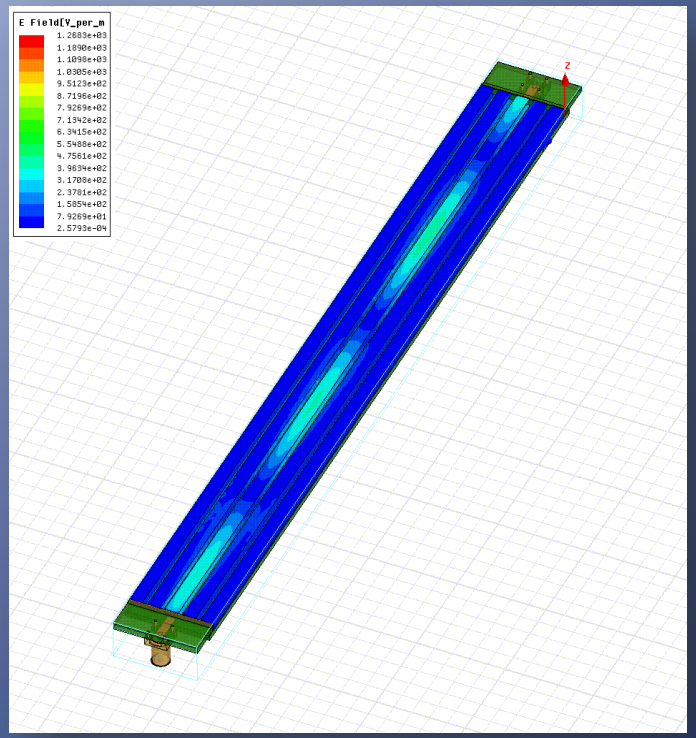
Signal development results

Propagation in the stripline



Micro-stripline array typical bandwidth:

- ✓ Measured (red)
- ✓ Simulated (blue)



Micro-stripline simulated in HFSS @ 1Ghz.

2.5Ghz = 140ps rise time

Detector simulation

Simulation of the signal generation and propagation in the stripline

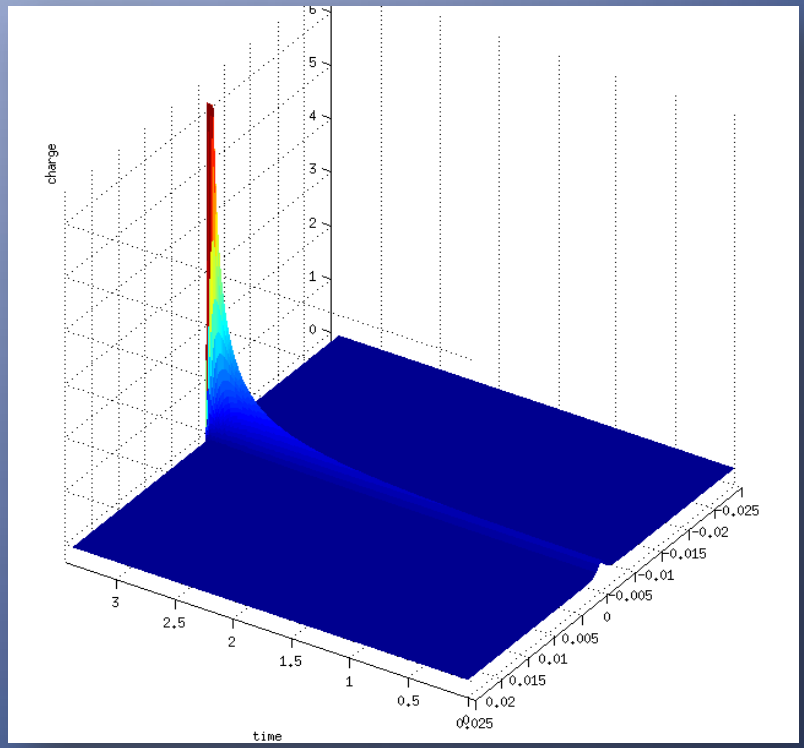
- ✓ In progress
- ✓ Challenging

Simulation difficulties

- ✓ Near field
- ✓ Particle in cell
- ✓ Time dependent

Objectives

- ✓ Validate experimental results
- ✓ Improve detector efficiency (by better coupling the electron energy in the striplines)

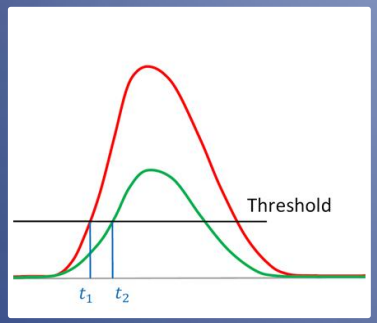


Surface charge induced on the strip as a function of time and position

Signal sampling – Theory

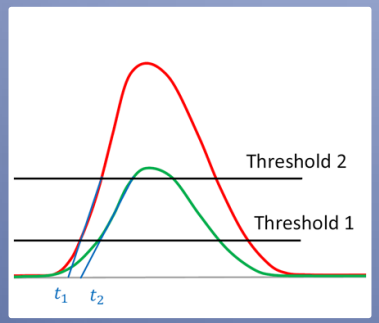
How to get to the picoseconde

Single threshold



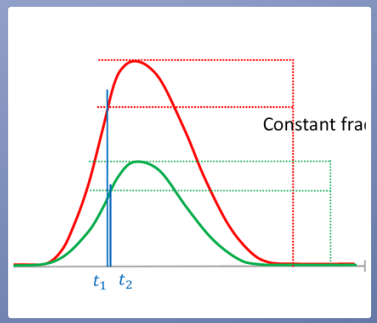
The single threshold is the least precise time extraction measurement. It has the advantage of simplicity.

Multiple threshold



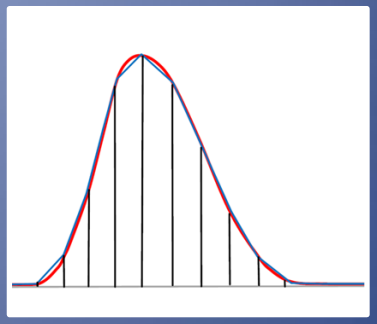
The multiple threshold method takes into account the finite slope of the signals. It is still very easy to implement.

Constant fraction



The constant fraction algorithm is very oftently used due to its relatively good results for and relative simplicity.

Waveform sampling



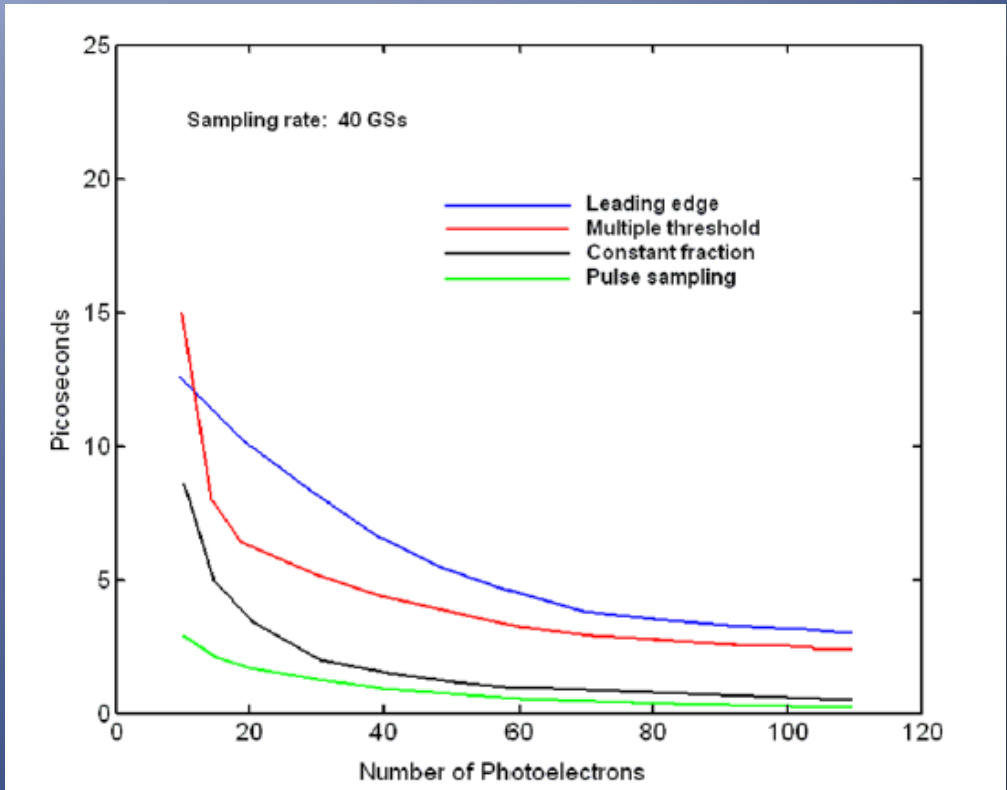
The waveform sampling above the Shannon frequency is the best algorithm since it is preserving the signal integrity.

We believe that sampling above the Shannon frequency and fully reconstruct the signal preserve at best the timing information.

Signal sampling – Theory

How to get to the picosecond

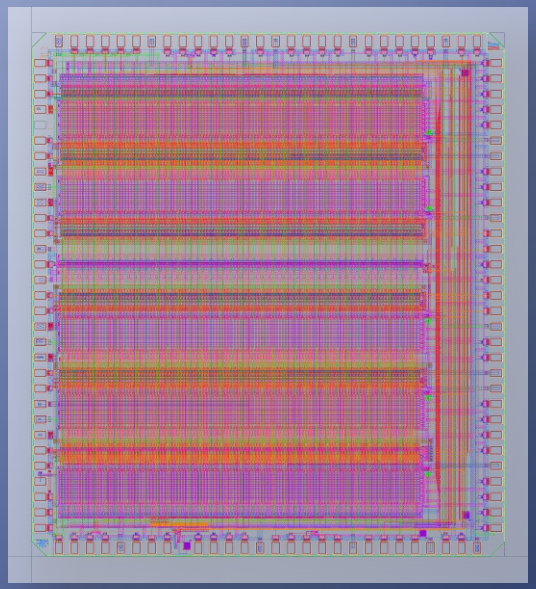
- The four models have been simulated with Matlab.
- For pulse sampling the time is extracted with template fitting using the LMS algorithm.
- The pulse sampling algorithm give the best results, more noticeably for small number of PE.
- The best readout chip for an MCP-PMT detector is therefore a sampling chip.
- The sampling frequency is taken to be 2× the fastest harmonic in the signal: 10Gs/s



From Jean-François Genat

LAPPD : Development of a 10Gs/s sampling chip

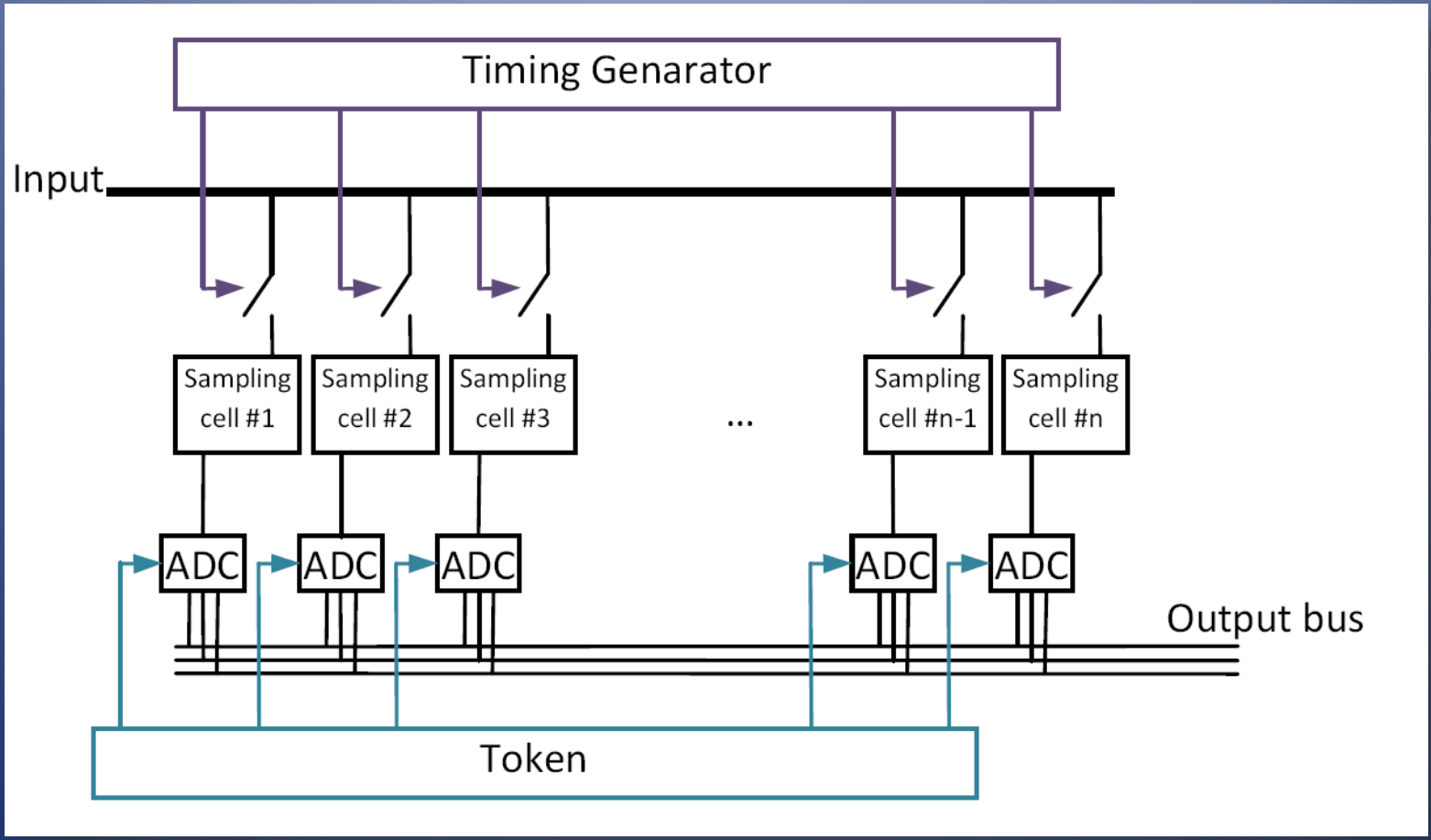
Chip characteristics	Value
Technology	IBM CMOS 0.13µm
Sampling frequency	>10Gs/s
Number of channel	4
Number of sampling cells	256
Input bandwidth	>2GHz
Dead time	2µs
Number of bits	8
Power consumption	To be mesured



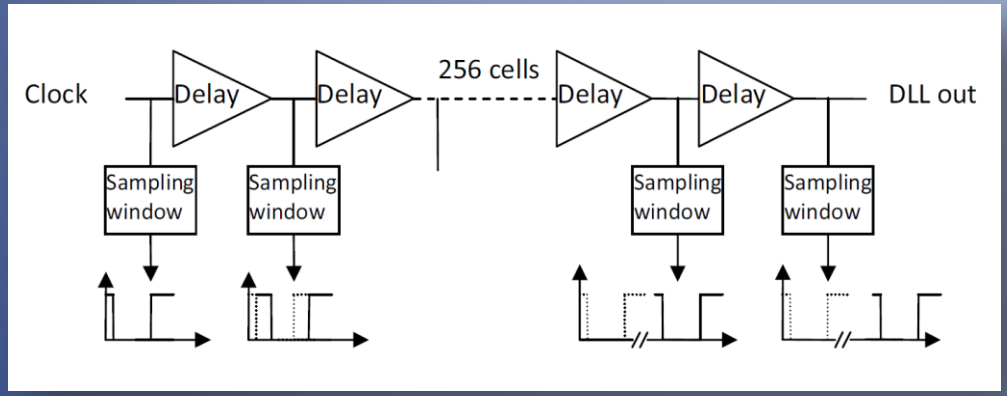
Psec3

No results to present yet.

Chip (basic) internal architecture

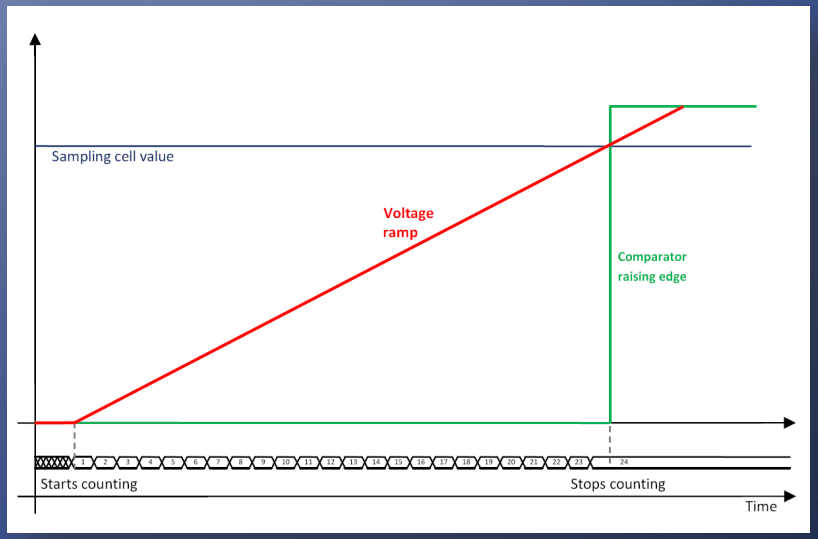


Timing generator



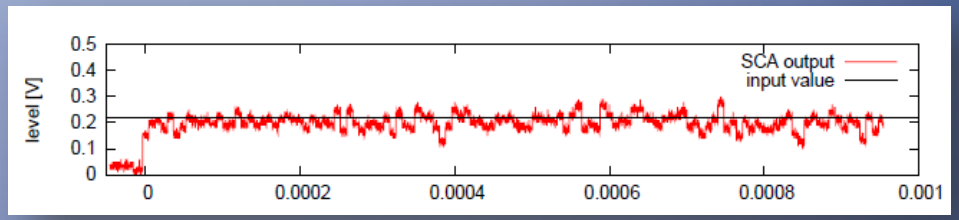
- **Generates a sampling frequency at= $\frac{1}{Delay}$**
  - ✓ The min delay is smaller for smaller process
  - ✓ Locking the DLL improves temp. dependency, jitter, …
  - ✓ Current sampling speed : 11Gs/s

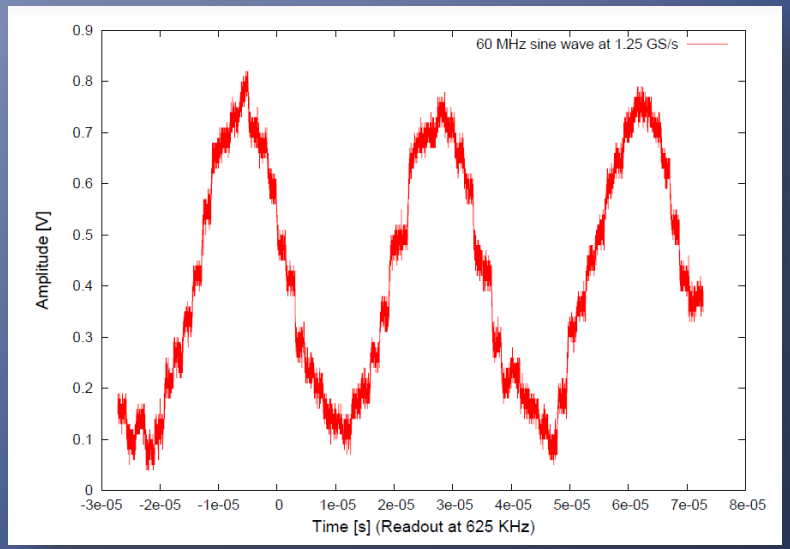
- **Digitization: count until the comparator reaches the threshold.**
  - ✓ Slow process (2µs)
  - ✓ Good linearity (given by the ramp)
  - ✓ Question: number of counter to use (so far: 1 counter per cell) ?



Chip evolution

- **Issues faced during development**
  - ✓ Lack of support from IBM (new kit).
  - ✓ Wrong ESD protections.
  - ✓ Leakages.
  - ✓ Digital part (flip-flop, counters).
- **Strengths of the design**
  - ✓ The relative simplicity.
  - ✓ Has already be fully proven working (Delagnes, Breton, Ritt, Varner).
  - ✓ Support from G. Varner, E. Delagnes and D. Breton
- **Future plans**
  - ✓ More testing in the upcoming month (boards and chips coming).



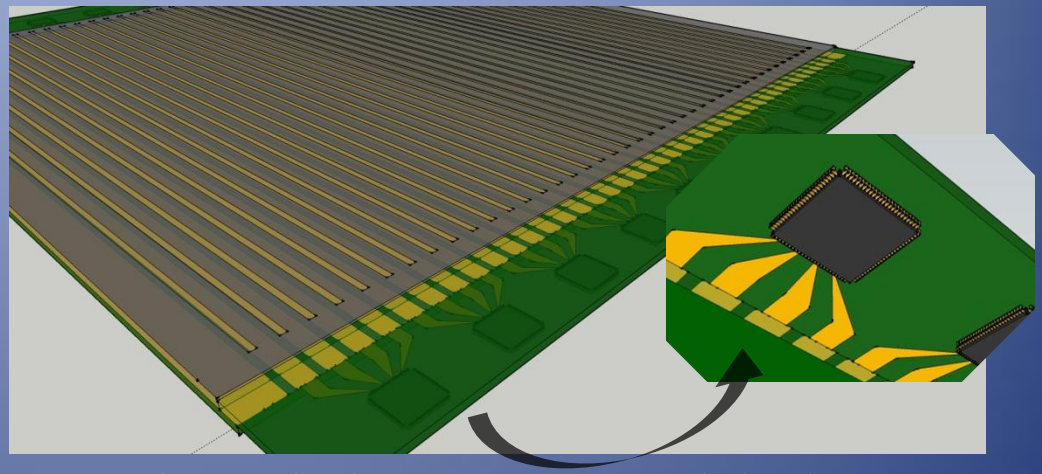


Analog outputs from Psec2 before correction showing cell-to-cell offset (and scope noise).

System integration

Electronics to detector

- **Electronics – Detector integration**
  - ✓ Simple design
  - ✓ Simple assembly
  - ✓ Being simulated now – tested soon



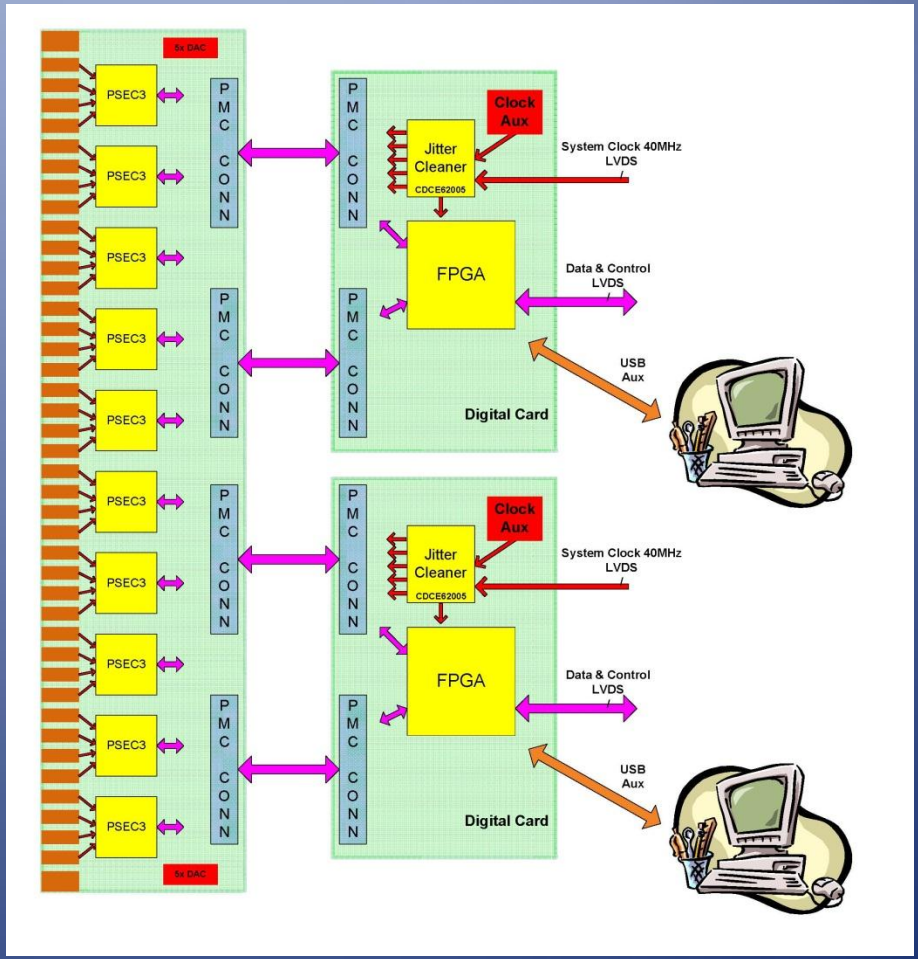
Picture showing the detector integration with the electronics.

Mock-up of the detector assembly

System integration

Electronics

- **Electronics master controller**
  - ✓ Under development (might not be final design)
  - ✓ 1 FPGA servicing 4 Psec chip
  - ✓ 1 clock distributed to every chip (less jitter)

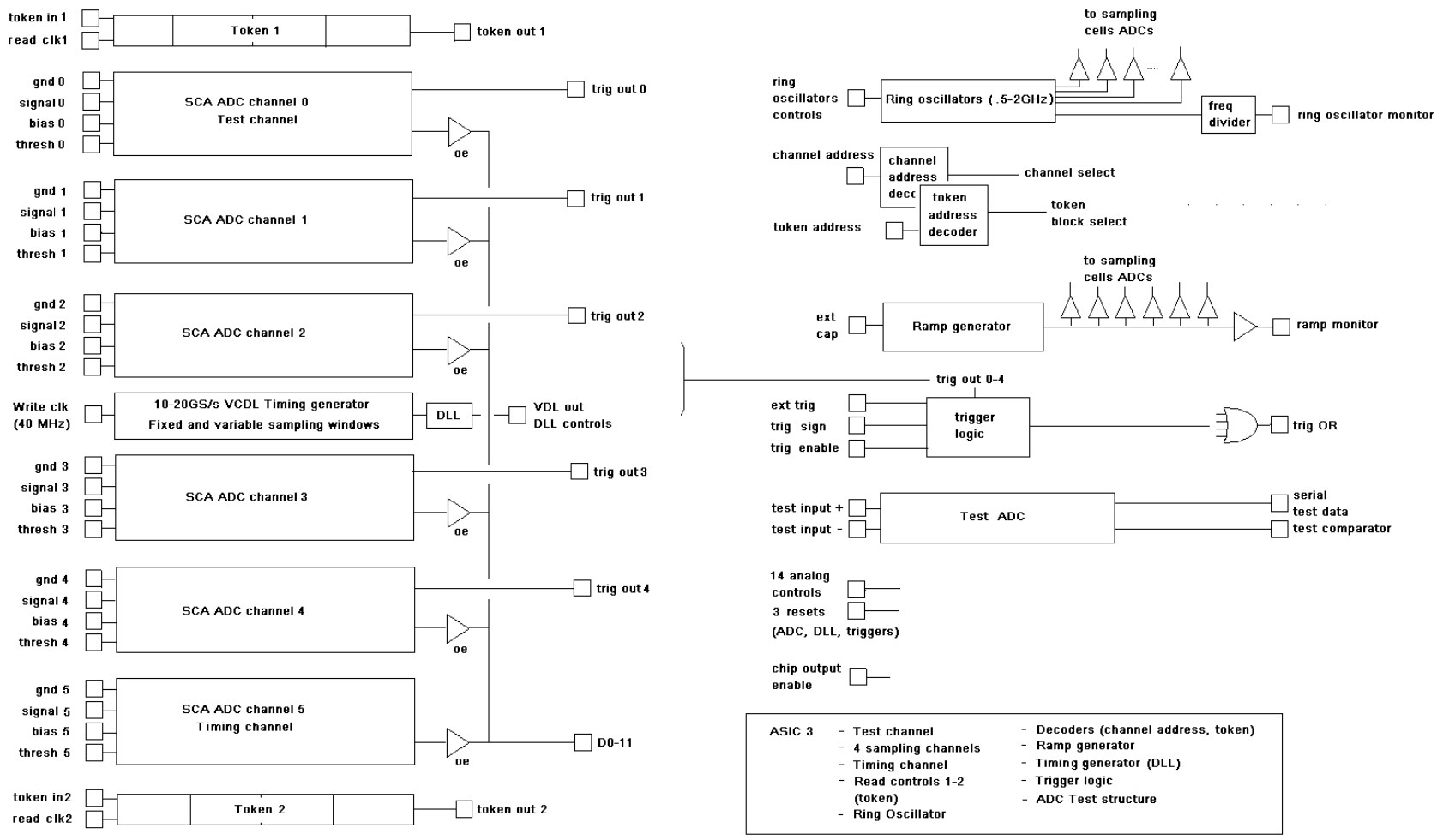


Conclusion

- Project in development
- Simulation work started few months ago
- Few result, but very exciting
- Electronics part manufacturing has been delayed. We except new result at the end of this year

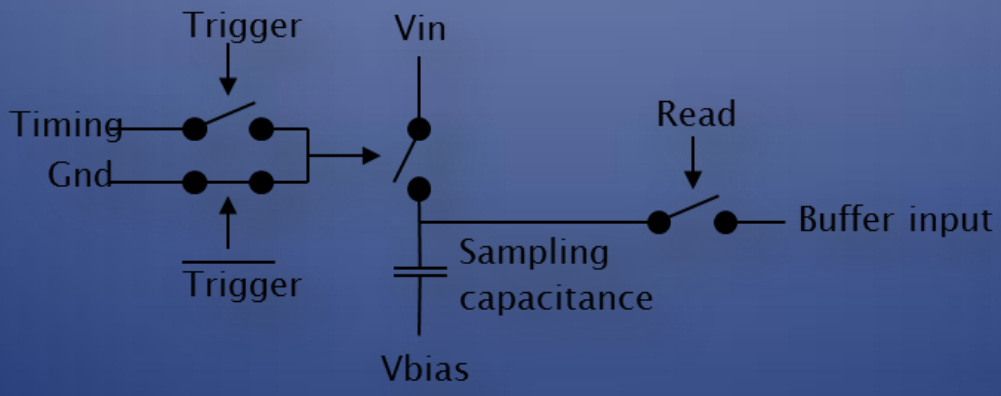
Backup

Psec3 Block view



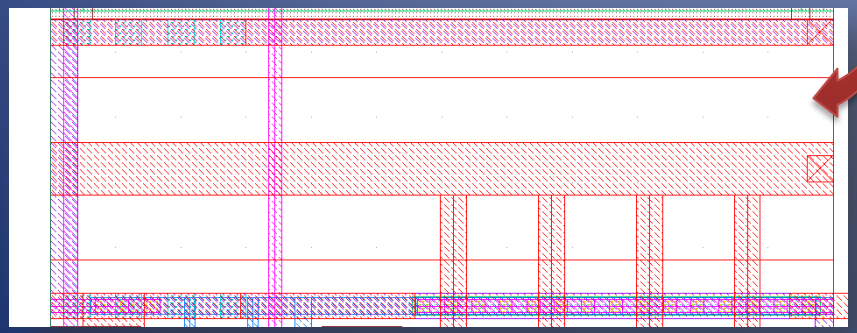
Sampling cell

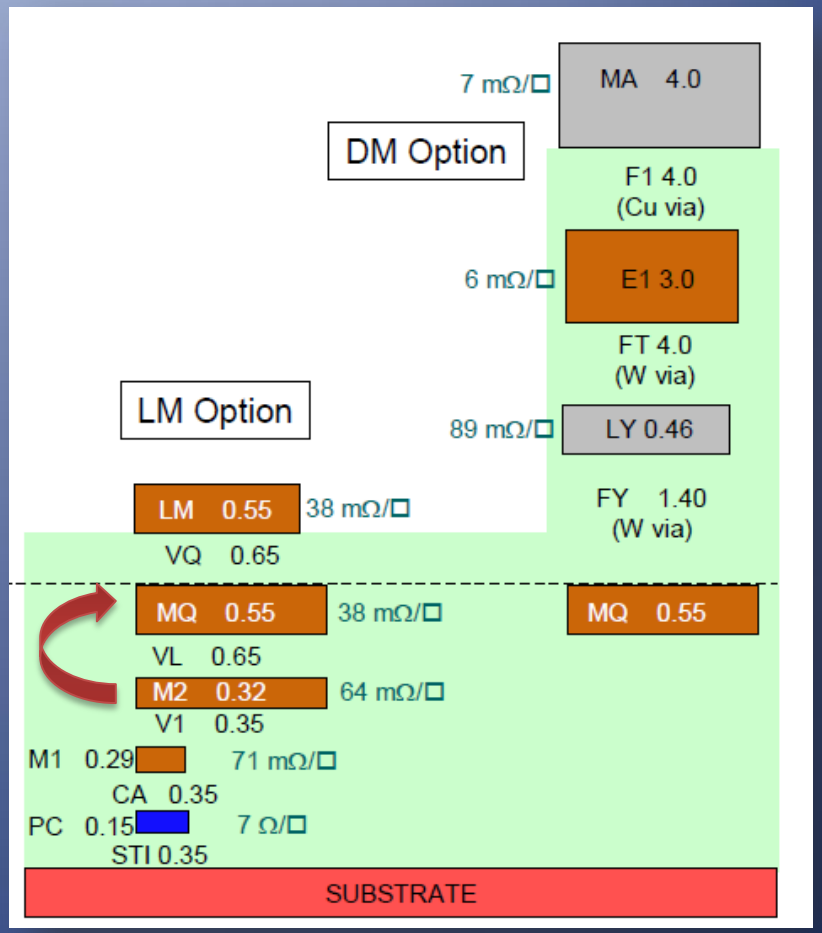
- An unit is basically made of one storage capacitance controlled by two signals :
  - Timing (800ps wide pulse).
  - Trigger (in case of an event).
- Timing stores the analog values in the sampling capacitance at a rate of 15Gs/s.
- Trigger open all the write switches in case of an event at the input.



Test channel sampling cell

- Went from M3 to MQ (gain a factor 2 in lin.res.).
- Add anti-fill layers, for layers from M1 to MG.
- Increase the width.

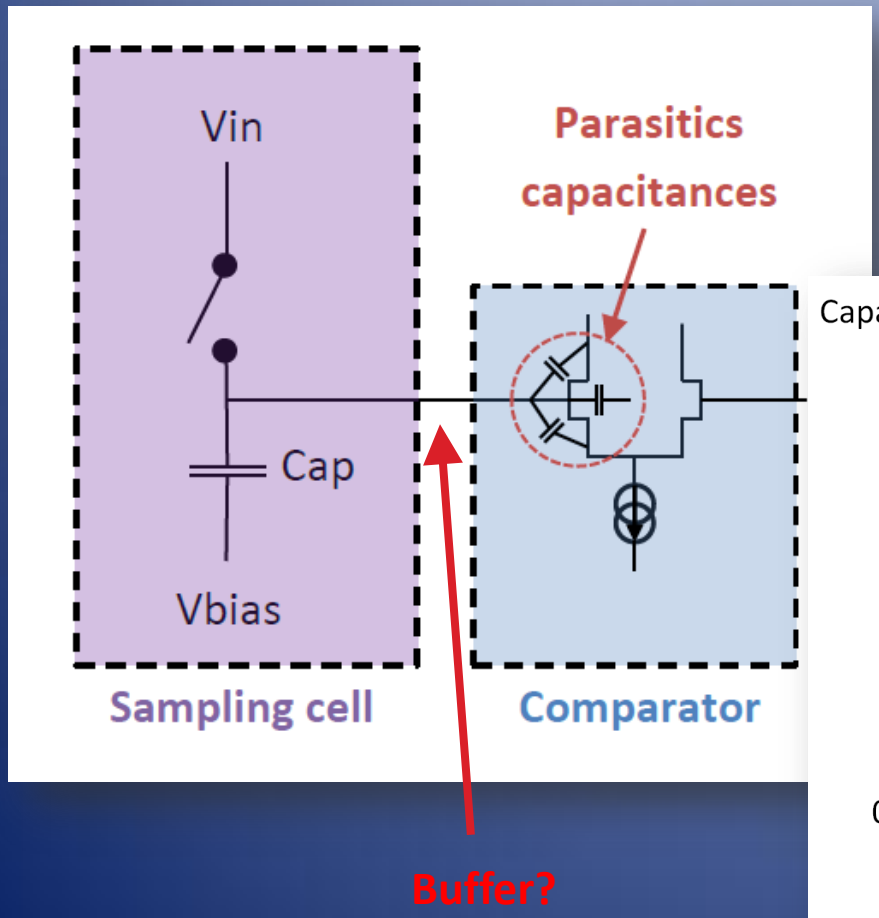




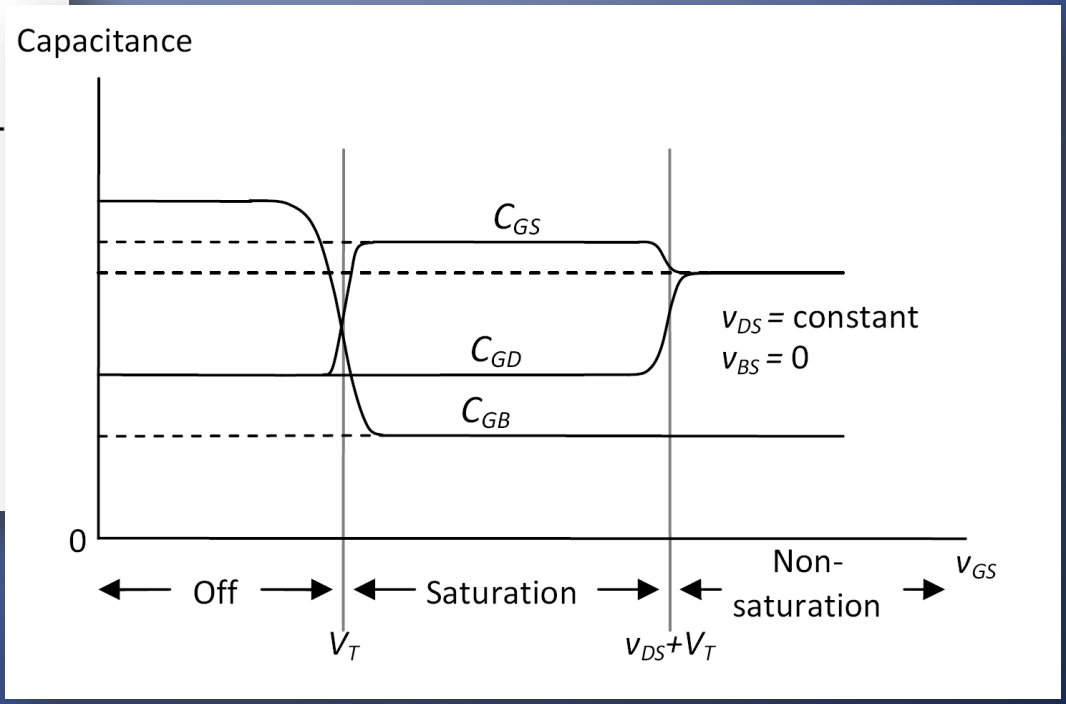
The 50Ω input resistance

	Advantages	Disadvantages
On the board	• Can be replaced • Possibility of a good transmission line until the terminaison.	• The pad capacitance ~3pF and input line cap ~1.5pF are in series with 50Ω. • Bwth <1GHz
After the pad	• Input signal won't see the pad input cap. • Bandwidth 1-2GHz.	• Non replaceable. • More impedance mismatch at the input of the chip.

Is fast buffer necessary?



- Comparator parasitics capacitance value: 3.5fF

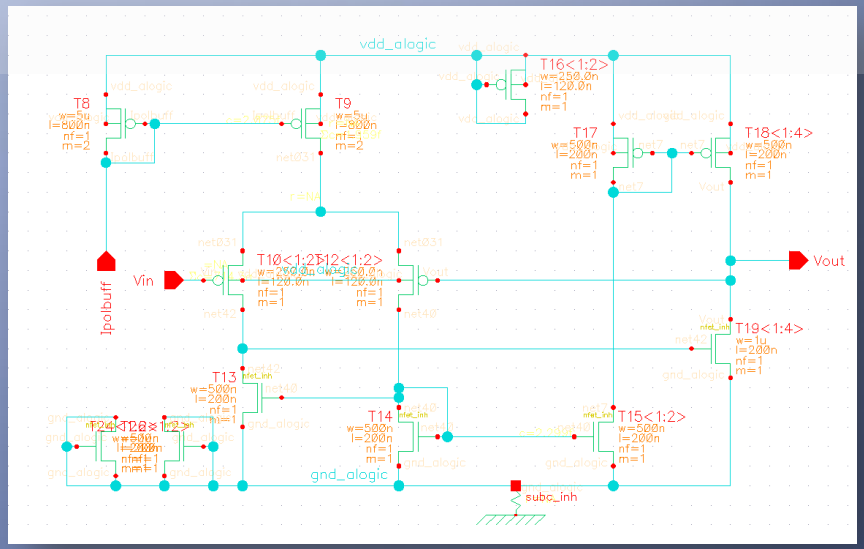


With and without buffer

	Without buffer	With buffer
Offset	Offset of the comparators	Offset of the comparators + buffers
Noise	Thermic noise of the 50Ω	Noise of the buffer added
Readout delay	None	Buffering delay
Input dynamic	Maximum	Buffer dynamic
Linearity	Degraded by the parasitic capacitance of the comparator	Linearity of the buffer.

To answer the question : buffer in 4 channels. No buffers in test channel.

The buffer



- Characteristics:
  - 14ns buffering time < 25ns of the write cycle.
  - 30µV of integrated noise from 1kHz to 10GHz.
  - Low power: 1uA/buffer.
  - Big offset variation due to process variation (100mV measured buffer to buffer).
  - 1V linear range.

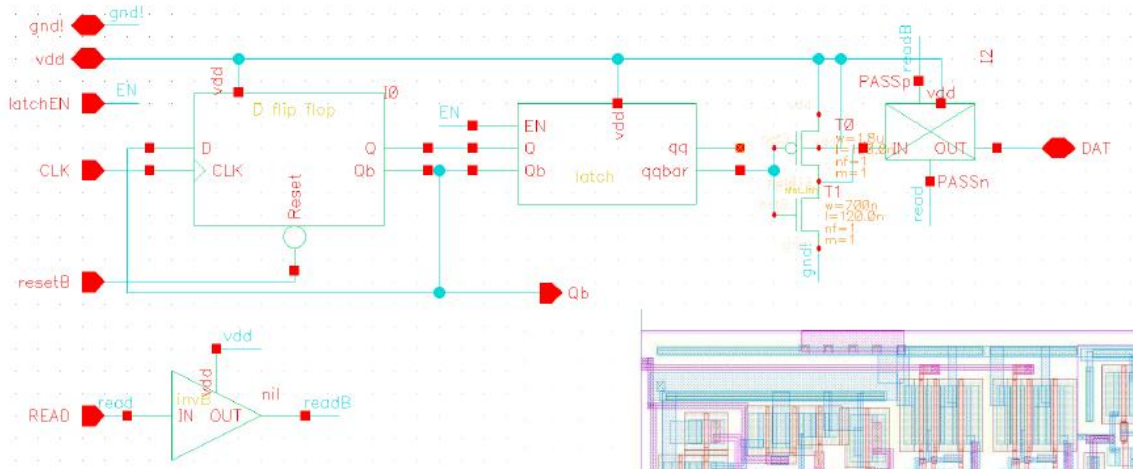
The ADC

Same architecture as before.

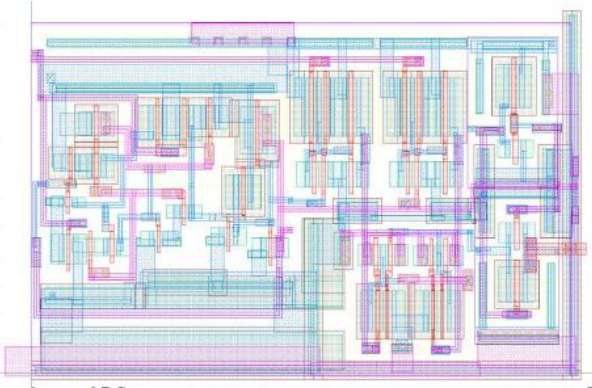
Latch inserted at the output stage to be leakage independant.

ADC

Up to 12 bit Wilkinson ADC with 2 stage structure of counter+storage (fast dff+latch)



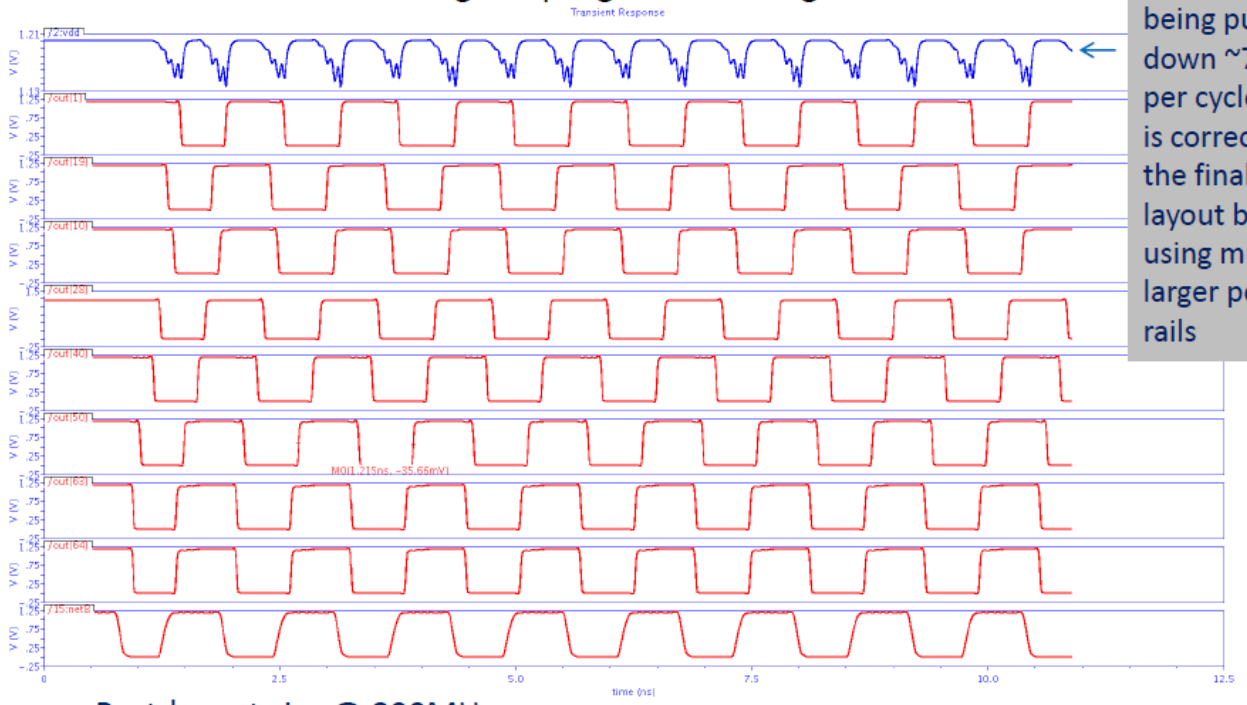
In the future, this 2-stage structure could be tweaked to allow concurrent readout and digitization (would drastically reduce dead-time).



The clock fan-out

Clock fan-out

- fully simulated post-layout. Successfully distributes RO clock to 256 cells up to about 1.8 GHz.
- drivers can be turned off during sampling to reduce digital noise

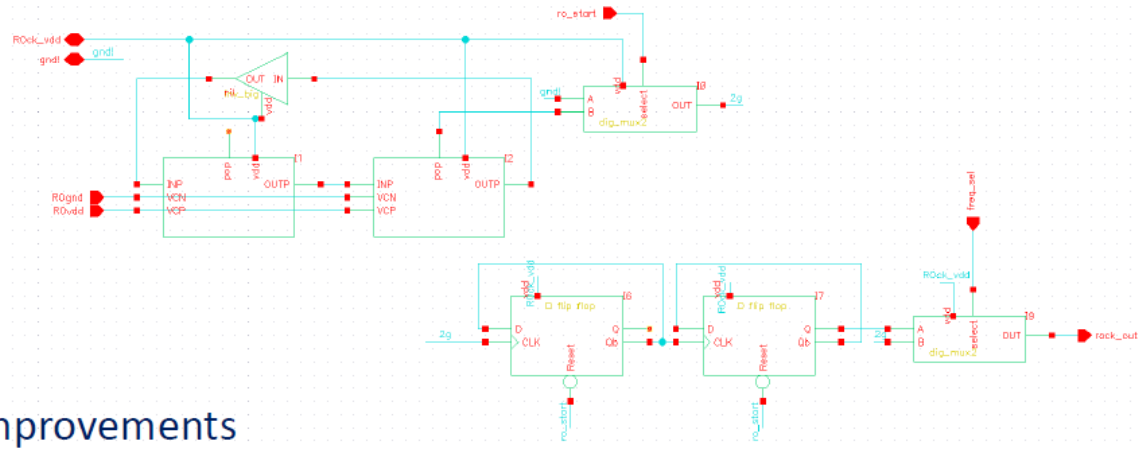


Post-layout sim @ 800MHz

Note: vdd is being pulled down ~70 mV per cycle. This is corrected in the final ADC layout by using much larger power rails

The ring oscillator

ring oscillator



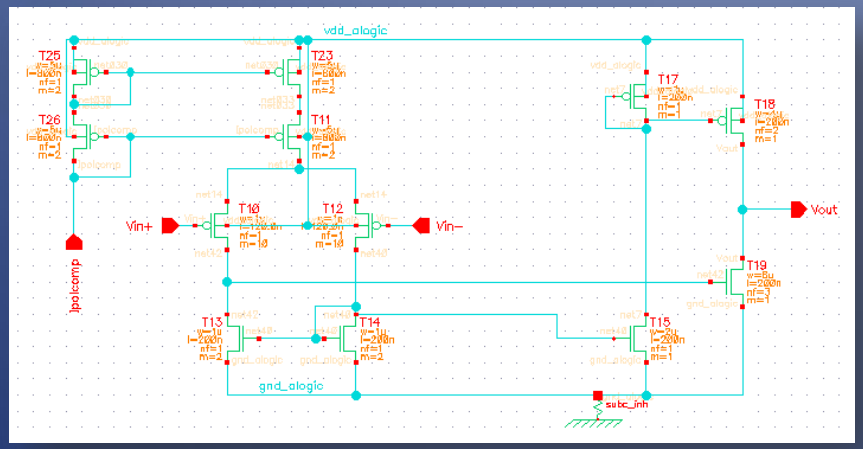
improvements

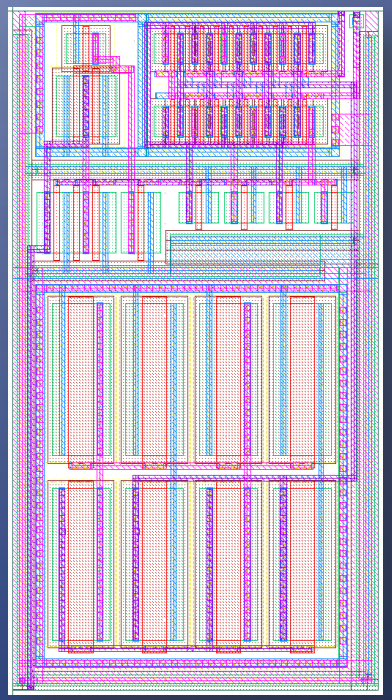
- 'frequency select' option: duty cycle of RO departs from 50% @ f<1GHz, so to run slower, send 2GHz through divide-by-4 stage. Gives clean clock up to 500 MHz.

- 'RO_enable' option: RO is free-running, but RO_en allows the fan-out drivers to be turned on/off (reducing noise).

The comparator

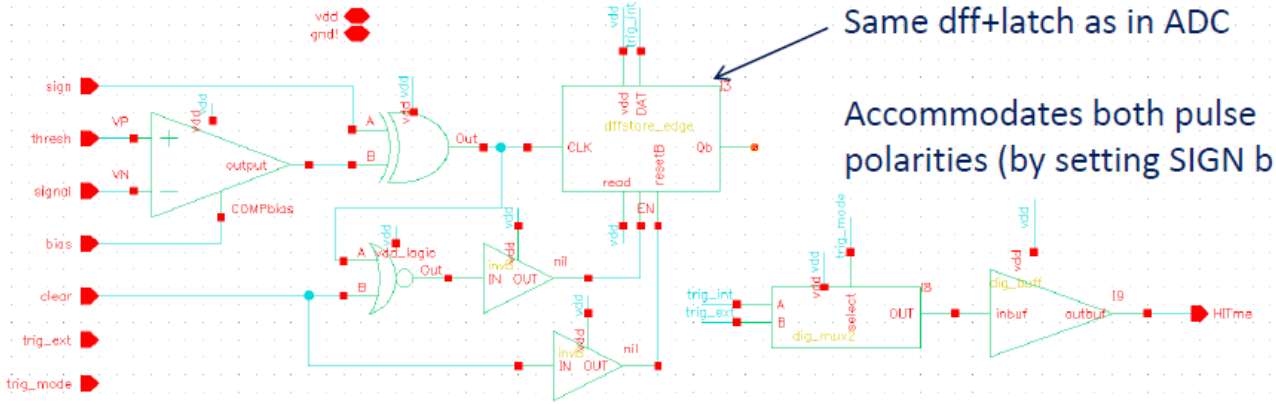
- Two comparators have been used.
  - The comparator of Psec2 has been reused
  - A fast, high gain, new comparator has been used in the test channel.

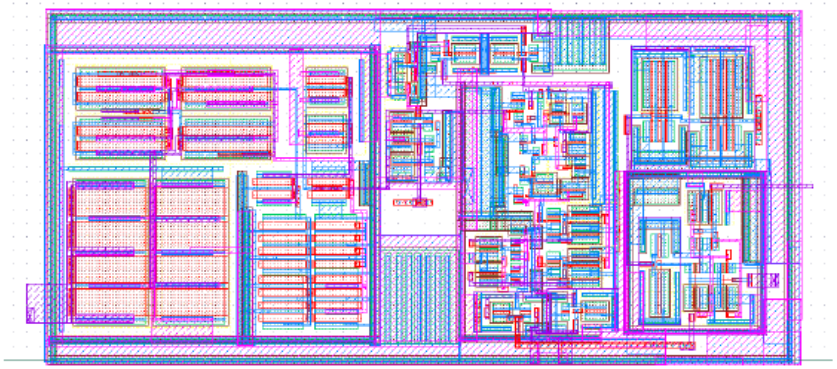




The trigger

schematic/layout

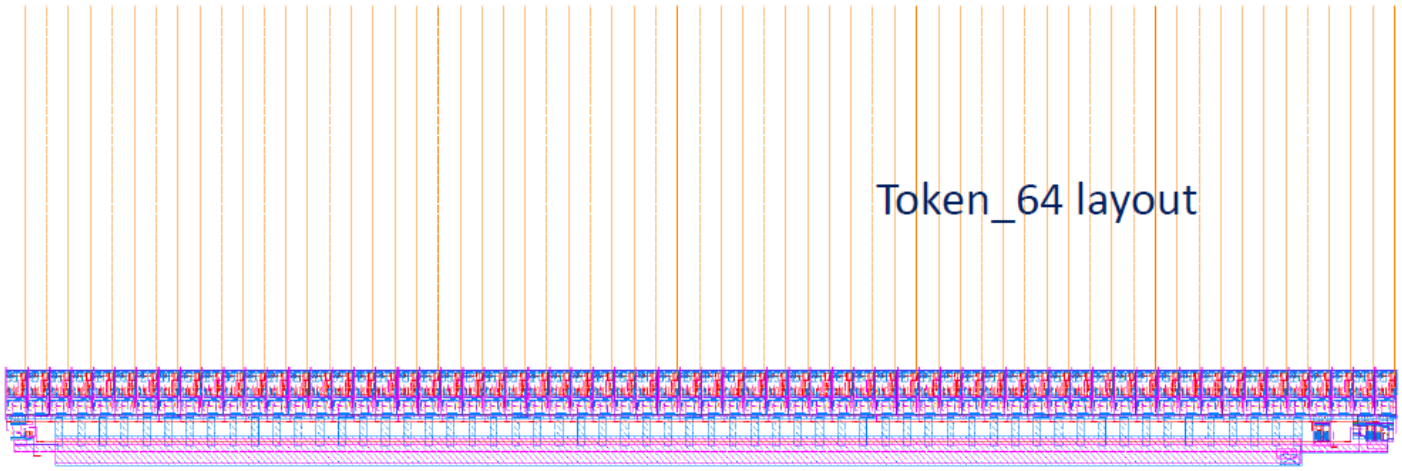




The token read-out

Token readout

- Shift register with one-shot logic
- Same design as on PSEC2 (worked as expected)



- Token made up of 4 Tok_64 blocks
- Readout blocks of 64 cells: 1-64 65-128 129-192 193-256
- Address data with Channel_select and Token_block_select + Read_Clock